Electron transport and the effect of current annealing in a two-point contacted hBN/graphene/hBN heterostructure device

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In this work, we fabricated a 2D van der Waals heterostructure device in an inert nitrogen atmosphere by means of a dry transfer technique in order to obtain a clean and largely impurity free stack of hexagonal boron nitride (hBN)-encapsulated few-layer graphene. The heterostructure was contacted from the top with gold leads on two sides and the device's properties including intrinsic charge carrier density, mobility and contact resistance were studied as a function of temperature from 4 K to 270 K. We show that the contact resistance of the device mainly originates from the metal/graphene interface, which contributes a significant part to the total resistance. We demonstrate that current annealing affects the graphene/metal interface significantly, whereas the intrinsic carrier density and carrier mobility of the hBN-encapsulated few-layer graphene are almost unaffected, contrary to often reported mobility improvements. However, after current annealing, a 75 % reduction in the contact resistance improves the overall performance of such a heterostructure device and the backgate-dependent transfer curve becomes more symmetric with respect to the Dirac point. A maximum carrier mobility of $11\,200\,\mathrm{cm^2V^{-1}s^{-1}}$ for this hBN/graphene/hBN heterostructure was measured at 4 K, showing good device performance, in particular, after current annealing.

I. INTRODUCTION

The recent development of techniques for combining graphene with other atomically thin van der Waals (vdW) crystals has led to the exploration of the characteristic properties of these so-called vdW heterostructures[1]. Hexagonal boron nitride (hBN) is one of the most popular vdW materials[1] and exhibits extraordinary properties, such as an atomically smooth surface and a large band gap[2], enabling electronic devices with low disorder and impurity concentration. Insulating hBN has received great attention as a substrate material for high performance graphene electronic devices with significantly reduced electron-hole puddles, compared to a SiO_2 substrate material[3]. Thus, heterostructures based on a combination of both materials are promising for 2D graphene-based nanoelectronics[4–6], such as field-effect transistors. In order to transfer 2D flakes on top of each other, a robust and efficient "dry transfer" technique for producing vdW heterostructure devices is necessary that can be developed, based on existing transfer techniques[7–12], to produce hBN/graphene/hBN structures. Contrary to the "wet transfer" process[13], the dry transfer technique leads to less residues, due to omitting solvents and chemical preparation steps, and results in less interfacial bubbles and wrinkles[7] and, as a consequence, shows an enhanced device performance. It is also a quick and efficient way to build multilayer two-dimensional vdW stacks[12]. Arbitrary exfoliated flakes can be selected by a microscope and picked up with a transfer stamp in a transfer stage such that a multilayer stack can be designed for specific requirements. In order to build a largely impurity-free heterostructure device we carried out the transfer in a nitrogen filled glove-box ($O_2 < 3\,\mathrm{ppm}$, $H_2O < 3\,\mathrm{ppm}$) and encapsulated the graphene sheet by hBN from the top and the bottom. This prevents the adsorption of significant oxygen and other impurities, especially in later device building steps. Beyond the clean fabrication of the stacks, additional improvements have been reported by annealing the stacks by current injection. In particular improvements of the mobility have been claimed[14], while the important contact resistance has often been neglected. In this work, the properties of few-layer graphene, encapsulated by hBN, are studied with devices fabricated in a special clean dry transfer process. We measure the key properties of charge transport in graphene, such as charge carrier densities and mobilities as a function of temperature. We carry out current annealing experiments to optimize the device performance and to observe its impact on carrier density, carrier mobility and in particular contact resistance, where large changes occur. All measurements correspond to a single sample, although several samples were produced but not characterized electrically.

II. EXPERIMENT

A. Sample preparation

In order to build a 2D heterostructure stack of various 2D layers, a dry transfer technique[10,12] was used. In our case, this comprises a clean transfer process with a minimal amount of bubbles, wrinkles and interfacial contamination[7]. This technique is based on the interfacial van der Waals-interaction between 2D layers. In the case of graphene and hBN, the attractive force is stronger between these 2D crystals as between a rough SiO_2 substrate and graphene or hBN[12]. Initially, a transfer stamp has to be prepared, out of a glass slide, MMA (methylmethacrylate), PDMS (poly-dimethylsiloxane) and PMMA (poly-methylmethacrylate) as depicted in Fig. 1a. Since PDMS is soft, chemically inert and transparent with a hydrophobic surface[15], it is an appropriate material for a 2D pick-up transfer. To further enhance the hydrophobic properties of PDMS and to reduce residues on its surface[16], PDMS

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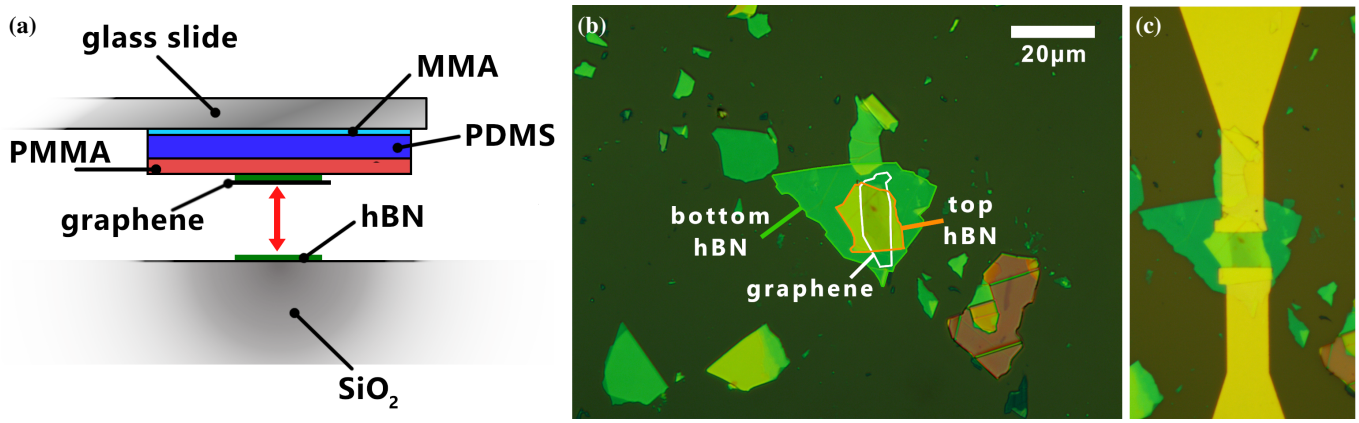

FIG. 1. In (a), the dry transfer stamp, composed of a glass slide, methylmethacrylate (MMA), polydimethylsiloxane (PDMS) and polymethylmethacrylate (PMMA) for the transfer of graphene or hBN onto a silicon wafer or on top of a 2D crystal is illustrated. In (b), a microscope image of the final structure is shown, where few-layer graphene is sandwiched by two approx. 60 nm thick hBN crystals. In (c), the same structure is presented with uncovered graphene parts contacted by gold electrodes, carried out with electron-beam lithography (EBL).

was treated in a UV-O_3 chamber at 1 L/min oxygen flow for 20 minutes. Moreover, the silicon present in PDMS reacts with oxygen atoms to form a $20-30$ nm thick layer of silicon oxide on PDMS leading to improved surface characteristics[17]. A small PDMS cuboid of 1 mm length was placed on a glass slide and glued with a drop of MMA (dissolved in ethyl lactate) onto the slide. An additional PMMA layer on top of the PDMS was used in order to improve the pick-up probability, due to enhanced cohesion between the 2D crystal and the PMMA. The whole transfer was carried out in a nitrogen filled glove box ($O_2 < 3$ ppm, $H_2O < 3$ ppm) with a transfer stage[18] and a microscope.

B. Pick-up transfer process

As a first step, an exfoliated hBN flake with appropriate size and thickness from a SiO_2 substrate is selected and the transfer stamp is then pressed softly onto the flake to have a direct contact of hBN and PDMS. Thereafter, the substrate is heated up to about 80 °C to enhance the probability of the pick-up of the flake. After three minutes the stamp can be withdrawn slowly such that the 2D flake is attached to the transfer stamp. Next, the substrate is changed to one with exfoliated graphene flakes and a few-layer graphene flake is picked up. Finally, the bilayer (graphene/hBN) is dropped onto a larger hBN crystal, by heating up the stamp to approximately 120 °C, resulting in a clean hBN/graphene/hBN heterostructure, as shown in Fig. 1b.

For this device, the top hBN flake is smaller than the bottom one and only covers the few-layer graphene flake partially. This allows for the contacting of the graphene flake from the top by contacting the uncovered parts with contact leads. The precise pattering of the contact leads was realized by electron-beam lithography (EBL). The leads were made out of 5 nm chromium and 55 nm gold deposited by means of magnetron sputtering. The area of the graphene sheet, which is covered by the metal, is approximately 15 μm^2 (at each contact site) and area encapsulated by hBN approximately 100 μm^2. An image of the final contacted structure is shown in Fig. 1c.

III. RESULTS AND DISCUSSION

Transfer curves of the hBN/graphene/hBN-device were measured from 270 K down to 4 K in a cryostat. The resistance was measured depending on the backgate voltage V_{bg} applied to the SiO_2/Si-substrate in steps of one volt. The voltage V_d, at the peak of a transfer curve called charge neutrality point or Dirac point appears to be negative for all curves, which indicates an intrinsically n-doped device according to: $n_e - n_h = C/e \times (V_{bg} - V_d)$ with n_e/n_h the electron/hole charge carrier density, C the capacitance density of the heterostructure device and e the electron charge. The capacitance density of the device is determined, as a model of two capacitors in series, through both dielectrics, SiO_2 and hBN by: $1/C = 1/C_{SiO_2} + 1/C_{hBN} = d_{SiO_2}/\varepsilon_0\varepsilon_{SiO_2} + d_{hBN}/\varepsilon_0\varepsilon_{hBN}$. Such an intrinsic n-type doping can be caused by covalently bonded nitrogen atoms[19], which is reasonable, because a nitrogen atmosphere was present during the 2D transfer in the N_2-filled glove-box. This intrinsic charge carrier density n_0 has to be taken into account when considering the total carrier concentration in the graphene-based heterostructure device. The total charge carrier density can be approximated by[20]: $n_{total} = \sqrt{n_0^2 + n^2(V_{bg} - V_d)}$, with $n(V_{bg} - V_d)$ being the gate induced carrier concentration as described above. All further results are shown as a voltage difference of the applied backgate voltage V_{bg} and the Dirac point V_d, depicted as $V_{bg-d} = V_{bg} - V_d$.

As it can be seen in Fig. 2a, all transfer curves are slightly asymmetric, meaning that the resistance for a certain V_{bg-d} value is slightly higher than its corresponding negative value. This asymmetry likely originates from the charge transfer at the metal/graphene interface, which acts as a p-p-p junction for negative V_{bg-d} and like a p-n-p junction for posi-

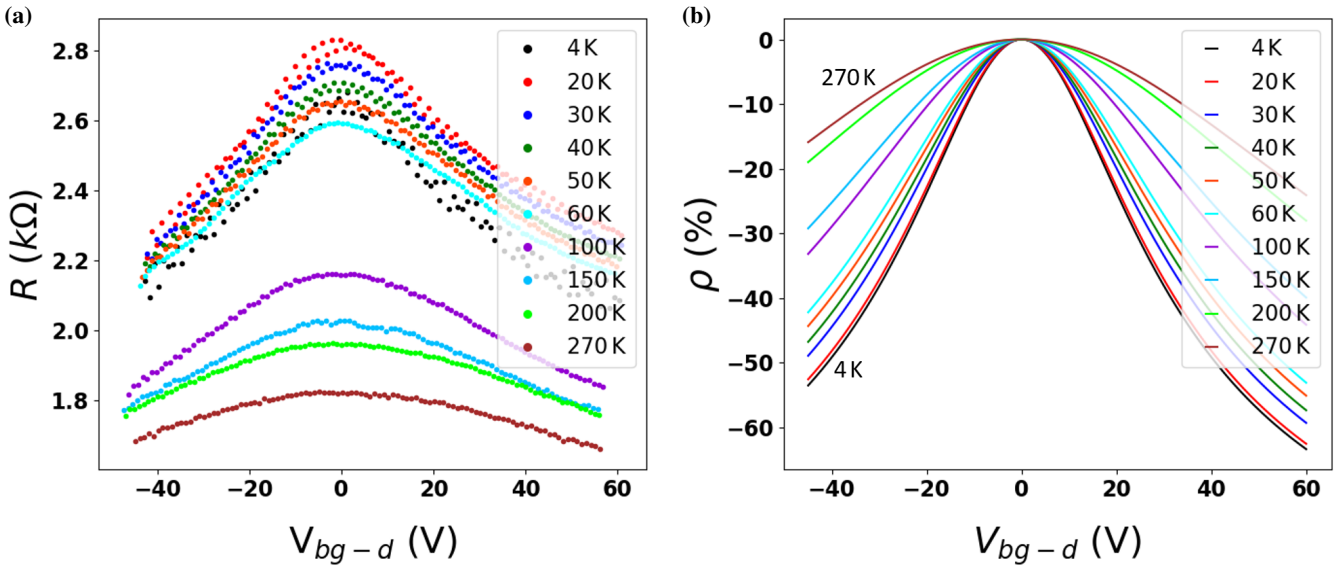

FIG. 2. Transfer curves at different temperatures ranging from 4 K to 270 K, as indicated by different colors. The measured total resistance is plotted against the voltage V_{bg-d} in (a), which is the difference of applied backgate voltage to the Dirac point. Error bars, due to measurement errors in the range of 15 Ω, are omitted for the sake of clarity. In (b), transfer curves normalized to zero V_{bg-d}, derived from fits (according to Eq. 1) of the data in a), are shown without the contribution of a contact resistance R_c. With increasing temperature the backgate effect on the relative resistance ρ increases.

tive V_{bg-d} values[21,22]. Experiments often show a clear difference between the resistivities at exactly opposite backgate voltages, which is usually attributed to different scattering cross-sections of charged impurities for opposite carrier polarities[23,24]. On the other side, this asymmetric transport property can be explained by the metal/graphene interface[25], which has been shown to be gate dependent[21], resulting in a strongly gate dependent contact resistance[26]. This interfacial effect is here regarded as an additional contribution to the contact resistance of the device and since it has a positive resistance contribution for positive applied V_{bg-d} and a negative contribution for negative V_{bg-d}[25,27], the contact resistance R_c is considered as a combination of a constant factor $R_{constant}$ and an asymmetric contribution aV_{bg-d}, with a being a fitting parameter, resulting in $R_c = R_{constant} + aV_{bg-d}$. This assumes a simplified linear dependence of the interfacial effect with the applied backgate voltage. The total resistance R of the heterostructure device can then be described by the following formula[20]:

$$R = R_c + \frac{L}{W}\frac{1}{e\mu\sqrt{n_0^2 + n^2(V_{bg}-V_d)}}, \qquad (1)$$

where n_0 is the residual charge density, $n(V_{bg}-V_d)$ the gate induced charge carrier density as described above, R_c the contact resistance, μ the mobility, L the channel length and W the width of the graphene sheet. R_c also comprises the resistance of the Cr/Au-contact pads, wires and sample holder cables, which have together approximately the size of 1 Ω. However, in comparison to the contact resistance of a few kΩ this is a negligible contribution.

The effect of the residual density n_0 on the transport behavior of graphene is only important near the Dirac point, and is negligible far away from the Dirac point. The advantage of this fitting method is the possibility to extract μ, n_0 and R_c by a single fit of a measurement of a "two-point" contacted device. For all temperatures, the transfer curves shown in Fig. 2a, were fitted with equation 1 and the parameters μ, n_0 and R_c were extracted. To better assess the temperature influence on the transfer curve of the hBN/graphene/hBN heterostructure, the relative resistance change $\rho = (R - R_d)/R_d$, with R the measured resistance of the device and R_d the resistance at the Dirac point, is plotted with the extracted parameters μ and n_0, but without the contribution of the contact resistance R_c in Fig. 2b. A consistent trend of a stronger backgate effect on the resistance for lower temperatures can be observed as expected[28]. This can be explained by the lower intrinsic charge carrier density n_0 for lower temperatures, due to less thermal activation of carriers, thus the total carrier concentration is dominated by the gate-induced charge carriers[20]. This trend for n_0 as a function of temperature is presented in Fig. 3b, with the lowest value for n_0 of approximately $1.5 \cdot 10^{12}\,\mathrm{cm}^{-2}$ at 4 K. The increase in carrier density with temperature can be explained by the thermal activation model for an hBN/graphene heterostructure[29,30] and by the theory of electron-hole puddle formation near the Dirac point[31], caused by intrinsic ripples or extrinsic charge-induced inhomogeneities.

The increase in mobility for lower temperatures, as shown in Fig. 3a, is caused by less phonon and electron-electron scattering. Phonon scattering, although being weak in graphene[32], always contributes to a reduced mobility with increasing temperature. The maximum charge carrier mobility of

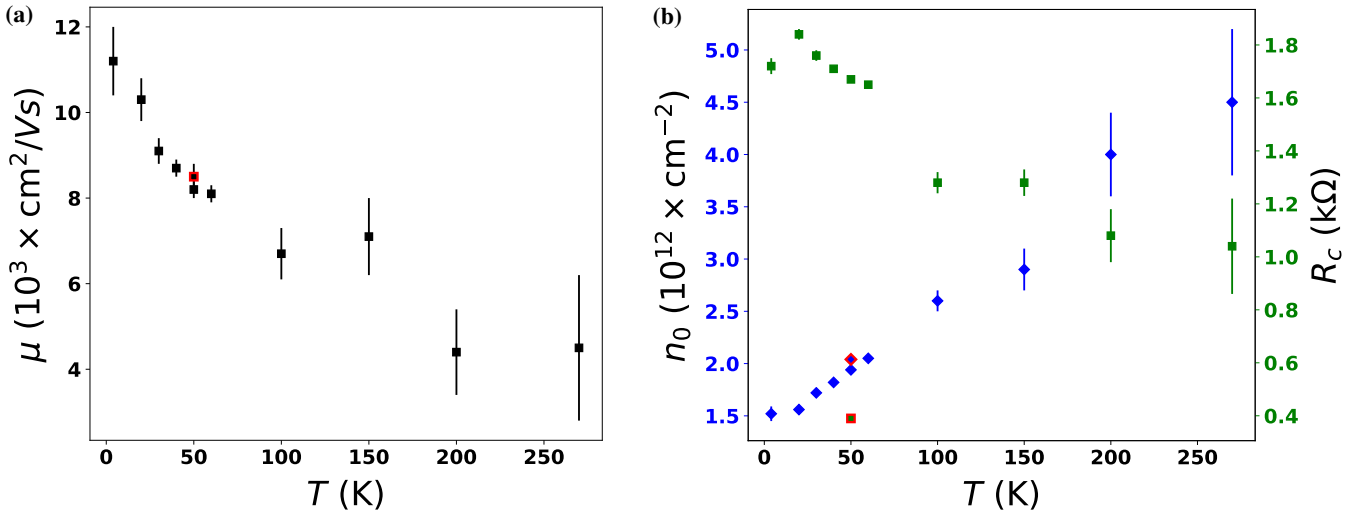

FIG. 3. The temperature dependence of mobility (a), charge carrier density (blue diamond data points) and contact resistance (green square data points) (b) is shown. Error bars are indicated and the red data points are linked to the parameters after the current annealing procedure (see. 4).

$11\,200 \pm 800\,\mathrm{cm^2V^{-1}s^{-1}}$ for this device was measured at 4 K and is higher than for typical SiO_2-substrate-based graphene devices[20,33,34].

Current annealing

A crucial and often overlooked contribution to the device performance and total resistance stems from the contact resistance, which is mainly determined by the interface of the metal contact lead and the graphene sheet. As mentioned above, a p-p-p junction occurs at the interface for negative V_{bg-d} and a p-n-p junction for positive V_{bg-d}[21]. However, this contact resistance can be improved significantly by means of current annealing. Current annealing (CA) is heating of the device due to ohmic losses[35]. This localized heating can lead to chemical desorption of adsorbents and electromigration (EM) is the transport of material caused by the gradual movement of ions in a conductor due to the momentum transfer between conducting electrons and diffusing atoms[36]. In addition, it could also lead to a rearrangement of interface atoms, by which the interface conductivity is modified. It is shown here, that after several current annealing procedures, the interface conductivity quadrupled. This increase in conductivity or drop in R_c is depicted in Fig. 3b as a green square data point with a red edge at 50 K. Contrary to the contact resistance, mobility and intrinsic carrier density were not significantly affected by the current annealing (shown as red edged data points in Fig. 3). These results reveal the significant impact of current annealing on the graphene/metal interface and for this device for the currents used we find either a clean hBN/graphene/hBN stack or more likely no significant desorption of remaining adsorbates, as corroborated by the lack of a change of n_0.

A change in n_0 would indicate that impurities of the encapsulated graphene sheet are desorbed or adsorbed to the graphene which thereby then affect the carrier density. However, this is not the case here and a more likely explanation is the impurity contaminated (due to lithography) metal/graphene interface, which could be improved by means of current annealing. Another effect might originate from electromigration at the interface. With an interface contact area of approximately $15\,\mu\mathrm{m}^2$, the maximum corresponding current density of $1.4 \cdot 10^9\,\mathrm{A/m^2}$ is of an order where electromigration effects such as the material transport in the gold electrode, caused by the electron momentum exchange and the related thermal gradient in the metal[37,38] or in our case the metal/graphene interface, can occur. The resulting depletion or accumulation of Cr and Au atoms at the interface is therefore able to influence the interface conductivity. As there are no particular chemical reactions for graphene/Cr interfaces reported, we do not expect to have particular chemical reactions occurring due to the current injection and the resulting heating. The current annealing process was conducted with the aid of a LabView program, which allows for an automatic control of the process. Six CA procedures were carried out at a temperature of 50 K. While conventionally, current annealing is done at room temperature, we carried out current annealing at 50 K to focus on electromigration effects. These can be induced by large current densities due to "electron wind" even at low temperatures, while thermal desorption requires mostly elevated temperatures. Each procedure comprised a start voltage and a target voltage V_T, which was applied as drain-source voltage and increased until the target was reached. Thereafter, the program sets the voltage back to the starting value and another cycle of incremental voltage increase is started. This is repeated about 50 times for each procedure. Fig. 4 shows the last three CA procedures with target voltages of 5, 10 and 15 volts. For each procedure the resistance at the start and at the end of the procedure is plotted as a data point, in Fig. 4a. All cycles for the three pro-

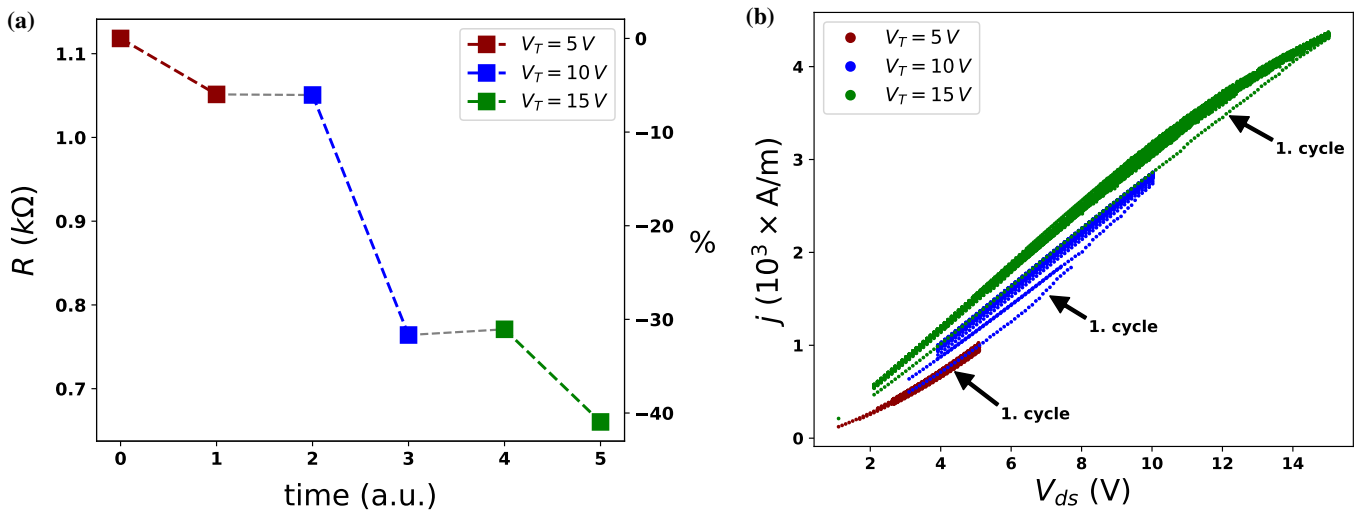

FIG. 4. The effect on the total device resistance by means of current annealing at a voltage of $V_{ds} = 5\,\mathrm{V}$ is shown in (a). Each color represents a current annealing procedure (for different target voltages) with pre- and post- resistance values indicated as data points. The dashed line serves as a guide for the eye. In (b), all cycles for each procedure are presented and the first cycle of each procedure is declared with an arrow. A significant change in resistance or in source-drain current can be seen.

cedures are plotted in Fig. 4b, where each first cycle is indicated, respectively. A gradual increase in source-drain current can be seen between CA procedures, indicating EM effects, as well as among different cycles of an individual procedure. This suggests an improvement of the device contact resistance or intrinsic charge carrier concentration. However, in Fig. 3b it was illustrated that the change in n_0 is negligible and that the change in R_c is the cause of the improved conductance. In addition, this shows the effectiveness of current induced annealing in desorbing contaminants from the interface to reduce the typically high contact resistivity for a Cr/Au electrode[39]. Another effect relates to the asymmetry of the transfer curve (see Fig. 2a), which is affected by EM in a way that the curve after CA is more symmetric than before, confirming a change in the metal/graphene interface, since this is the main origin of the asymmetry in the curve[21]. The maximum applied current density for this 2D heterostructure was approximately $4.4 \cdot 10^3\,\mathrm{A/m}$ and similar to current densities used for current annealing treatment in few-layer graphene devices[35]. As it is shown in this work, the contact resistance significantly limits the device performance and current annealing targets this limitation by improving the metal/graphene interface. It is likely that this improvement is mostly due to the rearrangement of interface atoms and desorption of adsorbants at the interface and not at the graphene sheet, since graphene is encapsulated by hBN (not "free standing"). Also CA affected the symmetry of the transfer curve, indicating a change at the interface. Contrary to other graphene field-effect devices, where current annealing improves the device performance due to an increase in carrier mobility[14], for our device, the enhanced performance stems from the impact on the interface, namely the contact resistance and not mobility. The change in mobility or carrier density due to CA is here negligible. Our results are valuable for top-contacted hBN/graphene/hBN heterostructures devices to reduce the interface resistance and to enhance the device performance.

IV. CONCLUSION

A hBN/graphene/hBN heterostructure device, fabricated in a nitrogen atmosphere by means of a dry transfer technique, was developed on a SiO_2 substrate and top-contacted with gold electrodes. Its intrinsic charge transport properties, like carrier mobility, intrinsic carrier density and contact resistance were studied from 4 K to 270 K. The fitting method allowed us to gain information about these parameters for a two-point contacted heterostructure device. By means of current annealing, it has been shown, that the graphene/metal interface can be improved significantly, whereas the intrinsic carrier density and carrier mobility of the hBN-encapsulated few-layer graphene are almost unaffected, contrary to other reports where the annealing affects mobility or carrier density. A 75 % lower contact resistance improves the overall performance of such a heterostructure device and therefore is be a valuable finding for the future development of 2D vdW devices. The observed asymmetry of the transfer curves is most likely attributed to the charge transfer at the metal/graphene interface and has been shown to be improvable by use of current annealing. For an increased performance in hBN/graphene heterostructure devices, current induced annealing should be considered.

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DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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