HCl Gas Gettering of 3d Transition Metals for Crystalline Silicon Solar Cell Concepts

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Abstract

In order to reduce the costs of crystalline silicon solar cells, low-cost silicon materials like upgraded metallurgical grade (UMG) silicon are investigated for the application in the photovoltaic (PV) industry. Conventional high-purity silicon is made by cost-intensive methods, based on the so-called Siemens process, which uses the reaction to form chlorosilanes and subsequent several distillation steps before the deposition of high-purity silicon on slim high-purity silicon rods. UMG silicon in contrast is gained from metallurgical silicon by a rather inexpensive physicochemical purification (e.g., acid leaching and/or segregation). However, this type of silicon usually contains much higher concentrations of impurities, especially 3d transition metals like Ti, Fe, and Cu. These metals are extremely detrimental in the electrically active part of silicon solar cells, as they form recombination centers for charge carriers in the silicon band gap. This is why simple purification techniques like gettering, which can be applied between or during solar cell process steps, will play an important role for such low-cost silicon materials. Gettering in general describes a process, whereby impurities are moved to a place or turned into a state, where they are less detrimental to the solar cell. Hydrogen chloride (HCl) gas gettering in particular is a promising simple and cheap gettering technique, which is based on the reaction of HCl gas with transition metals to form volatile metal chloride species at high temperatures.

The aim of this thesis was to find the optimum process parameters for HCl gas gettering of 3d transition metals in low-cost silicon to improve the cell efficiency of solar cells for two different cell concepts, the standard wafer cell concept and the epitaxial wafer equivalent (EpiWE) cell concept. Whereas the former is based on a wafer which is the electrically active part of the solar cell, the latter uses an electrically inactive low-cost silicon substrate with an active layer of epitaxially grown silicon on top. Low-cost silicon materials with different impurity grades were used for HCl gas gettering experiments with the variation of process parameters like the temperature, the gettering time, and the HCl gas concentration. Subsequently, the multicrystalline silicon neighboring wafers with and without gettering were compared by element analysis techniques like neutron activation analysis (NAA). It was demonstrated that HCl gas gettering is an effective purification technique for silicon wafers, which is able to reduce some 3d transition metal concentrations by over 90%. Solar cells were processed for both concepts which could demonstrate a significant increase of the solar cell efficiency by HCl gas gettering. The efficiency of EpiWE cells could be increased by HCl gas gettering by approximately 25% relative to cells without gettering. First process simulations were performed based on a simple model for HCl gas gettering processes, which could be used to make qualitative predictions.

Zusammenfassung

Um die Kosten für kristalline Silicium-Solarzellen zu senken, wird kostengünstiges „upgraded metallurgical grade“ (UMG)-Silicium für den Einsatz in der Photovoltaik-Industrie untersucht. Konventionelles hochreines Silicium wird mit Hilfe von aufwendigen Verfahren hergestellt, basierend auf dem sogenannten Siemensprozess. Dieser nutzt die Reaktion zu Chlorsilanen, die anschließend mehrfach destilliert und an dünnen hochreinen Silicium-Stäben abgeschieden werden. Dagegen wird UMG-Silicium aus Rohsilicium über physikalisch-chemische Reinigung (z.B. Säureextraktion und/oder Segregation) gewonnen. Dieses Silicium enthält jedoch viel höhere Verunreinigungs-Konzentrationen, vor allem 3d-Übergangsmetalle, wie z.B. Ti, Fe, Cu. Diese Metalle sind extrem schädlich im elektrisch aktiven Teil von Solarzellen, weil sie Ladungsträger-Rekombinationszentren in der Bandlücke von Silicium bilden. Deshalb werden einfache Reinigungsverfahren wie das Gettern eine wichtige Rolle für solche kostengünstigen Silicium-Materialien spielen, das zwischen oder während Zellprozess-Schritten angewendet werden kann. Gettern allgemein ist ein Prozess, bei dem Verunreinigungen entfernt oder dahin bewegt werden, wo sie für die Solarzelle weniger schädlich sind. Speziell HCl-Gettern ist ein vielversprechender, einfacher und kostengünstiger Getter-Prozess, welcher auf der Reaktion von gasförmigem Chlorwasserstoff (HCl) mit Metallen und der Bildung von bei hohen Temperaturen flüchtigen Metallchloriden beruht.

Ziel der Arbeit war es, optimale Prozessparameter für HCl-Gettern von 3d-Übergangsmetallen in kostengünstigem Silicium zu finden, um den Zellwirkungsgrad für zwei verschiedene Zellkonzepte zu verbessern, das Standard-Wafer-Zellkonzept und das Epitaktische Waferäquivalent-Zellkonzept. Während das erstgenannte auf einem Silicium-Wafer basiert, der elektrisch aktiv ist, benutzt das zweite ein elektrisch nicht aktives kostengünstiges Silicium-Substrat mit einer darauf abgeschiedenen aktiven Silicium-Schicht. In der vorliegenden Arbeit wurden kostengünstige Silicium-Materialien mit verschiedenen Verunreinigungsgraden für HCl-Getter-Experimente mit Prozessparameter-Variation von Temperatur, Getterdauer und HCl-Konzentration verwendet. Anschließend wurden die multikristallinen Folgewafer mit und ohne Gettern mit Elementanalyse-Verfahren wie Neutronenaktivierungs-Analyse (NAA) verglichen. Es wurde gezeigt, dass HCl-Gettern eine wirksame Reinigungsmethode für Siliciumwafer darstellt und manche Übergangsmetallkonzentrationen um mehr als 90% senken kann. Für beide Zellkonzepte wurden Solarzellen hergestellt, die eine deutliche Erhöhung des Zellwirkungsgrades durch HCl-Gettern aufwiesen. Der Wirkungsgrad konnte durch HCl-Gettern um 25% (relativ) gesteigert werden. Erste Prozesssimulationen wurden auf Basis eines einfachen HCl-Getter-Modells durchgeführt, die für qualitative Vorhersagen verwendet werden konnten.

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1 Introduction

The most common solar cell technologies are based on crystalline silicon. They have a market share of over 80% of today's photovoltaic (PV) market [1]. Silicon has some benefits as material for solar cells. It is one of the most abundant elements in the earth's crust (27.7% by weight). It is a non-toxic and well-known semiconductor material. Raw silicon, which is called metallurgical grade (MG) silicon, is produced from quartz and is relatively inexpensive. It still contains a lot of dopants and metallic impurities and is conventionally purified by the Siemens process, which is based on the reaction to gaseous chlorosilanes and subsequent distillation steps. However, the Siemens process is expensive compared to the production of MG silicon. Although today it is still the most common method, alternative physicochemical purification processes are investigated to reduce the cost of silicon for solar cells. For example, the reduction of dopants and metals can be done by processes like slag treatment and segregation, respectively. The product is called upgraded metallurgical grade (UMG) silicon and still contains high amounts of impurities, mainly C, O, N, B, P, Al, Ca, and 3d transition metals like Ti, V, Cr, Mn, Fe, Co, Ni, and Cu. Especially transition metals are detrimental for solar cells even in small concentrations, as they form recombination centers in the silicon band gap. Depending on the type and number of applied purification steps, the impurity levels of UMG silicon can vary in large ranges.

When UMG silicon is used for crystalline silicon solar cell concepts, it is crucial to apply an additional step on the way from wafer to solar cell to further reduce detrimental impurities like transition metals. This can be effectively done by processes, whereby the transition metals are either moved to a place in the cell, where they are less detrimental or completely removed from the cell. This technique is called gettering. The most common gettering techniques are phosphorus gettering and aluminum gettering, which occur during standard cell processes like the P emitter diffusion and the rear side Al contact formation. Hydrogen chloride (HCl) gas gettering is an alternative promising gettering technique which can be applied to crystalline silicon solar cell concepts and will be introduced and investigated as the main focus of this work.

HCl gas gettering is a chemical gettering technique with a gettering effect based on the reaction of HCl with transition metals to form volatile chloride species. The chloride species are removed from the silicon wafer surface, whereby a concentration gradient occurs,

leading to an enhanced diffusion of transition metals from the wafer bulk to the surface. HCl gas gettering is known from the microelectronic industry and has to be adopted for the purpose of solar cell applications, as the requirements are different. The removal of much higher impurity concentrations from the whole wafer bulk instead of only the surface region and the use of a different gas atmosphere are required. HCl gas gettering has been investigated in this work for the application in two crystalline silicon based solar cell concepts. The standard wafer cell concept is the most common concept used in the PV industry. It is based on a wafer which is the electrically active part of the solar cell. The second concept is the epitaxial wafer equivalent (EpiWE) cell concept, which is based on an electrically inactive low-cost silicon substrate with an active layer of epitaxially grown silicon on top. In order to reduce the cost of future solar cells, both concepts could use low-cost silicon materials, in principle. Though, the standard wafer cell concept has much higher requirements as compared to the EpiWE cell concept regarding the contents of transition metals and especially of doping elements in low-cost silicon. Nevertheless, HCl gas gettering could represent an effective purification step for both cell concepts when appropriate low-cost silicon materials are used. In the next paragraph an outline of this work will be given.

In the following chapter 2, the various silicon materials are introduced including their terminology and specification. These silicon materials are used for the two different cell concepts, the standard wafer solar cell concept and the EpiWE cell concept, which are described subsequently. In the second part of the chapter the most relevant used analysis techniques are briefly presented with an emphasis on the respective sample preparations and detection limits.

Chapter 3 deals with HCl gas gettering in silicon. First, the most relevant properties of 3d transition metals in silicon with regard to gettering, such as diffusion, distribution and the impact on solar cells, are described. Secondly, the reaction of HCl with the matrix silicon will be investigated, as it occurs during HCl gas gettering at high temperatures. The reaction mechanism, the reaction kinetics, and the threshold temperature of HCl etching of silicon are discussed followed by a brief characterization of the surface morphology of some exemplary HCl processes. Thirdly, the mechanism of HCl gas gettering is discussed starting from the general definition of gettering and conventional gettering techniques. The mechanism steps of HCl gettering are successively described with emphasis on the gettering efficiency limiting potential of each step. Finally, the mainly used lab-type reactor and a typical HCl gas gettering process are presented, followed by a discussion of contamination sources during gettering.

In chapter 4, the typical vertical and horizontal impurity distribution in a multicrystalline silicon ingot is introduced followed by a detailed analysis of 3d transition metals in

neighboring wafers of the MG and UMG silicon materials which were used in this work for HCl gas gettering. The results of this chapter are relevant for chapter 5.

Chapter 5 describes the results of several HCl gas gettering experiments and solar cells. It is structured into four parts. Both the first and the second part deal with the EpiWE cell concept. In the first part, the element-analysis results of HCl gas gettering in MG silicon wafers are presented. In the second part, analysis results of UMG silicon wafers are shown with variation of the parameters temperature, gettering time, and HCl gas concentration. The third part of this chapter deals with the standard wafer cell concept. The different requirements of HCl gas gettering for the standard wafer cell concept compared to the EpiWE cell concept is pointed out and minority carrier lifetime measurements are shown both for gettering experiments in the lab-type reactor and in an industrial-type diffusion furnace. In the fourth part, solar cell results of EpiWE cells and standard wafer cells with and without HCl gas gettering are presented and compared.

In chapter 6, a first simulation model for HCl gas gettering processes is introduced, which is based on diffusion equations of 3d transition metals in silicon. The assumptions and simplifications, which the model is based on, will be explained. The results of the simulations are shown, focusing on the influence of the most relevant simulation parameters, which are the transport coefficient, the temperature, and the gettering time.

The main results of this work are finally summarized in chapter 7.

2 Solar cell concepts and characterization methods applied

In the first part of this chapter, different silicon materials are introduced, which are defined by their manufacturing method and their purity level. These silicon materials are the basis of two further described silicon solar cell concepts, which were applied in this work, the standard wafer cell concept, and the epitaxial wafer equivalent (EpiWE) cell concept. In the second part of this chapter, the mainly applied analysis techniques are briefly described including sample preparation.

2.1 Crystalline silicon solar cell concepts

In this work, solar cell structures were processed to investigate the improvement by HCl gas gettering on solar cell level. Two different cell concepts were applied: the standard wafer cell concept, which is the most common concept used in the solar cell industry today, and the EpiWE cell concept, which is based on a thin silicon layer on top of a low-cost silicon substrate, and which amongst others is pursued at the *Fraunhofer ISE*. Both concepts are briefly described after an introduction about the definition of silicon materials, which are used for the cell concepts.

2.1.1 Silicon materials

There are various types of silicon, which can be classified by their manufacturing route and by their purity levels. Silicon is manufactured by the electrothermic reduction of quartz with coal at ~ 1800°C:

$$690\ \mathrm{kJ} + SiO_2 + 2C \rightarrow Si + 2CO\ . \qquad (2\text{-}1)$$

To prevent the production of SiC, an excess of C must be avoided. The produced silicon is called metallurgical grade (MG) silicon and is the starting material for other silicon materials. Conventional multicrystalline (mc) silicon is made by using a process sequence including the common Siemens process [2, 3], whereby gaseous trichlorosilane ($SiHCl_3$) is reduced to silicon, which is deposited on silicon rods. In the first step, $SiHCl_3$ is produced by the reaction of MG silicon with hydrogen chloride (HCl) in a fluidized bed reactor at ~ 300°C:

$$Si + 3HCl \rightarrow SiHCl_3 + H_2 + 218\,\text{kJ} \ . \qquad (2\text{-}2)$$

In the second step, $SiHCl_3$ is separated from byproducts like silicon tetrachloride ($SiCl_4$) and dichlorosilane (SiH_2Cl_2) by fractional distillation. A high purity of the $SiHCl_3$ can be achieved by several distillation processes. In the third step, the actual Siemens process is performed in a Siemens reactor, where the silicon is deposited on high-purity slim silicon rods at ~ 1150°C, according to the following reaction:

$$964\,\text{kJ} + 4SiHCl_3 + 2H_2 \rightarrow 3Si + SiCl_4 + 8HCl \ . \qquad (2\text{-}3)$$

The product is polycrystalline silicon and is called electronic grade (EG) silicon. It can be crystallized by ingot casting to obtain conventional mc silicon. Monocrystalline (mono-c) silicon, which is used in the semiconductor industry, and is often used as reference silicon material in the photovoltaic research sector, can be obtained by the Czochralski (Cz) process or by the float zone (FZ) process. Cz silicon is gained by introducing a seed crystal into the polycrystalline silicon melt and pulling it out slowly while rotating. Single crystals with a diameter of up to 30 cm and a length of 1.5 m are obtained. FZ silicon is gained by passing a polycrystalline rod through a heating coil, whereby the silicon melts, and the molten zone is floating through the rod. Both processes are described detailed in [4].

The conventional route to gain pure silicon using the Siemens process has a high energy consumption and is therefore cost-intensive. To reduce the cost of silicon for the photovoltaic industry, the production of solar grade (SoG) silicon was forced recently. The definition ‘solar grade’ implies that this type of silicon has reduced purity requirements compared to EG silicon, which is used in the semiconductor industry, but still is suitable for solar cell production. This means that especially concentration of dopants must not be too high with a significantly lower concentration of phosphorus compared to that of boron in the case of p-type silicon. Two routes are pursued, the simplification or modification of the conventional Siemens process and the metallurgical route, which means the physico-chemical purification of MG silicon without the formation of chlorosilanes. The product of the latter route is called upgraded metallurgical grade (UMG) silicon. This route can be significantly more cost efficient than the conventional Siemens process [5]. However, the removal of many impurities is challenging. The impurity reduction is focused on dopants and metals, especially transition metals. There are several purification processes that can be applied in the metallurgical route, e.g., acid leaching or segregation, which are further described in [6]. Depending on the type and number of used purification steps, the purity levels of UMG silicon can vary a lot. This is visualized in Fig. 2.1, where impurity concentrations in silicon materials are given, which were sold as UMG silicon.

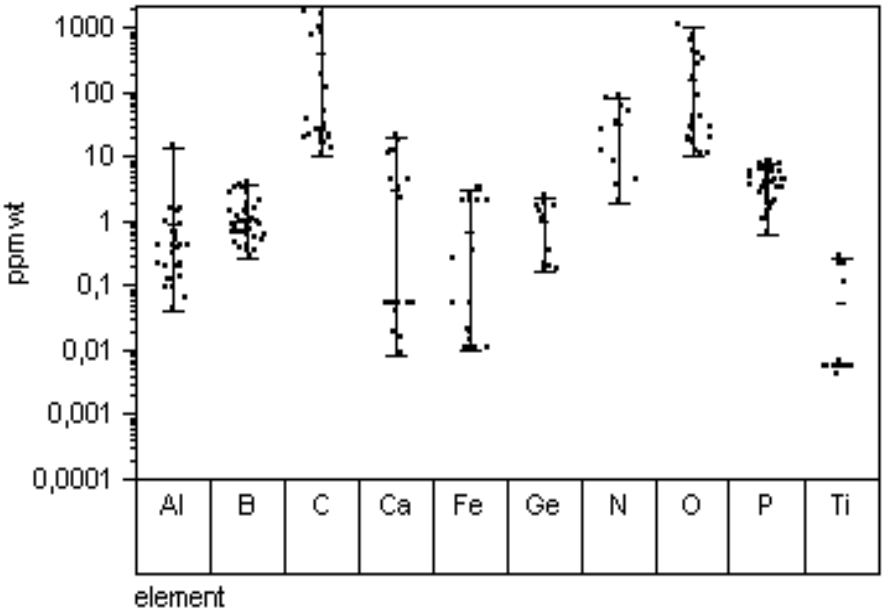

Fig. 2.1 Large impurity concentration ranges in silicon materials, which were sold as UMG silicon [7].

To give an overview over the several types of silicon materials, a rough classification by the purity level is presented in Table 2.1. It can be summarized that the purity levels in silicon materials can have large differences. The concentrations of the transition metals which can be found in silicon materials range from below ppbw[1] (ng/g) in EG silicon to hundreds of ppmw[2] (µg/g) in MG silicon. In the unit of atoms per cm^3, depending on the element, this corresponds to approximate values of below 10^{12} cm^{-3} up to 10^{19} cm^{-3}. Mono-c silicon is the material with the highest purity level. For example, high quality Cz silicon typically contains less than 10^{10} cm^{-3} of metal impurities [8].

Table 2.1 Classification of silicon material types.

Type of silicon material	Silicon purity level [%]
MG	99 – 99.9 (2N – 3N)
UMG	99.9 – 99.999 (3N – 5N)
SoG	99.99 – 99.99999 (4N – 7N)
EG	99.99999 – 99.999999 (7N – 8N)

[1] ppbw = parts per billion by weight

[2] ppmw = parts per million by weight

The silicon materials are present in the form of chunks, flakes, or granulate, and are used as feedstock for the crystallization by ingot casting. The bottom, top, and side parts of the ingot are usually cut away, the rest of the ingot is cut to bricks, and subsequently to mc wafers by multi-wire sawing [9]. Cz silicon, which is usually present as large cylindrical ingots, can be directly cut to mono-c wafers. It must be noted that the mc wafers, which were crystallized by ingot casting, can again have different purity levels as compared to their feedstock material, since crystallization usually leads to reduced metal concentrations due to the segregation effect, but at the same time acts as a contamination source for impurities like O, C, N, and also common transition metals.

2.1.2 Standard wafer cell concept

The standard wafer solar cell concept is based on a moderately-doped silicon wafer. Most commercial cells are made from mc SoG or EG silicon wafers, but low-cost materials like moderately-doped UMG silicon are investigated and intended for the standard wafer cell concept. However, the requirements of UMG material for the standard wafer cell concept are rather strict, as the doping level must not be too high to prevent the recombination of generated carriers. Fig. 2.2 (a) presents the scheme of a p-type doped standard silicon wafer solar cell. To create a p-n junction near the wafer surface, a highly n-type doped (n+) emitter is formed by a phosphorus diffusion step. The contacts are usually realized by a full-area Al layer on the rear side and a silver grid with busbars and fingers on the front side, which is industrially made by screen printing of Al and Ag pastes. The contact is improved by a high temperature firing step, which also leads to an Al p+ back surface field (BSF). The BSF prevents minority carriers, in this case electrons, from diffusing to and recombining at the rear side [10, 11]. The surface is usually passivated by a silicon nitride layer (not included in the scheme), which also acts as an antireflection coating (ARC). In a lab-scale, the passivation can also be done by oxidation and a double layer antireflection coating can be applied.

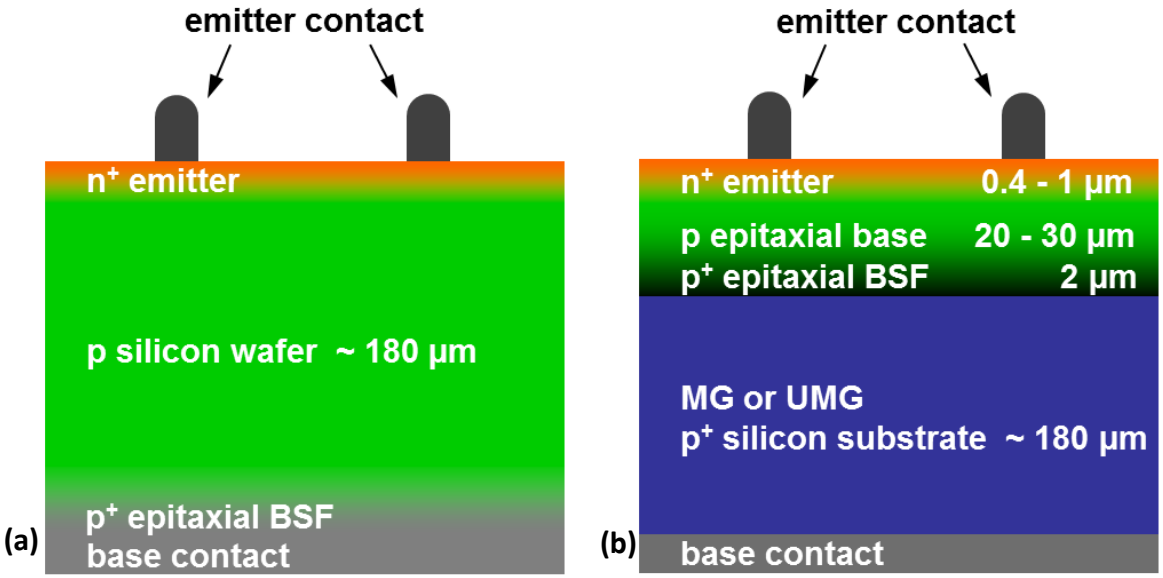

Fig. 2.2 Schemes of solar cell concepts: the standard wafer cell concept (a), and the epitaxial wafer equivalent (EpiWE) cell concept (b). The schemes are not to scale.

Detailed descriptions of the fundamental physics of solar cells can be found in [12-15]. Only the relation of the main cell parameters shall briefly be introduced. The conversion efficiency η_{cell} of a solar cell is defined by the power density at the cell operating point, which is called maximum power point P_{max}, divided by the incident light power density P_{inc}:

$$\eta_{\mathrm{cell}} = \frac{P_{\mathrm{max}}}{P_{\mathrm{inc}}} = \frac{V_{\mathrm{max}}\, J_{\mathrm{max}}}{P_{\mathrm{inc}}} = \frac{V_{OC}\; J_{SC}\; FF}{P_{\mathrm{inc}}}, \tag{2-4}$$

whereby V_{OC} is the open circuit voltage, J_{SC} is the short circuit current, and FF is the fill factor. V_{max} and J_{max} are the voltage and the current density at the maximum power point, respectively. The characterization of a solar cell can be done by *I-V* measurements. The cell is illuminated under standardized conditions and the main cell parameters can be extracted from the illuminated *I-V* curve as shown in Fig. 2.3. The FF is a curve ideality factor and describes the rectangularity of the *I-V* curve. According to eq. (2-4) it can be written as

$$FF = \frac{V_{\mathrm{max}}\, J_{\mathrm{max}}}{V_{OC}\; J_{SC}}. \tag{2-5}$$

The FF can be graphically interpreted as the ratio between the red-dotted and the blue-dotted rectangular area in Fig. 2.3.

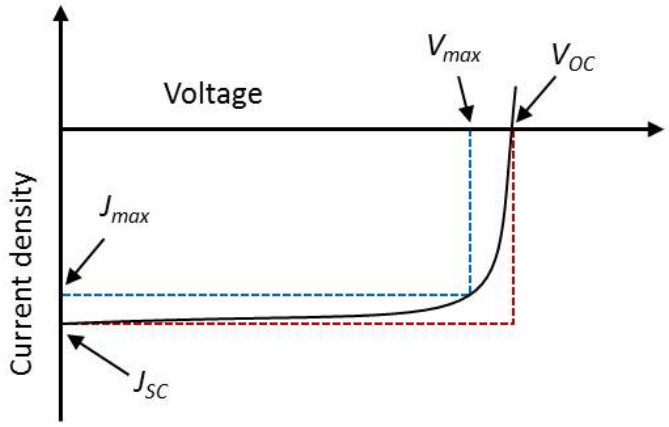

Fig. 2.3 Scheme of an illuminated *I-V* curve of a silicon solar cell. The fill factor (*FF*) can be graphically interpreted as the ratio of the red-dotted and the blue-dotted rectangular areas.

As is described in section 3.1.3, charge carriers can recombine at recombination centers, which are represented by impurities and defects in the silicon. Therefore, impurities like transition metals affect the minority carrier diffusion length *L*, which is related to the minority carrier lifetime τ as follows:

$$L = \sqrt{D_C\,\tau}\,, \tag{2-6}$$

where D_C is the charge carrier diffusivity. The introduced fundamental equations (2-4) and (2-6) are also valid for the epitaxial wafer equivalent (EpiWE) solar cell.

The main process steps, which were used in this work, starting from the silicon wafer and ending with the final characterization of the cells, are presented in Fig. 2.4. Cells with and without gettering can be compared. The wafers were treated by a chemical polishing (CP) etching solution (HF/HNO_3) to remove the saw damage. Then the gettering was performed. To reach high cell efficiencies a clean-room cell process was applied at *Fraunhofer ISE* for the standard wafer cell concept. A diffused $POCl_3$ emitter with a sheet resistance of approx. 120 Ω/sq (ohms per square) was applied, followed by an oxide surface passivation step, resulting in a silicon oxide layer of approximately 10 nm. The metallization was done by photolithography. The front side contacts were processed by evaporating a sequence of Ti/Pd/Ag (50 nm, 50 nm, 100 nm), and the rear side was processed by full-area evaporation of a 3 µm thick Al layer. Ag electroplating increased the thickness of the front contacts up to 10 – 20 µm. Finally, a double layer antireflection coating (DL-ARC) consisting of 50 – 60 nm TiO_2 and 105 nm MgF_2 was deposited, and the edges of the cell were isolated to prevent shunting.

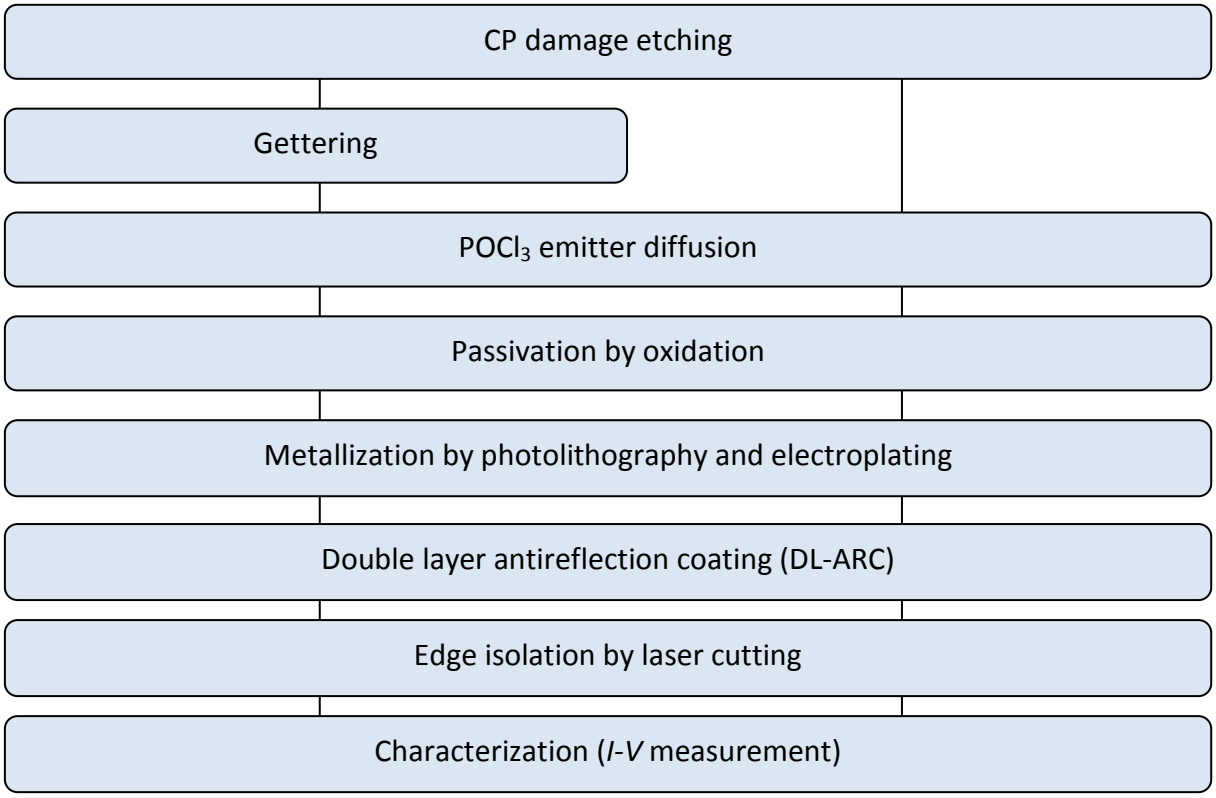

Fig. 2.4 Process steps used in this work for the standard wafer cell concept.

2.1.3 EpiWE cell concept

The epitaxial wafer equivalent (EpiWE) cell concept is based on a low-cost inactive silicon substrate and an epitaxially grown active thin silicon layer. The scheme is presented in Fig. 2.2 (b). “Epitaxial” literally means the growth of a layer on top (epi = “on top”) of the substrate with the same crystal orientation (taxis = “in ordered manner”) as the substrate. The term “wafer equivalent” implies that it can be treated like a standard silicon wafer and common industrial solar cell processes can be applied. This is one of the advantages of this simplest type of crystalline silicon thin-film (cSiTF) solar cells, which have the purpose of using less high-purity silicon in combination with a low-cost substrate. Another advantage is the possibility to apply emitter epitaxy [16-18], which is a very promising process (also for standard wafer based solar cells). By adding more or less P containing gases like PH_3 to the process gas, the emitter can be designed as desired, e.g., with a highly-doped peak at the surface for an improved contact formation. However, emitter epitaxy was not applied in this work. A challenge of the EpiWE cell concept is the relatively low current due to the thin active layer, where the light is absorbed and charge carriers are generated. The light should be trapped in the active layer to increase the carrier generation. The current can be

significantly improved by an optical confinement, including texturing of the surface and an intermediate layer between the substrate and the thin silicon layer, e.g., a porous silicon (PoSi) layer [19, 20] or a perforated silicon oxide layer, which is laterally overgrown by epitaxy [21].

The substrate of the EpiWE cell is a highly-doped low-cost silicon wafer made from MG or UMG silicon. In contrast to the standard wafer cell concept, where UMG wafers have to be lowly or at least moderately-doped to prevent recombination of generated carriers, high doping levels are even beneficial to the EpiWE cell concept to guarantee a proper conductivity in the inactive UMG substrate. The thin active layer consists of epitaxially grown p+ doped BSF and p-type base layers. The epitaxial deposition of the thin silicon layer is pursued by chemical vapor deposition (CVD) in atmospheric pressure chemical vapor deposition (APCVD) reactors, which were developed at the *Fraunhofer ISE* (see section 3.3.3). Principles and applications of CVD are described in general in [22, 23] and CVD of silicon in the context of the EpiWE concept in particular in [18, 24, 25]. In Fig. 2.5 a typical doping profile of EpiWE cells, which were processed in this work, is presented. Doping concentrations of about $5x10^{16}$ – $8x10^{16}$ cm^{-3} for the p-type base and up to 10^{18} cm^{-3} for the BSF were used. In this case p+ substrates with a doping level of around $3x10^{17}$ cm^{-3} and an applied PoSi layer on the substrate surface was used, which was processed in collaboration with the solar cell group at *IMEC* in Leuven. Typical thicknesses of the epitaxial base in this work were 20 – 35 µm. The epitaxial process was carried out at a temperature of about 1220°C.

After the epitaxial deposition of the BSF and the base, the emitter has to be applied to create the p-n junction. In principle, all kinds of emitters can be used for the EpiWE cell, an epitaxially grown emitter, a diffused emitter, and also an amorphous silicon emitter, which is called heterojuntion emitter. As the emitter formation by $POCl_3$ diffusion is a very common and reliable process, it was applied in this work to all solar cells, except for the heterojunction emitter structures which are presented in section 5.4.3.

If not otherwise indicated, all EpiWE cells in this work were processed with the process steps, which are presented in Fig. 2.6. It is a simplified clean-room cell process compared to the high efficiency clean-room process for standard wafer cells. The main difference is the 80 Ω/sq diffused emitter without oxide passivation and the direct evaporation of the front contacts through a shadow mask. This simplified cell process was used because low-cost substrates can result in whiskers (see section 5.4.1), which harm the photolithography masks. Furthermore, not high efficiencies were the main goal for most solar cell runs presented in this work, but rather the comparison of cells with and without gettering. After the $POCl_3$ emitter diffusion, the formed phosphosilicate glass (PSG) layer is etched-off and the rear side contact is formed by the evaporation of ~ 3 µm Al. The front side metallization

is done by direct evaporation of a sequence of Ti/Pd/Ag through a shadow mask. The thickness of the front grid is increased by silver plating subsequently. Finally, DL-ARC of 58 nm TiO_2 and 105 nm MgF_2 is applied and the edges of the cells are isolated by laser cutting.

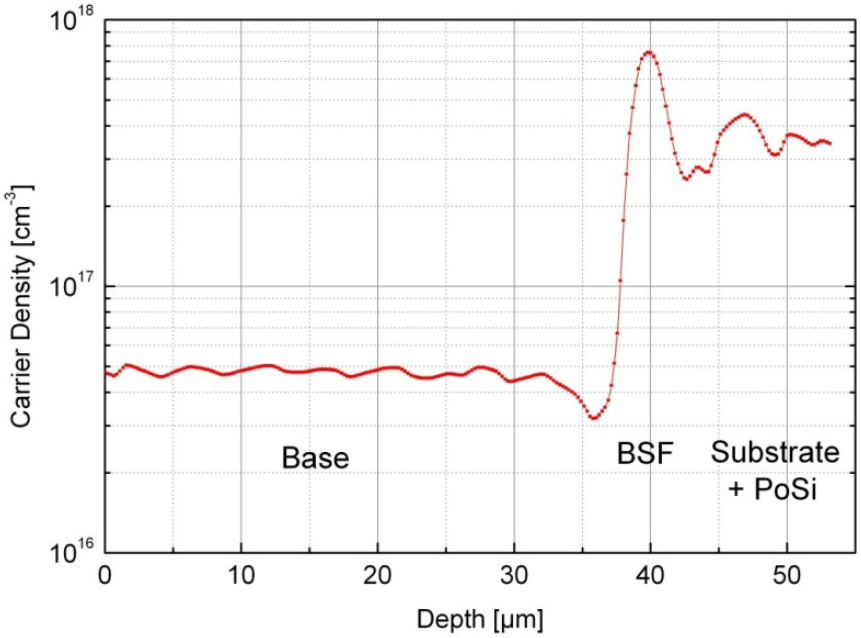

Fig. 2.5 Typical doping profile of a p+ UMG-Si substrate with porous Si layer (PoSi), epitaxially grown p+ back surface field (BSF) and p base, measured by spreading resistance profiling (SRP).

If not otherwise indicated, *I-V* measurements were done on lab equipment without certified quality control. If no uncertainties are given for *I-V* measurement results in this work, then the general uncertainty of measurement has to be considered, which are given for the following measured parameters as: V_{OC} ~ 0.5%; J_{SC} ~ 2.5%; *FF* ~ 1% (rel.). As the cell efficiency η_{cell} can be calculated after eq. (2-4), its uncertainty can be calculated by the propagation of uncertainty: η_{cell} ~ 2.9%. Most solar cell results presented in this work (see section 5.4) are given as average values obtained from several comparable cells.

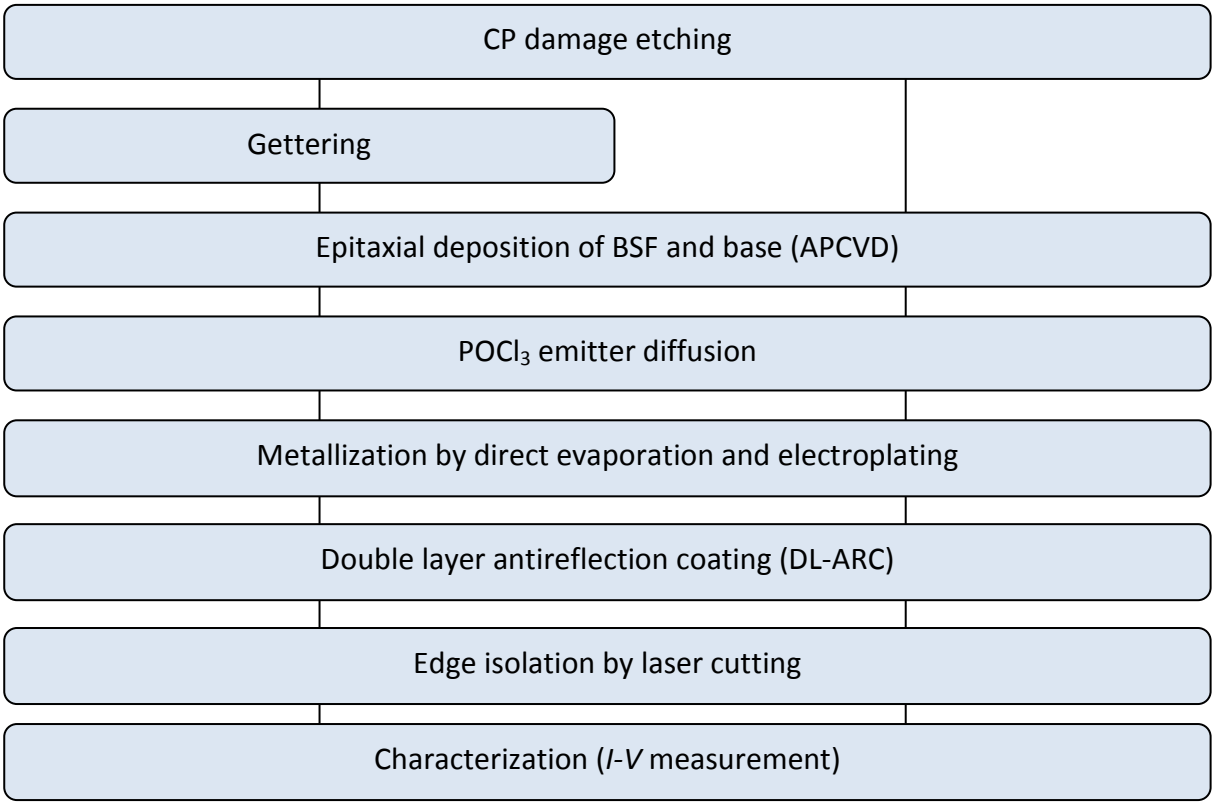

Fig. 2.6 Process steps used in this work for the EpiWE cell concept.

2.2 Characterization methods

2.2.1 Element analysis methods

The most relevant element analysis techniques, which were used in this work, are briefly introduced in this section. For detailed descriptions, the reader is referred to the references, which will be given in the respective sections. Note that all techniques are bulk analyses, which means the overall impurity concentration of the entire sample is determined.

Instrumental neutron activation analysis

Instrumental neutron activation analysis (INAA) is a technique to determine trace elements in various materials. It is based on the irradiation of the sample with neutrons, whereby radioactive nuclides are produced, and the measuring of emitted element characteristic radiation. With this bulk measurement method around 70 elements can be determined with a high sensitivity, independent from the actual chemical state of the elements. Fundamentals of INAA are described in details in the literature [26, 27]. Only some fundamentals of INAA concerning the detection of 3d transition metals in silicon and some process details of the performed INAA measurements are described herein.

$A(t_{irr})$ is the activity, which is produced after an irradiation time t_{irr}. It also depends on other parameters like the reaction cross section σ, the neutron flux Φ, the number of atoms N of the element, the abundance H of the isotope, and the half-life $t_{1/2}$, as described in eq. (2-7):

$$A(t_{irr}) = \sigma\ \Phi\ N\ H\ (1 - \exp(-\frac{\ln 2}{t_{\frac{1}{2}}}\ t_{irr}), \tag{2-7}$$

whereas the number of atoms N is described by Avogadro's constant N_A, the sample mass m, and the molar mass M as follows:

$$N = N_A \frac{m}{M}. \tag{2-8}$$

A neutron is captured by the nucleus and the produced radioactive nuclide decays by β decay, whereby the emitted γ radiation is measured by means of γ spectroscopy. The γ energy is characteristic for the specific elements. The amount can be determined by the γ-intensity, which is proportional to the number of atoms of the specific element in the sample. Although INAA is an absolute analysis technique, it is more practical to determine activities relatively to reference element samples with a well-defined element concentration.

Silicon is an ideal matrix for INAA, because it produces mainly short-lived nuclides. Table 2.2 shows the most relevant nuclear reactions with silicon. The only nuclide with a medium half-life of two and a half hour is ^{31}Si. But it is produced with a reaction cross section of only 0.1 b from the nuclide ^{30}Si, which has an abundance of only 3%. The other reactions are even less relevant, as they have much smaller reaction cross sections and/or occur with fast neutrons instead of thermal neutrons, and the flux of fast neutrons is much lower compared to the flux of thermal neutrons. However, the determination of elements, which are detected via short-lived nuclides (V and Ti), is influenced by the reactions with silicon and thus can only be achieved with much higher detection limits. The detection of Cu is limited by the low γ-intensity of ^{64}Cu. This is why V, Ti, and Cu were not determined by means of INAA. Mn was determined via ^{56}Mn, which has excellent properties in terms of INAA, thus can be detected with low detection limits, although the half-life of 155 minutes is similar to that of ^{31}Si. The long-lived nuclides ^{51}Cr, ^{59}Fe, ^{60}Co are also detectable with acceptable, in the case of Co excellent, detection limits when relatively long irradiation, decay, and measuring times are applied. Ni can only be determined via the (n,p) reaction to produce ^{58}Co.

The INAA measurements presented in this work were carried out at the *TRIGA Mark II* reactor at the Institute for Nuclear Chemistry, University of Mainz [28]. It is one of three still operational research reactors in Germany, where INAA measurements can be done, as there are also the *BER II* at the Helmholtz-Zentrum Berlin (HZB) and the *FRM II* of the Technical

University of Munich in Garching. The highest neutron flux at the *TRIGA Mainz* of $4.2x10^{12}$ cm^{-2} s^{-1} is achieved in the central experimental tube.

Table 2.2 Nuclear reactions of neutrons with silicon [29]. The reaction cross section of the $^{29}Si(n,p)^{29}Al$ reaction is taken from [30].

Stable nuclide	Isotopic abundance *H* [%]	Nuclear reaction	Reaction cross section σ [b]	γ energy [keV] (intensity [%])	Half-life $t_{1/2}$ [min]
^{30}Si	3	$(n,\gamma)^{31}Si$	0.1	1266 (0.07)	156
^{29}Si	4.7	$(n,p)^{29}Al$	0.0039 (from [30])	1273 (91)	6.5
^{28}Si	92.2	$(n,p)^{28}Al$	0.006	1779 (100)	2.2
^{30}Si	3	$(n,\alpha)^{27}Mg$	$1.5x10^{-4}$	844 (72) 1014 (28)	9.5

Achieved detection limits of INAA measurements at the *TRIGA Mainz* and the *FRM-II Garching* are summarized in Table 2.3. They depend not only on the characteristics (e.g., σ and *H*) of the nuclide, which is used for the determination, but also on the sample mass *m*, the neutron flux Φ, and the γ detector efficiency. Also crucial are the irradiation, the decay, and the measuring times, which should be selected depending on the half-life of the respective nuclide. This is why details about the above mentioned parameters are also given in the following. Values in [31] were obtained for a sample mass of around 700 mg, an irradiation time of 6 hours with a neutron flux of approximately $4x10^{12}$ cm^{-2} s^{-1}, a decay time of around 42 days, a measuring time of 12 hours with a detector efficiency of 72.6%. Values in [32] were obtained for a sample mass of around 200 mg, an irradiation time of 3 hours with a neutron flux of approximately $4x10^{12}$ cm^{-2} s^{-1}, a decay time of around 3 hours, a measuring time of 30 minutes with a detector efficiency of 27.7% for Mn, and for a sample mass of around 250 mg, an irradiation time of 90 hours with a neutron flux of approximately $1.1x10^{14}$ cm^{-2} s^{-1}, a decay time of around 21 days, a measuring time of 15 hours with a detector efficiency of 27.7% for Cr, Fe, Co, and Ni, respectively.

The sample preparation for INAA is simple. In contrast to other analysis techniques, where the silicon samples have to be dissolved for the measurement, only a surface cleaning step was applied to all samples prior to the INAA measurements in this work. The cleaning was done by a short dip in a HF/HNO_3 mixture actually removing around 1 µm of the surface. Therefore, the risk of contamination is much lower compared to ICP-OES or ICP-MS, where the silicon samples had to be dissolved before the measurement. Furthermore, INAA is applicable for materials, which are difficult to dissolve by chemical digestion. For example, the determination of transition metals in quartz material in section 3.3.4, which is used for

HCl gas gettering processes, was achieved by INAA, as silicon dioxide is an ideal matrix just as silicon.

Table 2.3 Detection limits of INAA measurements on Si at the *TRIGA Mainz* and the *FRM-II Garching*

Element	*TRIGA Mainz* [ng/g]	*FRM-II Garching* [ng/g]
Cr	6 [31]	0.43 [32]
Mn	0.85 [32]	Not determined
Fe	300 [31]	23 [32]
Co	0.6 [31]	0.05 [32]
Ni	20 [31]	400 [32]

There are several error sources which have to be taken into account to obtain the overall uncertainty of measurement: the error which occurs from different geometries of sample and reference element sample, the weighing errors of sample and reference element sample, and the error of the γ spectroscopy counting statistics. The overall uncertainty of measurement for every sample was calculated by the propagation of uncertainty from the above mentioned single errors.

It can be concluded that INAA is generally well-suited for the detection of transition metals in silicon. A large range of transition metal concentrations can be detected in various silicon materials, from less than ng/g to mg/g. V, Cr, Mn, Fe, and Co were determined in MG silicon in this work with sufficient detection limits. Furthermore, the As profile of a whole silicon ingot made from UMG silicon feedstock was measured and is presented in section 4.1.

Prompt gamma activation analysis

Prompt gamma activation analysis (PGAA) was used to determine B concentrations in UMG silicon, which is presented in section 4.1. The principle of PGAA is similar to INAA with the difference that prompt gamma rays, which are emitted immediately after the absorption of a neutron, are detected. This means that the spectroscopy has to be done simultaneously to the irradiation. The sensitivity of PGAA is lower compared to INAA. However, the B concentration in the UMG samples were above 1 ppmw, and could therefore be easily determined. The measurements were performed at the PGAA facility of the high flux reactor (HFR) in Petten, Netherlands. Details about the analysis method and facilities of PGAA in Petten and also at the *FRM-II* in Garching are given in [33-35].

Inductively coupled plasma optical emission spectroscopy

Inductively coupled plasma optical emission spectroscopy (ICP-OES), sometimes also called atomic emission spectroscopy (AES), was used to determine Ti, Cr, Mn, Fe, Co, Ni, and Cu in MG and UMG silicon in this work. The inductively coupled plasma, generally based on Ar, is used for the decomposition of molecules to excited atoms and ions, which during relaxation emits electromagnetic radiation with element characteristic wavelengths. The intensity is proportional to the concentration of the respective element in the sample. ICP-OES is an easy-to-use multi-element method allowing the simultaneous detection of several elements. It is a relative technique and has to be calibrated by element standards. ICP-OES can be limited by spectral interferences. A detailed description of ICP-OES can be found in [36]. Besides INAA it was applied for most analyses in this work.
The sample preparation was done, applying the same wet-chemical treatment as used for INAA measurement. A short dip in a HF/HNO_3 mixture removed about 1 µm of the sample surface. In the next step, the samples were completely dissolved in HF/HNO_3. To achieve better detection limits the sample solutions were subsequently evaporated using a microwave system and finally measured in a small volume of diluted HNO_3.

Inductively coupled plasma mass spectrometry

Inductively coupled plasma mass spectrometry (ICP-MS) uses the same excitation method, the inductively coupled plasma, to produce ions, which are accelerated into a mass spectrometer, where they are separated by their mass/charge ratio and finally are detected. The concentration of a sample can be determined by the calibration with certified reference materials such as single or multi-element reference standards. ICP-MS is also a multi-element method. It offers an extremely high sensitivity to a wide range of elements with generally better detection limits than ICP-OES. However, ICP-MS can also be limited by interferences, which can occur with the matrix elements or other molecular species. Detailed descriptions of the techniques can be found in [37]. The sample preparation was done in the same way as described for ICP-OES. ICP-MS was only used for one analysis in this work, as the equipment was rarely available.

Graphite furnace atomic absorption spectroscopy

Graphite furnace atomic absorption spectroscopy (GF-AAS) is based on the absorption of light in the evaporated solvent containing the atomized analyte element, which is measured by a detector. The evaporation and atomization is done using a flame (F-AAS) or an electrically heated graphite tube (GF-AAS). GF-AAS has a much better detection limit than F-AAS. It has similar or even lower detections limits for most transition metals compared to ICP-MS. However, its analysis time is relatively long and it is a mono-element method, since element-

specific hollow cathode lamps are used as light sources. Thus GF-AAS was applied in this work only in the case of the ICP-OES detection limit being not sufficient. The sample preparation was done in the same way as described for ICP-OES and ICP-MS.

2.2.2 Minority carrier lifetime characterization methods

In this section, the minority carrier lifetime is briefly introduced, followed by the lifetime measurement methods, which were applied in this work.

The minority carrier lifetime is the average time it takes for excess charge carriers, electrons or holes, to recombine. Higher lifetime values mean a higher electrical quality of the silicon and tend to result in a higher solar cell efficiency. In p-type silicon, the minority carrier lifetime τ is defined by the excess electron density Δn, and the bulk recombination rate U [38]:

$$\tau = \frac{\Delta n}{U} = \left(\frac{1}{\tau_{\mathrm{rad}}} + \frac{1}{\tau_{\mathrm{Aug}}} + \frac{1}{\tau_{\mathrm{SRH}}} + \frac{1}{\tau_{\mathrm{surf}}}\right)^{-1}. \tag{2-9}$$

The excess charge carriers, which are produced by photogeneration in the silicon, can recombine through different mechanisms: radiative recombination, Auger recombination, Shockley-Read-Hall (SRH) recombination, and surface recombination. The respective lifetimes, the radiative recombination lifetime τ_{rad}, the Auger recombination lifetime τ_{Aug}, the SRH recombination lifetime τ_{SRH}, and the surface recombination lifetime τ_{surf}, contribute to the effective lifetime τ, that is measured, as presented in eq. (2-9). Radiative recombination is a mechanism, whereby an electron and a hole recombine and its energy is emitted as light. This process is the inverse process of the generation of an electron-hole pair. However, this mechanism has only a low probability in silicon. Furthermore, Auger recombination can occur, whereby an electron and a hole recombine and the energy is transferred to a second electron or hole which relaxes by emitting phonons. It is only significant for doping levels higher than $10^{17}\,\mathrm{cm}^{-3}$ in silicon. SRH recombination is a mechanism due to deep level metal impurities in the silicon band gap. The recombination at the silicon surfaces is similar to the SRH mechanism, as dangling bonds on the silicon surface lead to defect levels in the band gap. By applying surface passivation layers such as silicon nitride or oxide layers, the surface recombination rate can be decreased, and τ_{surf} is thus sufficiently high. Since for all lifetime measurements in this work, surface passivation was applied, and high transition metal levels are present in most investigated silicon materials, the dominant mechanism, which is limiting the minority carrier lifetime, is SRH recombination through transition metal impurities. The lifetime is supposed to increase by the application of gettering methods.

Quasi-steady-state photoconductance

The quasi-steady-state photoconductance (QSSPC) measurement method is used for the determination of the minority carrier lifetime. The excess charge carriers in the silicon sample are generated by a Xe flash light. It should be assured that the decay rate of the flash light is considerably larger than the minority carrier lifetime to have a quasi-steady-state condition of the charge carriers. In this state, the generation rate *G* of carriers equals the recombination rate *R*. A coil of a calibrated radio-frequency (RF) bridge, which is inductively coupled to the sample (see Fig. 2.7), is used to measure the excess photoconductivity of the sample. The illumination intensity is monitored by a reference solar cell, which is illuminated simultaneously. From these data, the effective lifetime τ can be obtained:

$$\tau = \frac{\Delta n}{G}, \tag{2-10}$$

where Δn denotes the excess electron density, and *G* denotes the generation rate. Δn is obtained from the change in photoconductivity, and *G* is obtained from the illumination intensity. Detailed descriptions of the QSSPC technique can be found in [39, 40].

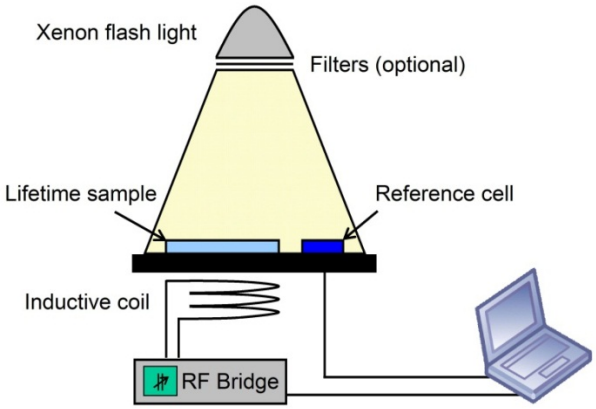

Fig. 2.7 Scheme of the quasi-steady-state photoconductance (QSSPC) measurement setup (from [41]).

Quasi-steady-state photoluminescence calibrated Photoluminescence imaging

The method of the quasi-steady-state photoluminescence (QSSPL) calibrated photoluminescence imaging (PLI) can also be used to determine the minority carrier lifetime in silicon wafers. In contrast to the QSSPC measurement method, where an average lifetime is obtained on an area of several cm^2, by QSSPL calibrated PLI space-resolved lifetime maps of wafers in a spatial resolution of typically 100x100 μm^2 can be obtained.

Photoluminescence (PL) means the optical excitation (generation of excess carriers by incident light) and the radiative recombination of electron-hole pairs (by emitting photons). The minority carrier lifetime is again obtained by using eq. (2-10). In contrast to the QSSPC method, Δn is obtained from the PL data. Although radiative recombination in silicon has a low probability compared to non-radiative recombination mechanisms, PL can be detected via a measurement setup, which is described in the following.

PLI in this work was done using a laser as excitation source. As detector a charge coupled device (CCD) camera was applied, which was placed relative to the laser such that the laser light reflected from the sample cannot directly enter into the detector, as presented in Fig. 2.8. The detection of irradiation intensity is prevented by an optical long-pass filter. Detailed descriptions of the PLI technique can be found in [42].

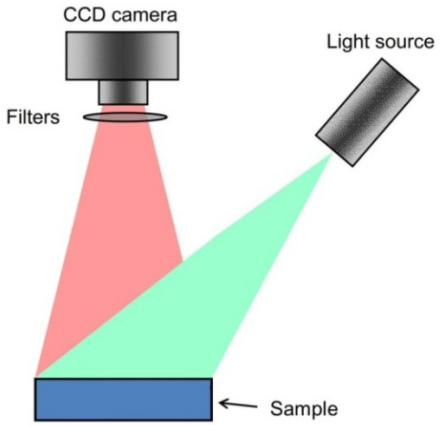

Fig. 2.8 Scheme of the photoluminescence imaging (PLI) measurement setup (from [41]).

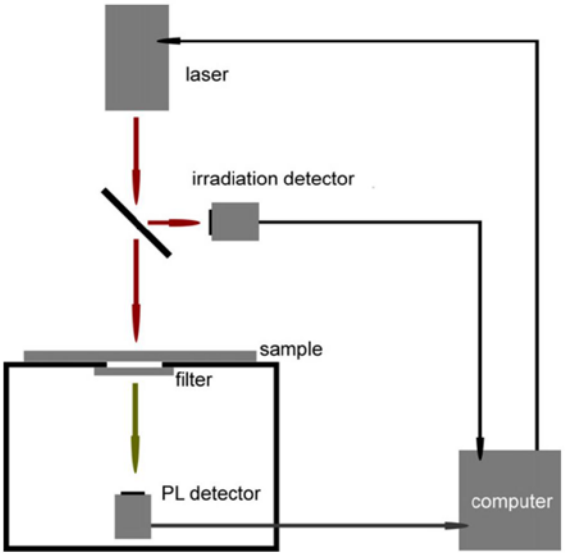

Fig. 2.9 Scheme of the quasi-steady-state photoluminescence (QSSPL) measurement setup (from [43]).

In the QSSPL measurement setup (see Fig. 2.9), the light intensity of the laser light source is measured by an irradiation detector by using a beam splitter. The PL of a silicon sample is measured by a PL detector, which is shielded from the laser irradiation by both the sample and long pass filters. Irradiation and PL signals can be amplified and simultaneously read into a computer. The active measurement area of the QSSPL measurement is approx. 16 cm^2 in the middle of the sample. The averaging procedure derived in [43] enables a lifetime calibration by adequately relating the locally measured PL intensities within the active area to a QSSPL lifetime.

2.2.3 Solar cell characterization methods

Electroluminescence

Electroluminescence (EL) is the emission of light due to radiative recombination of electron-hole pairs, but in contrast to PL, the excess carriers are caused by an injection of excess carriers, for example by applying a forward bias [44]. To apply a voltage, electrical contacts are required. This is why EL can only be applied to finished solar cells, in contrast to PL measurements, which can also be done on silicon wafers without metallization. It means that during the EL measurement, the solar cell in principle acts as a light emitting diode, even though very inefficiently. The emitted light is detected by a CCD camera. An EL image of the solar cell is obtained. The emission intensity depends on the density of defects in the silicon. In areas where a high defect density is present in the silicon solar cell, non-radiative recombination mechanisms dominate, leading to darker areas in the respective EL image. For all EL measurements shown in this work, a forward bias of 600 mV was applied to the cells. EL images were used for qualitative analysis purposes.

Internal quantum efficiency

The external quantum efficiency (EQE) is the ratio of the number of charge carriers collected by the solar cell and the number of incident photons [12]. As reflection of the incident light can occur at the surface of the cell, it is taken into account in the internal quantum efficiency (IQE). Thus, the IQE is the ratio of the number of carriers collected and the number of photons, which have not been reflected but actually have entered the cell. To obtain IQE curves, which are shown in this work, the current density of the solar cell is measured in dependence of the wavelength of the incident light. If the wavelength dependent reflection $R(\lambda)$ is measured as well, the $IQE(\lambda)$ can be calculated from the $EQE(\lambda)$ as follows:

$$IQE(\lambda) = \frac{EQE(\lambda)}{1 - R(\lambda)}. \tag{2-11}$$

3 Fundamentals of HCl gas gettering in silicon

In this chapter, the principle reactions of HCl gas with silicon (HCl etching) and with transition metals in the silicon (HCl gas gettering) are described. Furthermore, the reactor is briefly presented, which was used for most HCl gas gettering processes. In the first part, the most relevant properties of transition metals in silicon regarding HCl gas gettering are described. As etching of silicon occurs during HCl gas gettering at high temperatures, the etching reaction is described in general, and investigated for MG and UMG silicon, in particular in the second part. In the third part, the basic mechanism of HCl gas gettering is discussed with emphasis on the limiting process steps, and the reactor is introduced followed by the consideration of contamination sources during gettering processes.

3.1 Transition metals in silicon

Transition metals are common impurities in silicon. Mainly 3d transition metals like Cr, Mn, Fe, Co, Ni, Cu, are described as they are prominent impurities in silicon and can be detrimental for silicon solar cells. Transition metals are already present in the quartz, the material, which silicon is manufactured from. But they are also contaminants, which are brought into the silicon during all steps of the technological process in silicon application industry. For example, Fe can be a contamination source for silicon material during heat treatment. It is very difficult to do heat treatment experiments without contamination [45]. Studies on the solubility of 3d transition metals were already presented since the early sixties [29, 46], and an overview on properties like the diffusion, solubility, and electrical activity of 3d transition metals in silicon was given in [47]. The diffusion is further described, as it plays an important role during gettering in silicon. Moreover, the distribution of transition metals in silicon, the impact on the solar cell performance, and definitions of the different types of silicon material are discussed.

3.1.1 Diffusion

The dominant diffusion mechanism for the 3d elements Cr, Mn, Fe, Co, Ni, and Cu in silicon is the interstitial diffusion [47]. The diffusivity D of transition metal impurities in intrinsic monocrystalline silicon is given by

$$D = D_0 \, e^{-\frac{H_M}{k_B T}} . \tag{3-1}$$

D_0 is referred to as the maximum diffusion coefficient (at infinite temperature), H_M is referred to as the migration enthalpy. k_B is the Boltzmann constant and *T* is the temperature. Data for D_0 and H_M of 3d transition metals were taken from [47] and [48] for all calculations, which were done in this work, e.g., for the simulations of chapter 6. The diffusion length L of a transition metal in silicon depends on the diffusivity D and the diffusion time t, as follows:

$$L = \sqrt{D \, t} . \tag{3-2}$$

Some transition metals, e.g., Zn, Pt, and Au, are dissolved predominantly on substitutional sites and diffuse via a more complex mechanism (kick-out mechanism). Since in this work, only transition metals are investigated, which diffuse interstitially, it is only mentioned and referred to [4, 49] for a detailed description.

3.1.2 Distribution

It was found in different types of mc silicon that the minority carrier diffusion length was much better than expected from the metal content measured by INAA [50]. It was concluded that the metals must be inhomogeneously distributed within the samples as precipitates or agglomerates. Due to a strong temperature dependence of their solubility in silicon, transition metals become supersaturated even at relatively low concentrations during cooling after a temperature process, e.g., crystallization, and may form nanoprecipitates. The precipitates are mainly located at extended defects like dislocations and grain boundaries, which are present in mc silicon in a much higher density than in monocrystalline silicon. Synchrotron-based measurements [51] were performed in [52] to detect the spatial and size distributions of metal defects in commercial mc silicon made by directional solidification. The nanoprecipitates have a radius of about 20 – 30 nm and contain about $10^6 – 10^7$ metal atoms each. The precipitates are present in the sample with a density of about 10^8 cm^{-3}. Also another type of metal-rich particles was detected, which were found to be composed of metal oxides. They are inclusions in the average size of several micrometers each containing about $10^{12} – 10^{14}$ atoms and are present in a density of $10^4 – 10^6$ cm^{-3}. Since the silicon-oxygen bond is stronger than most metal-oxygen bonds [53], and the particles are

too large to have formed from precipitated impurities, it was concluded that these metal-oxide species with melting temperatures significantly above that of silicon had already existed during melting and were trapped during crystallization of the silicon. The composition was found to be either similar to that of stainless steel or Fe oxide or Ti oxide. The contaminants had probably already been in the feedstock or were introduced during crystal growth coming from the furnace parts. Partial dissolution of such particles in the molten silicon during crystal growth may be the reason in general, when high metal concentrations are found in mc silicon. Beside the nanoprecipitates and the described inclusions, metals were also found in interstitial sites as dissolved metal point defects in a density of about 10^{13} cm^{-3}. It was also reported that co-precipitation of multiple-metal species is found in silicon and it was reported that the precipitation formed during annealing and cooling from high temperatures (≥ 1200°C) are much more difficult to explain with precipitation models than precipitation at lower temperatures [54].

The distribution of metallic impurities was recently also investigated in UMG silicon. A study is reported in [55], where UMG silicon feedstock was measured by synchrotron-based scanning X-ray fluorescence microspectroscopy. Large particles with sizes between 5 µm and 60 µm containing several transition metals were found predominantly located at grain boundaries. For example, Fe-rich particles were found, which also contained Mn, Cu, Ni, and Zn. Cu was also found almost uniformly distributed across the sample with higher concentrations than the background noise and with even higher concentrations in large hazes which were not aligned to grain boundaries. Such a uniform distribution of Cu was not expected since Cu is a fast diffusor in silicon and should be accumulated at grain boundaries during cooling. This is an indication for intra-grain defects like dislocations, which act as effective precipitation sites for Cu. However, the above mentioned investigations were done on feedstock material before the crystallization step. After crystallization, the distribution of Cu can be different. This is actually indicated by the results of another report, where all Cu impurities were found in various types of directionally-solidified mc silicon wafers as precipitates in the grain boundaries [56].

3.1.3 Impact on solar cells

Transition metals are detrimental for silicon solar cells because they form deep levels in the silicon band gap. Fig. 3.1 shows energy levels of 3d transition metals. The charge carriers (electron-hole pairs), which are produced by photogeneration in a solar cell, can recombine at recombination centers formed by metal impurities before they reach the cell junction and thus cannot contribute to the current of the solar cell. The minority carrier lifetime and therefore the cell efficiency are reduced. The recombination mechanism due to deep level metal impurities is known as Shockley-Read-Hall (SRH) recombination [57, 58]. There are

also other recombination mechanisms present in silicon which can limit the minority carrier lifetime, such as radiative recombination, whereby an electron and a hole recombine and its energy is emitted as light. This process is the inverse process of the generation of an electron-hole pair. However, this mechanism has only a low probability in silicon. Furthermore, Auger recombination can occur, whereby an electron and a hole recombine and the energy is transferred to a second electron or hole which relaxes by emitting phonons. It is only significant for doping levels higher than 10^{17} cm^{-3} in the case of silicon solar cells. The recombination at the silicon surfaces can also limit the minority carrier lifetime, which can be prevented by applying surface passivation layers such as silicon nitride or oxide layers. The overall lifetime is limited by a combination of all mentioned recombination mechanisms. High impurity levels are present in most silicon materials used in this work, and the dominant mechanism therefore is the SRH recombination through impurities and crystal defects.

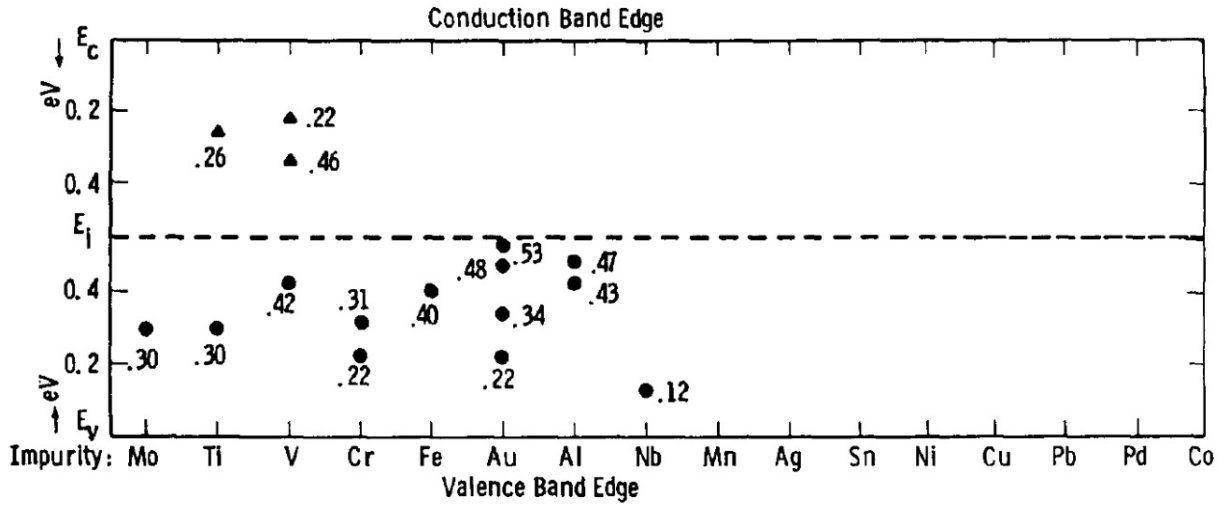

Fig. 3.1 Measured deep levels for impurities, mainly transition metals, grown into monocrystalline silicon [59].

Fig. 3.2 presents how strong the solar cell efficiency is affected by various metals, depending on the metal concentration. According to this, for example, already concentrations of Ti or V below ppba[3] significantly degrade the cell efficiency. It has to be noted that this is only valid in monocrystalline silicon. Furthermore, the presented degradation is given for solar cells with a p-type base. It was found that n-type based solar cells are generally less affected by most impurities than p-type based cells [60]. Thus research was done on n-type solar cells,

[3] ppba = parts per billion atoms

but today, most silicon suppliers only offer boron-doped silicon and most solar cell concepts are still based on p-type silicon. One reason is the segregation coefficient of B (0.8)[4], which is closer to 1 than that of P (0.35)[4], thus leading to a higher yield of silicon with appropriate resistivity after ingot crystallization.

It was shown by Istratov et al., that in multicrystalline silicon not only the total metal concentration is relevant for the impact of metals on the solar cell efficiency but also the distribution and the chemical state of the metals [50]. Defects such as grain boundaries or dislocations are thought to be weak recombination centers when they are clean [61, 62]. However, it is very unlikely to find a clean dislocation in mc-Si since dislocations are efficient gettering sites which collect metal impurities thus becoming efficient recombination centers [8]. Metal precipitates and clusters are also recombination active but can act as a kind of inactive storage for metals because only metal atoms near the surface of such clusters are influencing the recombination properties [63]. This is why precipitation is preferable in case the metals cannot be removed completely. External gettering techniques are used to remove metals from the silicon. Gettering in general and HCl gas gettering in particular will be described in section 3.3.

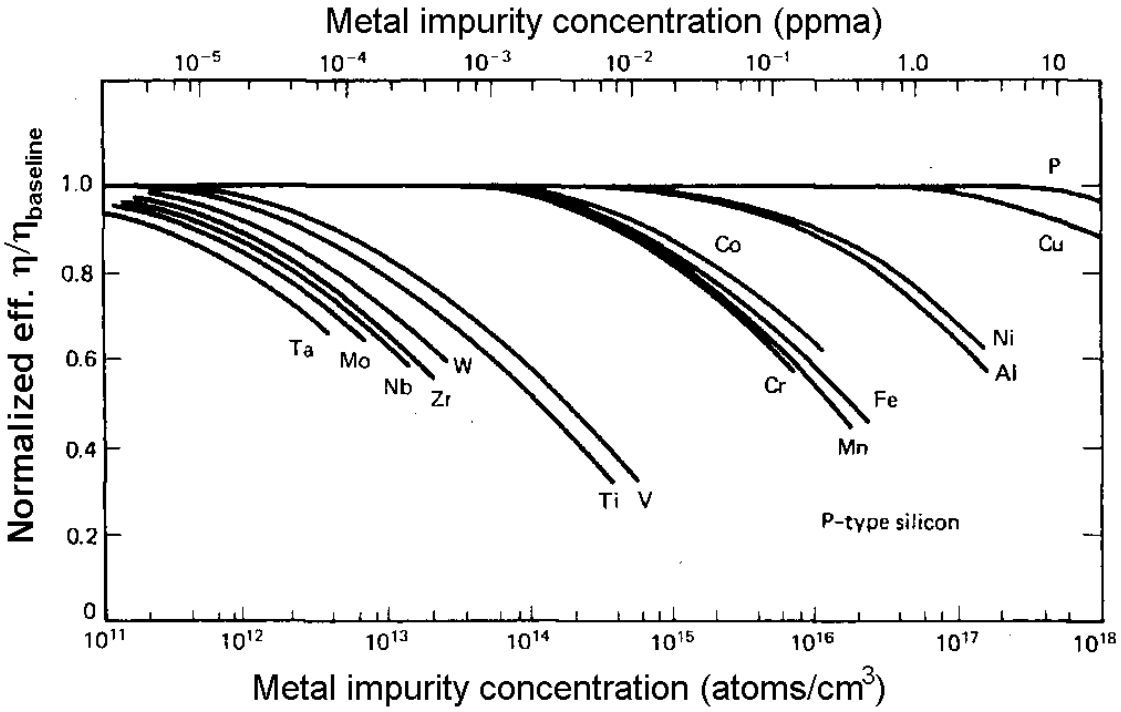

Fig. 3.2 Impact of impurities, mainly transition metals, on the performance of p-type monocrystalline silicon solar cells [64].

Istratov et al. reported that the recombination properties of metals vary in a wide range depending on their chemical or structural state and suggested that metals do not have to be

necessarily removed but can be converted to a less recombination active state to minimize their impact on the solar cell performance [50]. They proposed the term 'metal passivation through defect engineering'. Although further studies on this topic have been done [52, 54, 65, 66], still today the understanding of the chemical states of metals in mc silicon, especially in highly contaminated silicon, and also appropriate defect reactions to convert the metals into a desired state, is rather poor.

In EpiWE solar cells, transition metals have an impact on the solar cell performance only if they are present in the epitaxially grown active layer. Metals in the silicon substrate in principle are not detrimental. However, they already diffuse into the active silicon layer during the high-temperature epitaxial deposition process. Thus moderately and fast diffusing impurities are present nearly with the same concentrations in the epitaxial layer as in the substrate [67, 68]. An intermediate layer, which is intended for an optical confinement, e.g., a porous silicon (PoSi) layer or a perforated silicon oxide layer, would act as a diffusion barrier simultaneously. It could prevent transition metals from diffusing into the epitaxial layer more or less effective [69]. But since it could not stop diffusion of transition metals completely, and since low-cost silicon can contain extremely high metal concentrations, gettering is still considered to be a crucial step in the EpiWE cell concept.

3.2 HCl gas etching of silicon

3.2.1 Reaction mechanism

It is known that HCl gas reacts with silicon at elevated temperatures. The silicon is etched by the formation of volatile silicon chloride species like $SiHCl_3$ and $SiCl_4$. HCl etching at high temperatures (1200°C) is known from the microelectronic industry as a standard surface cleaning process. The overall reaction, which is also a basic reaction in the Siemens process, is simply described by the equation

$$Si + 3HCl \rightleftharpoons SiHCl_3 + H_2 \,, \tag{3-3}$$

whereas the reaction mechanism is assumed to be as shown in Fig. 3.3 [70-72]. In the left scheme (a), the partial reactions are described with their reactants, products, and side products. The epitaxy reactions are also described which are in competition with the etching. The right scheme (b) illustrates the transport phenomena of the reactant HCl to the surface and depicts where the reactions take place. At first, the partial dominant reactions in Fig. 3.3 (a) shall be described, which are:

$$Si + HCl \rightarrow {}^*SiCl + \frac{1}{2}H_2 \uparrow \,, \tag{3-4}$$

$$*SiCl + HCl \rightarrow *SiCl_2 + \frac{1}{2}H_2 \uparrow , \tag{3-5}$$

$$*SiCl_2 + HCl \rightarrow SiHCl_3 \uparrow . \tag{3-6}$$

The asterisk (*) indicate a chemisorbed state. For increasing HCl concentrations, trichlorosilane ($SiHCl_3$) can further react to silicon tetrachloride ($SiCl_4$) in the gas phase:

$$SiHCl_3 + HCl \rightleftharpoons SiCl_4 + H_2 . \tag{3-7}$$

In competition to the etching process, the reactions leading to silicon epitaxy are:

$$SiHCl_3 \rightarrow *SiCl_2 + HCl , \tag{3-8}$$

$$*SiCl_2 + H_2 \rightarrow Si + 2HCl \uparrow . \tag{3-9}$$

Equation (3-8) can be considered as reverse reaction of eq. (3-6), whereas eq. (3-9) is the summarized reverse reaction of (3-4) and (3-5). These reverse reactions are suppressed for the HCl gettering processes as there is an excess of the HCl concentration compared to the $SiHCl_3$ concentration.

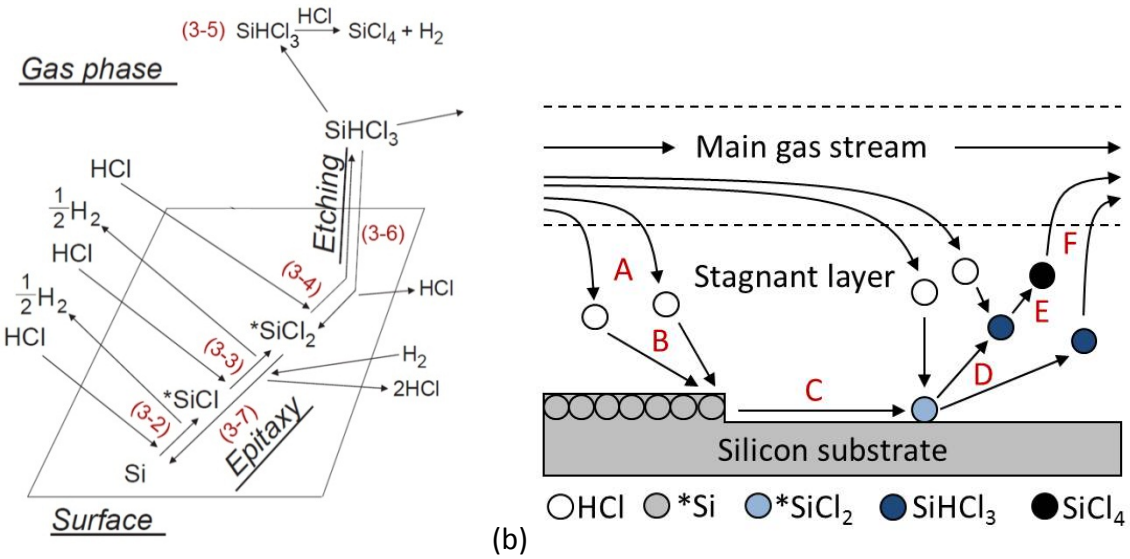

Fig. 3.3 Mechanism of HCl etching of silicon with emphasis on the partial reactions including epitaxy reactions (a) [70], and with emphasis on transport phenomena and reaction types of the process steps during etching (b).

In Fig. 3.3 (b) the main process steps are described, which are the HCl gas diffusion from the main gas stream into the stagnant boundary layer [73] and onto the silicon surface (A), the

chemisorption of HCl at the silicon surface (B), the surface diffusion of $*SiCl_2$ (C), the desorption of produced $SiHCl_3$ into the gas phase (D), the gas phase reaction to $SiCl_4$ (E) in the presence of HCl excess, and the gas diffusion of the main products $SiHCl_3$ and $SiCl_4$ (F) into the main gas stream.

It was shown that HCl gas remains the dominant species in the gas phase [74], and although it was proposed from equilibrium calculations by [75], that $SiCl_2$ is the dominant silicon-containing species in the gas phase, it was shown from experiments, that $SiHCl_3$ and $SiCl_4$ are dominating [70]. The fact that the $SiCl_4$ fraction is increased with an increasing HCl concentration can be confirmed with experimental data obtained by exhaust gas composition analysis by means of FT-IR. Fig. 3.4 shows an example of the increase of the $SiCl_4$ concentration due to an increasing HCl input concentration in ambient H_2.

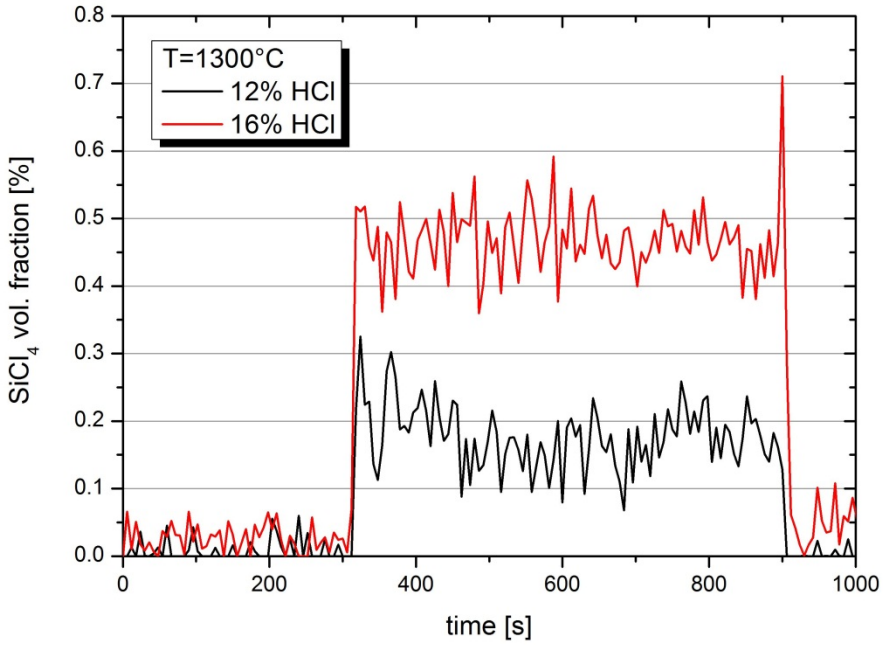

Fig. 3.4 Increasing silicon tetrachloride ($SiCl_4$) volume fraction with increasing HCl input concentration measured by FT-IR.

3.2.2 Etching rate and reaction kinetics

The dominant rate process was studied by Habuka et al. [70] by etching experiments between 750 – 1150°C and numerical calculation which included the transport phenomena in the entire reactor and the chemical reaction at the silicon surface. It was concluded that the dominant process is a first-order successive reaction at the silicon surface with an activation energy of $1.5x10^5$ $Jmol^{-1}$. This was confirmed by [76], who detected $SiHCl_3$ and

$SiCl_4$ as dominant etch products. Furthermore, a linear relation between the etching rate and the HCl gas concentration at least for concentrations above 4% was reported by [77]. Several earlier studies, e.g., by van der Putte et al. [74], who reported an activation energy of $1.7x10^4$ $Jmol^{-1}$, proposed a second order chemical reaction to produce $SiCl_2$, based on the nonlinear behavior of the etching rate at low HCl concentrations and based on the equilibrium theory [71, 72, 78]. However, these studies only considered the surface reaction. In contrast, Habuka et al. were taking into account the transport phenomena, like the diffusion fluxes of all chemical species driven by the concentration and temperature gradients in the reactor, by using two- and three-dimensional numerical calculations.

The etching rate R_{etch} and the reaction kinetics shall be investigated in the following including the result of this work. R_{etch} can experientially be obtained by weighting the silicon wafer before and after the etching. It can be calculated from the difference in weight and parameters like the silicon density and the wafer area. Therefore, R_{etch} is an average value over the whole silicon wafer. If the dominant process was a first-order reaction referring to HCl, the following relation should be valid for all HCl concentration regions:

$$R_{etch} \propto c_{HCl} \,. \tag{3-10}$$

The dependence of the R_{etch} on the HCl concentration as predicted from eq. (3-10) was investigated by etching experiments with both MG and UMG silicon wafers at 1300°C for different HCl concentrations between 2% and 20% for a process time of 10 minutes. The measured etching rates plotted against the HCl concentration can be seen in Fig. 3.5. The linear dependence of R_{etch} on the HCl concentration is confirmed for both MG and UMG silicon. No deviation from the linearity can be identified for HCl concentrations below 4%. Although few data are obtained in the low concentration region, this supports the assumption of a first-order reaction type.

It is noticeable that the etching rate is higher for all HCl concentrations in the case of MG silicon. This leads to the conclusion that the different silicon materials have to be examined separately, when considering the reaction mechanism of silicon etching by HCl gas. The difference in the etching rates of MG and UMG silicon might have its origin in the higher number and greater size of metal clusters in MG, as compared to most UMG silicon materials. These clusters are preferentially etched during HCl processes and therefore the etching rate might be increasing. This phenomenon leads to macroscopic holes in the wafer, especially for high HCl concentrations or for long process times, as can be seen in Fig. 3.6 (a). An example of a cluster at the silicon surface is presented in Fig. 3.6 (b). It was prepared by wet-chemical CP etching (HF/HNO_3), as metal clusters are not etched, while the surrounding silicon is etched by CP [18]. The possible range of the optimum gettering parameters

(temperature, time, HCl concentration) for MG silicon is therefore limited, as no solar cells can be processed on such substrates with macroscopic holes.

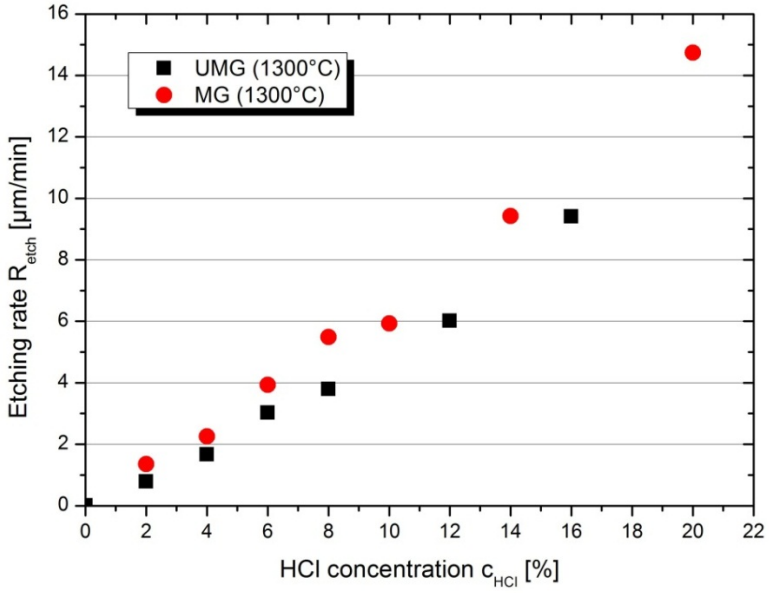

Fig. 3.5 Etching rate depending on the HCl concentration.

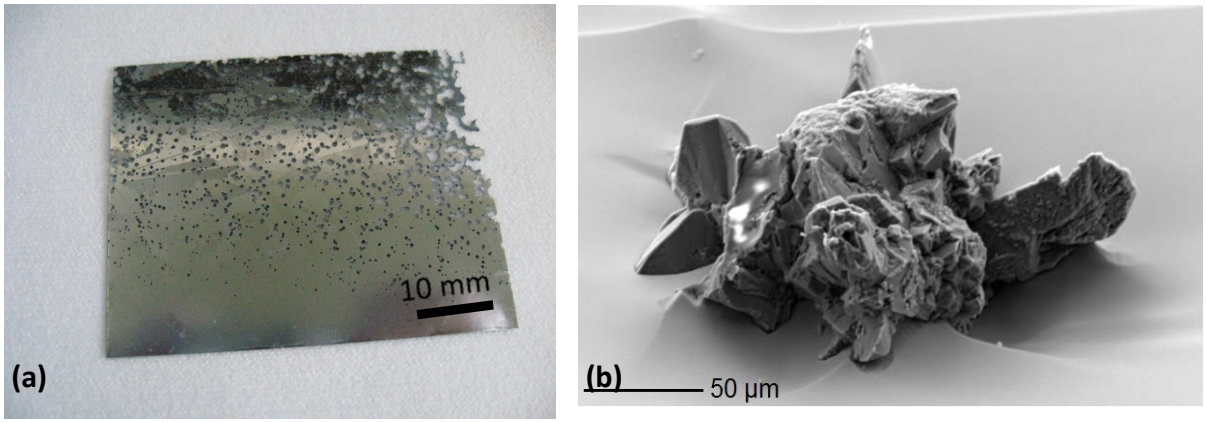

Fig. 3.6 MG silicon wafer after HCl gas gettering with 2% HCl in H_2 for a long gettering time (> 120 min), resulting in macroscopic holes (a), which are caused by the preferential HCl etching of metal clusters. An example of a metal cluster is presented in (b), which was prepared by wet-chemical etching of another MG silicon wafer [18].

The overall rate constant *k* of the etching process depending on the etching rate R_{etch} can be calculated as follows [70], assuming that the dominant process is a first-order successive reaction at the silicon surface:

$$k = \frac{R_{etch}\,\rho_{Si}}{M_{Si}\,c_{HCl}}, \tag{3-11}$$

whereby ρ_{Si} denotes the density of silicon, M_{Si} the molecular weight of silicon, and c_{HCl} the HCl concentration. With the Arrhenius equation,

$$k = A\, e^{\frac{-E_A}{RT}}, \tag{3-12}$$

whereby A is the pre-exponential factor, E_A is the activation energy, R is the universal gas constant, and T is the temperature, the following relation between the etching rate R_{etch} and the temperature T can be derived:

$$R_{etch} \propto e^{-\frac{1}{T}}. \tag{3-13}$$

Thus, a linear correlation is expected from a logarithmic plotting of R_{etch} versus the reciprocal temperature T. Instead of plotting ln(R_{etch}) with a linear scale, R_{etch} with a logarithmic scale leads to the same plot in terms of the curve characteristics and slopes and has the advantage that concrete values of the etching rate can be deduced from the plot directly.

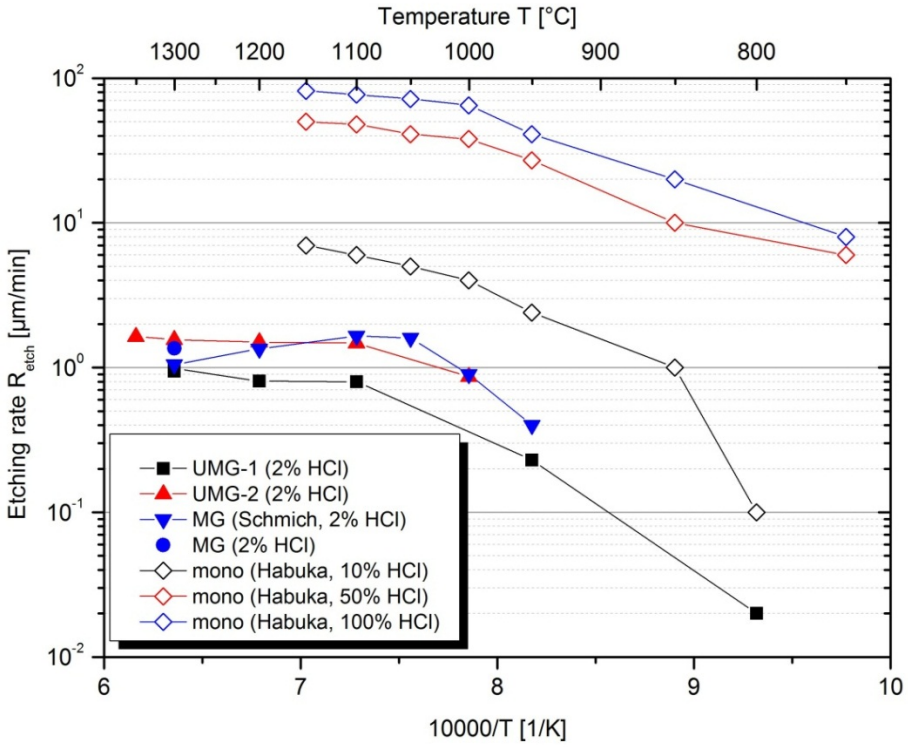

Fig. 3.7 Etching rate (logarithmic scale) versus the reciprocal temperature (Arrhenius plot).

Values for R_{etch} were obtained by etching experiments with neighboring UMG silicon wafers at different temperatures for a concentration of 2% HCl in H_2. In Fig. 3.7 the Arrhenius plot is presented, including data for MG silicon from Schmich [18], and data for monocrystalline

silicon at higher HCl concentrations from Habuka [70]. Regarding the data of UMG and MG silicon, two regions can be noticed obviously. In the low-temperature region (≤ 1050°C), a linear relation with a strong decrease is visible, whereas in the high-temperature region (≥ 1050°C) only little dependence of the etching rate on the temperature is noticeable. It is proposed that the etching rate is limited due to mass transport phenomena in the high-temperature region, as it is known from the silicon chemical vapor deposition (CVD) growth kinetics [22, 23, 79]. That means that the surface reaction to form $SiHCl_3$ is faster than the transport of the reactant to the surface, which is HCl in the case of etching. In contrast, the low-temperature region is the reaction rate limited region. The two regions can be identified more clearly for the processes with 2% HCl compared to the results of Habuka et al. It is deduced that the mass transport limited effect gets stronger in the low HCl concentration region. A clear etching rate independent region for temperatures above 950 – 1000°C was shown by [80] for concentrations of 0.4% and 1% HCl in H_2. The decrease of the etching rate with an increasing *T* at high temperatures, which was observed by Schmich for MG silicon wafers, can be explained due to fact that no neighboring wafers were used for these processes. Multicrystalline wafers, especially from MG and UMG silicon, might show large differences in the etching behavior, at least when no neighboring wafers are compared, but wafers with different grain structures. This assumption was proved by another etching process at 1300°C with the same MG material, resulting in a higher value (blue dot in Fig. 3.7), which corresponds to the conclusions above.

From the overall rate constants at different temperatures and the Arrhenius equation eq. (3-12), Habuka et al. obtained a value for the activation energy of $E_A = 1.5x10^5\,Jmol^{-1}$ [70]. The same was done in this work. However, the HCl input concentration was applied, unlike Habuka, who was taking into account the transport phenomena in the reactor and was able to calculate the HCl concentration at the surface. Thus, for the calculation of E_A, data of UMG-1 (2% HCl) only in the reaction rate limited region was used. A value of $E_A = 1.8x10^5\ Jmol^{-1}$ was obtained, which is in good agreement with Habuka.

Threshold temperature of significant etching

To determine, above which temperature the etching of silicon by gaseous HCl occurs, an etching experiment was carried out with UMG silicon for a concentration of 2% HCl in H_2 ambient. The threshold temperature shall be denoted by T_{etch}. In the experiment, the temperature was increased from room temperature to above 1000°C, and the exhaust gas composition was analyzed simultaneously by FT-IR. The determination of T_{etch} was done using the concentration data of $SiHCl_3$, since it is the main silicon-containing species in the exhaust gas and can be detected by FT-IR with favorable detection limits. In Fig. 3.8 the $SiHCl_3$ concentration depending on the temperature is presented. T_{etch} was calculated as

described in the following. The standard deviation of the background was calculated in a lower temperature region (between 500°C and 600°C). T_{etch} was then determined as temperature at which the triple standard deviation is permanently exceeded by the $SiHCl_3$ signal. T_{etch} (2% HCl in H_2, UMG silicon) has a value of 720°C ± 30°C. The high uncertainty of ± 30°C derives from the fact that the $SiHCl_3$ can only be analyzed with a certain time delay between the reaction on the silicon surface and the detection, and from the fact that a relatively high temperature rate of 50K/min was applied.

T_{etch} is an important threshold temperature for HCl gas gettering processes (see chapter 5). If gettering was still efficient at temperatures below 720°C, no etching of the silicon would occur, which could be advantageous, because longer gettering times could be applied to the wafers without losing thickness and without the risk of changing the surface morphology.

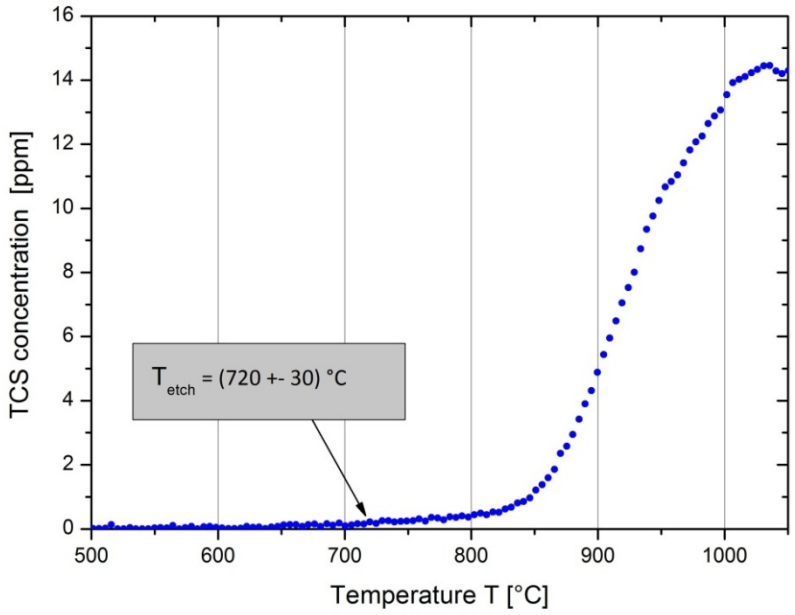

Fig. 3.8 $SiHCl_3$ (trichlorosilane) concentration during etching with 2% HCl in H_2 depending on the temperature. The $SiHCl_3$ concentration was measured by FT-IR for the determination of T_{etch}.

3.2.3 Surface morphology

HCl gas etching can result in smooth or rough surfaces depending on the HCl concentration and the temperature applied. Defects which are the reasons for rough silicon surfaces are for example etch pits or bunches. The formation of etch pits is caused by a high vacancy concentration at the crystal surface leading to a higher vertical etching in competition to the horizontal etching via steps [81]. Another explanation is given in [82], where it is proposed that deep etch pits are caused by dislocations or micro-defects, which can amongst others derive from the thermal stress in the crystal during high-temperature processes. Bunch formation is a macroscopic pile up of steps at the surface [75]. Further characterization of

the surface morphology after HCl gas etching can be found in the mentioned literature, e.g., also in [70, 74]. It can be summarized that with higher temperatures and lower HCl input concentrations a smoother surface morphology with less defect based structures can be obtained. Transition lines were reported from smooth to pitted and bunched surfaces [75], which are shown in Fig. 3.9. The transition lines strongly depend on the type of ambient (H_2 or Ar). It has to be noted that these transition lines are based on only moncrystalline silicon.

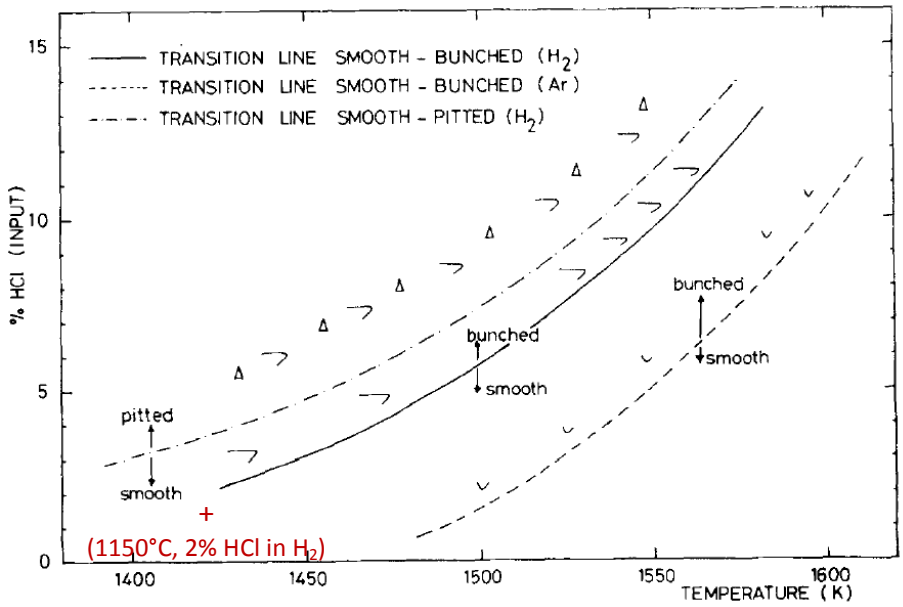

Fig. 3.9 Transition lines from smooth to pitted and bunched silicon surface structures depending on the HCl concentration and the temperature in H_2 ambient and in Ar ambient [75]. The red mark shows the process used for the wafer in Fig. 3.10.

The red mark represents a HCl gas gettering process on UMG silicon, which was performed in this work, applying a temperature of 1150°C and a concentration of 2% HCl in H_2. Fig. 3.10 shows the scanning electron microscope (SEM) images of the silicon surface in different grains after gettering. It can be observed that in some grains of the same sample bunches are visible (see Fig. 3.10 (a)) and in others the surface is relatively smooth (see Fig. 3.10 (b)). This corresponds to the findings in literature, as the conditions are near the transition line between bunched and smooth surfaces in H_2 ambient in Fig. 3.9.

At temperatures below 1000°C the formation of a dark haze on some parts of the silicon sample could be seen. Similar observations are reported in [18, 83]. A photograph showing the haze on the surface of the sample is presented in Fig. 3.11. In the regions of the haze deep extremely rough structures could be identified by scanning electron microscopy (SEM). They are most likely leading to a high absorption of light. It was observed that the area of haze formation increases with increasing HCl concentration from 2% HCl to 12% HCl [84].

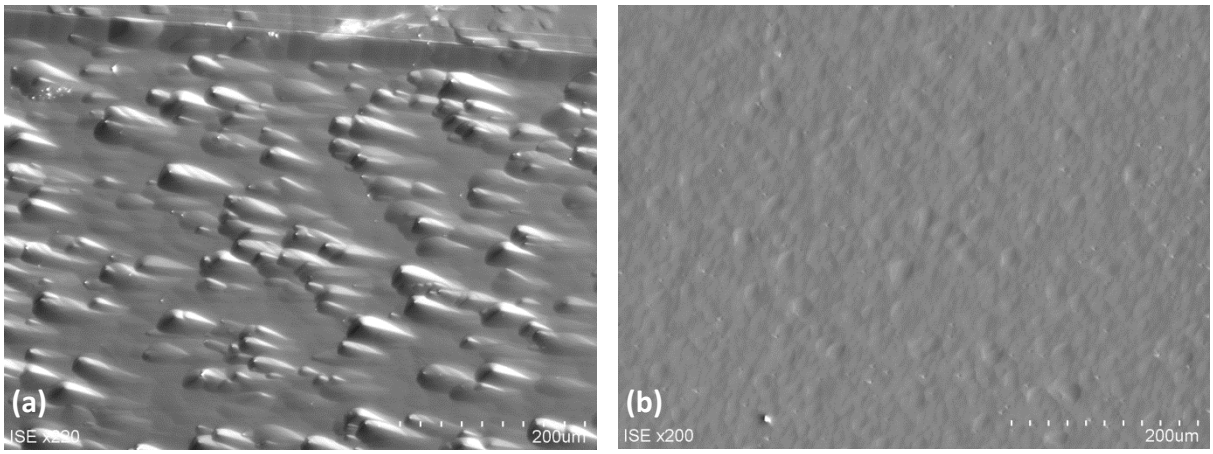

Fig. 3.10 UMG silicon wafer showing a grain with bunches on the surface (a) and the same wafer showing a relatively smooth surface of a different grain (b) after HCl gas gettering at 1150°C with 2% HCl in H_2.

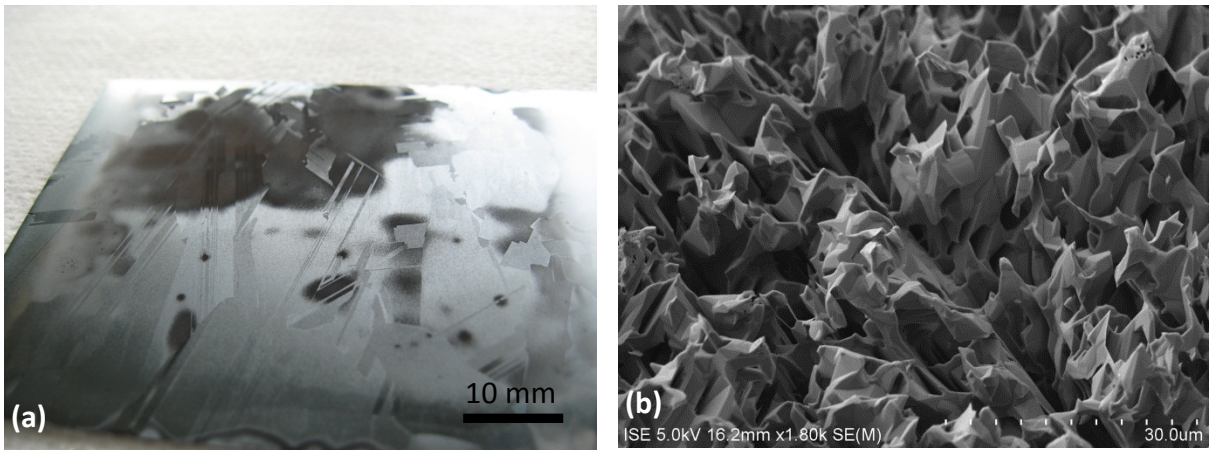

Fig. 3.11 UMG silicon wafer with a rough surface after HCl gas gettering at 880°C with 12% HCl in H_2 (a). The dark haze in the upper part of the sample was analyzed by scanning electron microscopy (SEM) revealing deep extremely rough structures as for example shown in (b) [84].

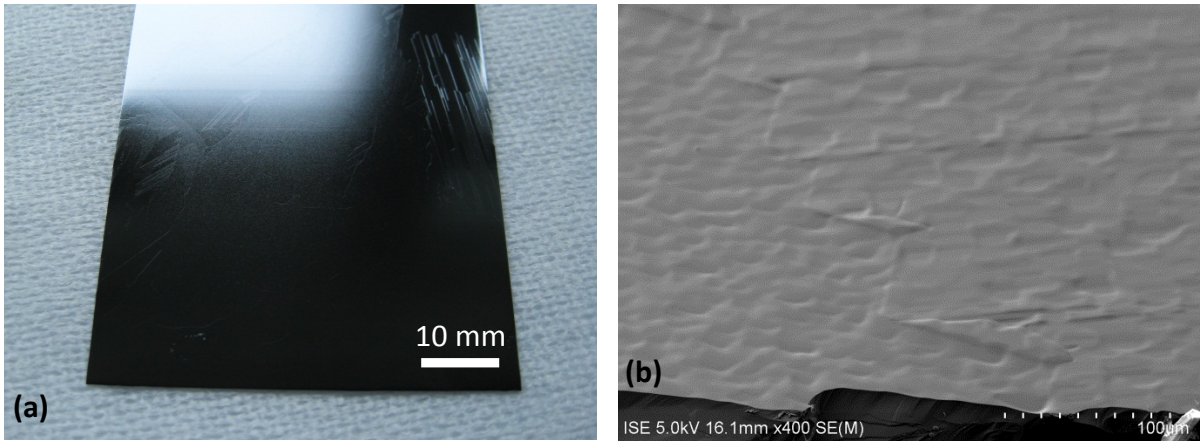

Fig. 3.12 UMG silicon wafer with a smooth surface after HCl gas gettering at 1300°C with 2% HCl in H_2, visible in the photograph (a) and in the scanning electron microscopy (SEM) image (b) [84].

3.3 HCl gas gettering in silicon

3.3.1 Principles of gettering

Gettering in general means a process, whereby impurities are moved to a place or turned into a state, where they are less detrimental to the device. As shown in Fig. 3.13, the principle concept of gettering involves three steps [85], which are (1) the release of the impurity from its original state, (2) the diffusion to the gettering site, and (3) the capture of the impurity at the gettering site. Some prerequisites can be defined for effective gettering. The energy barrier for the release of the impurity should not be too high, the diffusion length of the impurity should be shorter than the distance to the gettering site, and the captured impurity should not be released easily.

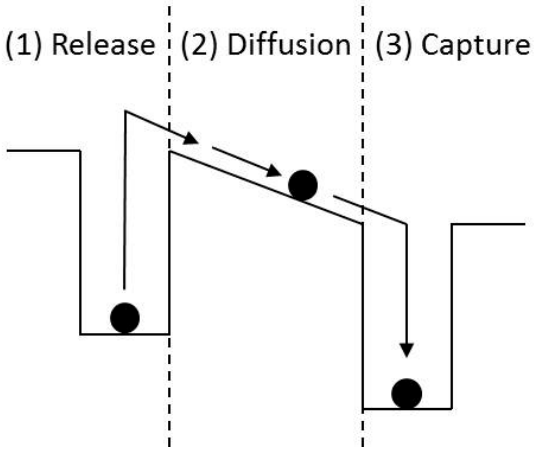

Fig. 3.13 Principle concept of gettering involving three steps: (1) release, (2) diffusion, and (3) capture of impurities (from [85]).

Furthermore, three general types of gettering mechanisms can be distinguished [86], which are (a) relaxation gettering, (b) segregation gettering, and (c) phosphorus diffusion gettering. However, it should be mentioned that it is not always possible to classify all gettering techniques to fit into one of the three categories, and sometimes the mechanism is a mixture of more types. An example for relaxation gettering is the gettering by silicon-oxide precipitates, where silicon-oxide precipitates are formed intentionally during temperature processes, which act as gettering sites for supersaturated metallic impurities. Higher precipitation rates at the gettering sites compared to regions with lower rates yield in a dissolved metallic impurity concentration gradient, which causes diffusion towards the gettering sites. This technique is used for example in silicon device technology to reduce the concentration of metallic impurities in the device-active surface region. An example for

segregation gettering is aluminum gettering, whereby a gradient of the solubility of impurities occurs by forming an Al-Si eutectic, which has a higher solubility for impurities as silicon. Phosphorus diffusion gettering has its own category involving a variety of physical processes. Mainly it is a combination of a so-called self-interstitial injection mechanism and segregation gettering. Silicon atoms in substitutional sites are replaced by phosphorus atoms leading to silicon self-interstitials, which in turn replace substitutional metal atoms. In consequence, the metal atoms are mobile by diffusing interstitially towards the gettering layer. The heavily n-type doped surface region additionally is part of the unique gettering mechanism leading to a change of the solubility of metals in this region.

There are further classifications for gettering techniques, as for example intrinsic and extrinsic gettering, depending on the location where the gettering takes place, in the wafer bulk (intrinsic) or at the wafer surface (extrinsic). Moreover, it is divided between internal and external gettering techniques, depending on whether an external treatment such as diffusion, mechanical damage, or ion implantation is needed. Internal gettering only requires annealing, e.g., the above mentioned gettering by silicon-oxide precipitates.

Phosphorus diffusion gettering (PDG) and aluminum gettering (AlG) are the most common gettering methods for photovoltaic applications, because they are done during steps in the solar cell processing which are essential. PDG is usually done by a diffusion process using P sources like $POCl_3$ in an oxidizing atmosphere, whereby P_2O_5 is formed. It is deposited on the silicon surface forming a phosphosilicate glass (PSG) layer, which in turn acts as a doping source for the phosphorus in-diffusion. Afterwards, the PSG layer has to be removed in a further wet-chemical etching step. This process is essential for solar cells to form the P diffused emitter. PSG was used in this work to compare HCl gas gettering to an established gettering technique. Therefore, not only the PSG was removed after the gettering step but also the emitter, which was done by the wet-chemical etching of 5 µm of the silicon surface. This procedure was applied to silicon substrates for the EpiWE cell processing. More information on PDG in silicon can be found in [86-91]. AlG is usually done by the deposition and subsequent heating of a thin Al layer on the rear side of the silicon wafer, which simultaneously forms the rear contact of the solar cell. AlG was not used as a comparison in this work. More information on AlG in silicon can be found in [86, 92, 93]. A summary of the gettering efficiency and kinetics of gettering processes like PSG and AlG in silicon photovoltaics is given in [94].

3.3.2 Reaction mechanism

HCl gas gettering is an external extrinsic gettering technique, which is called chemical gettering. It cannot be classified as one of the main three gettering mechanisms. The assumed mechanism is shortly described followed by a more detailed discussion about the

mechanism steps and their limitations for the efficiency of HCl gas gettering based on the current understanding. The simplified mechanism is illustrated in Fig. 3.14. Lots of metallic impurities in silicon are present in precipitates. They have to be dissolved into interstitial sites (A), to be able to diffuse to the surface of the silicon substrate (B). The reactant HCl is diffusing from the main gas stream into the stagnant boundary layer (C), where it reacts with the metal at the silicon surface (D). The metal chloride products, in this case $FeCl_2$, are volatile at high temperatures and are transported away from the surface (E) before diffusing back into the main gas stream (F). It is important to note what the actual gettering driving force is. Metals which are present at the surface from the beginning are removed by the reaction with HCl and thus a concentration gradient occurs between the silicon bulk and the surface. This gradient leads to the diffusion directed towards the surface. An alternative mechanism should be mentioned, which involves an intermediate step via the reaction of the metal not directly with HCl from the gas phase but with already chemisorbed $*SiCl_2$ at the surface [18]. The steps (A) – (F) can be assigned to the principle steps of gettering (see Fig. 3.13). Step (A) corresponds to the release step (1), step (B) corresponds to the diffusion step (2), and steps (C) – (F) correspond to the capture step (3).

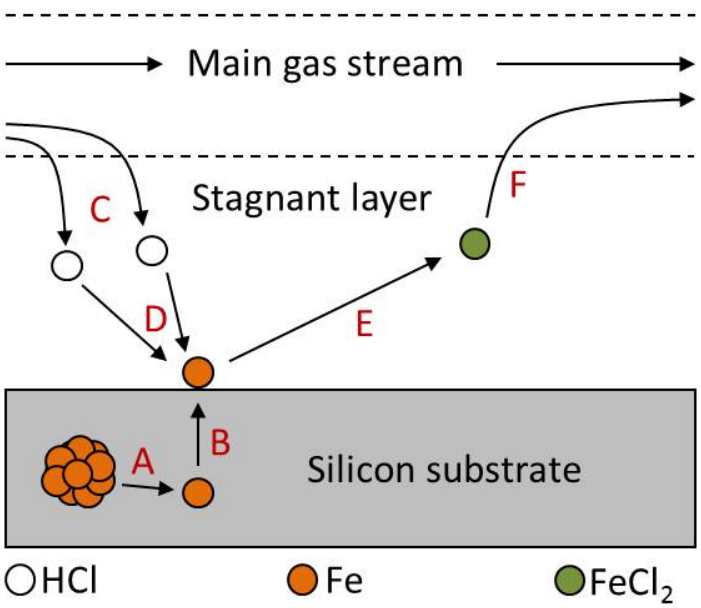

Fig. 3.14 Assumed mechanism of HCl gas gettering of silicon, using the example of Fe.

First reports about HCl gas gettering were published in the early seventies by Robinson and Heiman [95]. The number of publications on this topic is small. Almost all studies have been done in the microelectronic industry on the gettering by HCl and Cl_2 during the oxidation process for metal oxide semiconductor (MOS) structures [95-104]. The results from all these

studies can be summarized as follows. It was found that the presence of HCl or Cl_2 during oxidation had a beneficial effect on the oxide properties. It could reduce the surface state density at the silicon/silicon-oxide interface and improve the breakdown characteristics of MOS capacitors. Several reasons for the improvement were reported. A decrease of sodium ion instabilities in silicon oxide could be observed by the presence of HCl. Furthermore, HCl in the ambient was found to prevent impurities, e.g. positive alkaline ions but also transition metals, which are diffusing through the walls of the quartz furnace, from being introduced into the growing oxide. The main gettering effect was reported to be based on the reaction with the impurities to form volatile chlorine species. It was found that Cu could easily be removed, whereas Au and Cr were not affected. It could be shown that the concentration of interstitial Fe decreased by chlorine gettering leading to increasing minority carrier diffusion lengths in silicon.

But there are main differences of HCl gas gettering, described in the above mentioned studies in the microelectronic industry, compared to HCl gas gettering as described in this work and compared to potential gettering applications for the photovoltaic industry. Because of these differences, which are summarized in Table 3.1, the process known from the microelectronic industry cannot be directly adopted for solar cells.

Table 3.1 Differences between HCl gas gettering of silicon wafers for microelectronic and photovoltaic applications.

	Microelectronics	**Photovoltaics**
Impurity and defect concentration in the wafers	low	high (many interactions possible)
Purpose	remove impurities that may have contaminated the wafers	upgrade the low-quality silicon wafers
Regions to be affected	surface-near regions	whole wafer bulk
Gas atmosphere	oxidizing (with O_2)	Non-oxidizing (in this work primarily HCl/H_2)

The only report of experiments in a non-oxidizing atmosphere was published by Green et al. [98], who used a mixture of 4% HCl in SiH_4/H_2. Czochralski (Cz) wafers, which had been intentionally contaminated with Fe, Au, Cu or a combination of all three metals, were treated at 1000°C and 1275°C. After process times of 0, 10, 30, and 100 minutes, the

concentrations in the wafers were measured by optical emission spectroscopy (OES). At 1000°C, Cu needed 20 – 100 minutes to be reduced by a factor of 10, but Fe and Au could not be removed even after 100 minutes. At 1275°C, the concentrations of all three impurities were substantially reduced. For example, Fe was reduced by a factor of 5 after 30 minutes of gettering. An interesting observation was made: The removal of each impurity was retarded, when all three impurities were present in the sample, but could be achieved by longer treatments. This means that the presence of the other impurities may affect the gettering of one species. Green et al. compared the amount of concentration which was removed in the experiments with the theoretical expectations, assuming that only the diffusion through the wafer to the surface was the limiting factor. That means that metal impurities are homogeneously distributed throughout the wafer, and that there is a perfect sink at the surface during the gettering. It was found that much higher concentrations should have been removed when the assumptions are valid. Green et al. believed that the surface reaction rate and the evaporation rate of the products are sufficiently high and are not the limiting steps. They concluded that the impurities might be associated with crystalline defects or with precipitates and are much more difficult to getter, and referred to [87], where it was found for Cu that P gettering from precipitates was indeed slower than anticipated.

The question is further discussed, which the rate limiting step during HCl gas gettering is. Therefore, the individual mechanism steps are described more detailed. Step (A) in Fig. 3.14 represents the dissolution of metals in precipitates into interstitial sites. The metal precipitates can consist of one or several metals either in their metallic state or in form of silicide phases, e.g., in the case of Fe including ε-FeSi, α-$FeSi_2$, β-$FeSi_2$, Fe_5Si_3, Fe_3Si [86, 105], and are primarily located at extended defects like dislocations and grain boundaries in the case of multicrystalline silicon. The dissolution of precipitates can be done by a high-temperature treatment [18, 106, 107]. However, it was found that Fe can be present in the form of oxides or silicates, thus exhibiting a higher binding energy, which significantly reduces the removal rate [107]. Step (B) represents the diffusion of the interstitially dissolved metallic impurity. The diffusion is described by Fick's law (see section 6.1), whereby the diffusion length might be a limiting factor for efficient gettering, depending on the diffusivity D and the time t. This limitation can be avoided by choosing higher gettering temperatures and longer gettering times. However, there are other limitations which might be much more complicated to avoid. It was reported that the high strain field of a dislocation can form a preferable precipitation site for interstitially diffusing metals, which means that it is in competition to the gettering [108]. Furthermore, the metals can react with other impurities such as carbon or oxygen to form again more stable species than silicides or agglomerates [109]. Step (C) represents the diffusion of HCl from the main gas stream into the stagnant boundary layer. As described in section 3.2.2 for the silicon etching reaction,

there is a mass transport limiting region for high temperatures where the supply of HCl at the surface is the limiting factor. For the gettering reaction this might not be an issue because the surface reaction is considered to be exothermic, as it is explained in the next step. Step (D) represents the reaction with HCl to form volatile chloride species. In the case of Fe the reaction can be described by

$$Fe + 2HCl \rightleftharpoons FeCl_2 + H_2 \,. \tag{3-14}$$

The reaction of eq. (3-14) is not strictly in a thermodynamic equilibrium because the transport of HCl to and of the products away from the surface plays an important role. However, the reaction near the surface can be assumed to be in an equilibrium state. If this limit case is examined, the forward reaction of eq. (3-14) is an exothermic reaction. This means that for higher temperatures the equilibrium is shifted to the left side of the reaction, preferring the reverse reaction according to Le Chatelier's principle [110]. But the reaction rate of the forward reaction is still considered to be rapid for high temperatures [98]. Step (E) and (F) represent the transport of the products away from the surface. Since the vapor pressures of transition metal chlorides, e.g., Cu and Fe chlorides, are rather high at high temperatures [98], steps (E) and (F) are not considered to be rate limiting for typical HCl gas gettering processes. An advantage of HCl gas gettering over other gettering techniques is the infinite volume where the gettered impurities are captured, meaning the main gas stream in which the impurities are transported away. Other gettering techniques might be limited by the number of impurity atoms which can be gettered, as only a finite layer volume is available where the capture takes place. This layer is the heavily n-type doped surface layer in the case of PDG and the Al-Si eutectic layer in the case of AlG.

It can be concluded that most likely steps (A) and (B), which represent the release and the diffusion of impurities, are rate limiting and are therefore limiting the gettering efficiency of HCl gas gettering. In the case of the diffusion (B), high temperatures and long gettering times could provide a high diffusivity, at least for moderately and fast diffusing transition metals. However, interactions between diffusing metals and precipitates or other impurities like carbon or oxygen can again be limiting the gettering efficiency, especially in low-grade silicon like MG and UMG, which is primarily used in this work.

The most relevant parameters for the evaluation of the gettering processes are the gettering efficiency η_{gett} and the reduction by gettering r_{gett}. Both parameters represent the gettering success, whereas η_{gett} is the formal parameter, which is a factor commonly used for the assessment of gettering techniques. The parameter r_{gett} is additionally given in this work, as it is a more descriptive parameter given in percent (%).

η_{gett} is defined as

$$\eta_{\mathrm{gett}} = \frac{C_b}{C_a}, \tag{3-15}$$

where C_b denotes the impurity concentration before gettering and C_a denotes the impurity concentration after gettering. Because in this work, neighboring wafers were compared, it means that C_b is the impurity concentration measured in the wafer *without* gettering and C_a is the impurity concentration measured in the wafer *with* gettering. η_{gett} is a factor which is nondimensional. r_{gett} is given in % and is defined as

$$r_{\mathrm{gett}} = \frac{C_b - C_a}{C_b} \cdot 100\%\,. \tag{3-16}$$

Note that the relative maximum deviation d_{max} (%) and the maximum deviation factor f_{max}, which will be defined in chapter 4, are comparable to the relative reduction by gettering r_{gett} (%) and to the gettering efficiency η_{gett}, respectively.

3.3.3 RTCVD100 reactor

The epitaxial layers for EpiWE cells are grown by CVD in atmospheric pressure chemical vapor deposition (APCVD) reactors, which were developed at the *Fraunhofer ISE*. HCl gas gettering can be performed in the same reactor prior to the epitaxy. The different APCVD reactors are listed in the following by the year of their first run, including references with detailed descriptions: RTCVD100 (1996) [24, 25], RTCVD160 (2002) [24, 111], ConCVD (2006) [24, 112, 113], and ProConCVD (2012) [112]. The development has been done from lab-type reactors with silicon substrate sizes of about 50x50 mm^2 to high-throughput inline reactors with conventional industrial silicon wafer sizes of 156x156 mm^2 and a throughput of more than 1000 wafers per hour, corresponding to 30 m^2 per hour. If not otherwise indicated, all HCl gas gettering and epitaxial processes for EpiWE cells were done in the RTCVD100, which thus shall be further described in the following.

RTCVD means rapid thermal chemical vapor deposition. “100” indicates the diameter of the quartz tube of 100 mm. Fig. 3.15 shows a photograph of the RTCVD100 reactor during a process. It has been operating for over 15 years now. Until today more than 4200 processes were run in this reactor, which proves its high reliability. The reactor consists of a quartz tube, with an opening to load the tube with the sample carrier. It has a gas inlet (right side in the photograph) and an outlet (left side in the photograph). Optical heating by 6 halogen lamps (4.5 kW each) on top of the housing allows for rapid heating and cooling. A scheme of the sample carrier is shown in Fig. 3.16. Usually, two samples in the size of 65x50 mm^2 were placed in the middle of the top wafer row, where the temperature distribution can be

considered as constant. This means that the complete gettering and deposition area is 50x100 mm^2. The temperature is controlled near the surface of the samples by a thermo couple, which extends into the sample carrier through the exhaust funnel. The residual positions (top and bottom wafer row) were filled with silicon dummy wafers in case of epitaxy and with quartz wafers in case of HCl gas gettering processes. For the gas inlet a simple quartz tube with a round inlet cross section was used. During a process the gas is streaming between the top and the bottom wafer rows. A typical process in the RTCVD100 consists of purging steps by N_2 and subsequent H_2, followed by the rapid heating with a temperature ramp of 150K/min. After a short H_2 annealing, the main process step is applied. It can be HCl gas gettering or a combination of gettering and a subsequent epitaxial deposition of silicon. The latter is used for EpiWE solar cells. The HCl gas gettering was done at temperatures between 650°C and 1300°C with HCl concentrations in H_2 ambient of 2% - 16%. The gettering time was between 10 and 180 minutes. The epitaxy was done using $SiHCl_3$ in H_2 at around 1225°C for 4 – 6 minutes, adding B_2H_6 for p-doped layers. The H_2 annealing step prior to the gettering was used to remove the native oxide on the wafer surface and as pre-gettering step to dissolve metal precipitates. After the main process step, the reactor was again purged by H_2 and the system was cooled down with a temperature ramp of 150K/min.

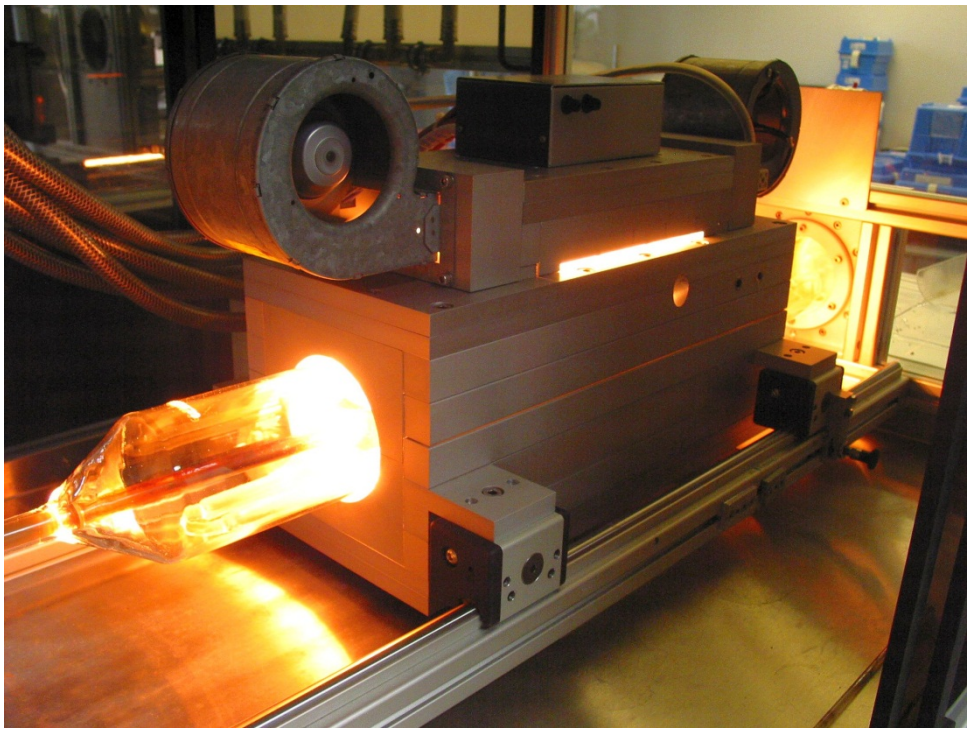

Fig. 3.15 RTCVD100 reactor during processing.

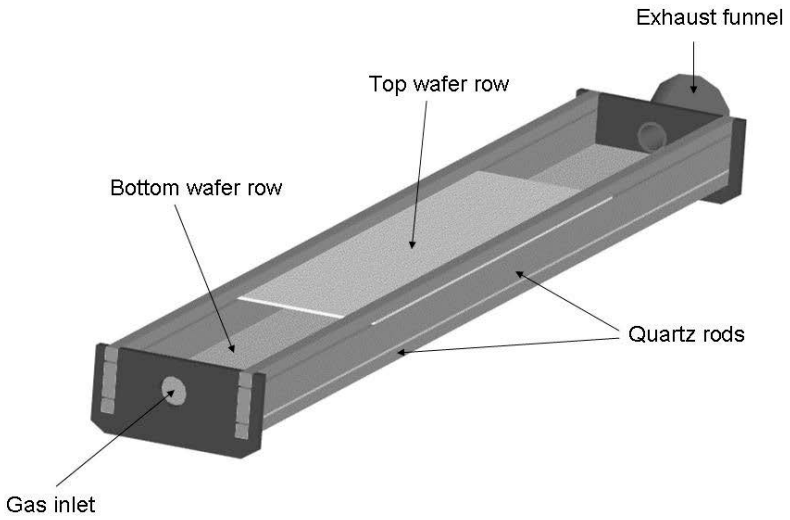

Fig. 3.16 Scheme of the sample carrier used in the RTCVD100 reactor [24].

3.3.4 Contamination sources

Several contamination sources are imaginable on the way from the silicon ingot, via the HCl gettering process, to the final impurity analysis. However, most steps are done at room temperature, like for example, wafer cutting, laser cutting to smaller samples, and preparing samples for analysis. Cleaning the surface of the silicon samples between such steps is therefore sufficient. The contamination risk is much higher though during high-temperature HCl gas gettering, as impurities are able to diffuse into the silicon sample and may be distributed completely in a very short time. In this case, a subsequent surface clean would not be helpful. Although gettering is actually a technique to remove impurities from the silicon, the background contamination in the reactor might limit the maximum removal quantity. This has to be considered, especially when low-cost silicon with rather low impurity levels is investigated. Thus, contamination sources during a high-temperature process like HCl gas gettering are briefly discussed in the following.

Impurities in the quartz material

As described above, semiconductor grade quartz carriers and plates (‘HSQ 300 quality’ from ‘Heraeus’) are used for all HCl gettering processes. INAA measurements were performed on quartz material in three different states to control the transition metal impurity level and assess the expected influences on the gettering results, as delivered, after wet-chemical cleaning, and after several processes in the RTCVD100 reactor.

The results of the INAA measurements, which are given in Table 3.2, reveal that the transition metal content is very low in the used quartz material. The contamination level after several processes is comparable to the untreated and cleaned quartz samples. Furthermore, an out-diffusion of transition metals from the quartz material is negligible, since the diffusivity of most common transition metals in quartz is low as compared to silicon [67] [114].

Table 3.2 Transition metal contaminations in the quartz material used for HCl gas gettering processes measured by INAA (DL = Detection Limit).

Element	supplier spec. [ng/g]	as delivered [ng/g]	after wet-chemical cleaning [ng/g]	after several processes [ng/g]
Cr	< 50	13	< DL (2)	< DL (2)
Mn	< 50	16	15	7
Fe	100	< DL (150)	< DL (90)	< DL (120)
Co	-	< DL (0.9)	0.7	2
Ni	-	< DL (170)	< DL (90)	< DL (130)

Impurities in the HCl gas

The HCl gas, which was used for all HCl gas gettering processes in this work, had a purity of ≥ 99.999% (Vol). The residual impurities were specified by the supplier 'Praxair' as shown in Table 3.3. Based on these values, a maximum possible contamination of the silicon samples during a typical HCl gas gettering process in the RTCVD100 reactor was estimated. Table 3.4 shows values which are based on a HCl density of 1.534 kg/m^3 (15°C, 1 bar)[115] and a concentration of 2% HCl in H_2. Note that these values are estimated for the hypothetical case that all impurities of the HCl gas are diffusing into the silicon samples during the process and that no gettering effect occurs.

Table 3.3 Certified specification of the HCl gas (Praxair, Belgium).

Element	mass fraction [ppmw]
Cr	< 0.1
Fe	< 0.5
Co	< 0.1
Ni	< 0.1
Cu	< 0.1

These calculations show that several tens or even hundreds of ng/g of common transition metals might be present in the silicon samples after high-temperature processes in the worst case. This has to be considered when evaluating impurity analyses on silicon with low impurity levels (see chapter 5).

Table 3.4 Estimated maximum possible contamination by impurities in the HCl gas. Values are estimated based on the specification of the used HCl gas for a typical HCl gettering process in the RTCVD100 reactor with a concentration of 2% HCl in H_2, assuming that all amounts of impurities diffuse into the silicon sample and that no gettering effect occurs.

Element	max. contamination after 10 min gettering [ng/g]	max. contamination after 30 min gettering [ng/g]
Cr	40	120
Fe	200	600
Co	40	120
Ni	40	120
Cu	40	120

3.4 Summary

In this chapter, the process of HCl gas gettering was explained. Properties of transition metals in silicon were described, like the diffusion, the distribution, and the impact on the minority carrier lifetime and thus the conversion efficiency of solar cells, which are the most relevant for the HCl gas gettering process.

The etching of silicon by HCl gas was discussed in theory, and the dependence of the silicon etching rate on HCl gas concentration and temperature was experimentally approved by the HCl gas gettering in MG and UMG silicon. Further experiments with UMG silicon demonstrated, that the threshold temperature of significant etching is 720°C ± 30°C (2% HCl/H_2), and that the surface morphology after typical gettering processes was as expected, corresponding to the dependence on the HCl gas concentration and temperature, which is generally described in the literature.

Based on the general mechanism of gettering processes, the HCl gas gettering mechanism was depicted step by step with emphasis on the limiting potential of every single step. HCl gas gettering is described as an external extrinsic chemical gettering technique, which is known from the microelectronic industry and has to be adopted for the purpose of solar cell applications. The removal of much higher impurity concentrations from the whole wafer

bulk instead of only the surface region and the use of a different gas atmosphere are required. The principle steps of gettering, which are the release, the diffusion, and the capture of impurities, can also be applied to HCl gas gettering in silicon. The release is represented by the dissolution of metal containing precipitates, which are primarily located at extended defects like dislocations and grain boundaries in mc silicon. This step can be limiting in terms of the gettering efficiency, depending on the chemical state of the metal in the precipitates. The second step is the diffusion. The diffusion length depends on the diffusivity for each impurity at a given temperature and on the process time, but it is only reliable if no interactions occur between the diffusing impurity and other impurities, e.g., in the form of precipitates. These interactions are most likely the case in low-grade silicon like MG and UMG silicon. The third step, the capture of the impurity, might be limiting in case the surface reaction and the transport of the products away from the surface during HCl gas gettering are not rapid enough. However, the first and the second step (release and diffusion) are considered to be likely the limiting steps for HCl gas gettering in silicon, especially in low-grade silicon.

Finally, the experimental setup was described. The RTCVD100 reactor is the first of several APCVD reactors which were developed at the *Fraunhofer ISE*. It was used in this work for epitaxy processes in the EpiWE cell concept, as well as for most HCl gas gettering processes. It enables rapid thermal processes by optical heating for sample sizes of about 50x50 mm^2 with various process gases like N_2, H_2, HCl, $SiHCl_3$, and B_2H_6. The samples are placed in a quartz carrier. For HCl gas gettering, the most relevant parameters, which can be varied, are temperature, time, and HCl concentration. Possible contamination sources during HCl gas gettering are the quartz material and the HCl gas. However, the contamination risk is marginal, as the transition metal concentrations in the used quartz was measured to be below the specification after several processes and the purity of the used HCl gas is above 5N. However, the presence of several tens of ng/g for each of the most prominent transition metals should be taken into account, especially when analysis results are discussed, which show transition metal concentrations in the same order of magnitude.

4 Impurity distribution in the silicon ingot

In this chapter, the vertical and horizontal impurity distribution in a multicrystalline silicon ingot is described. Especially, 3d transition metal concentrations in neighboring wafers are analyzed. The principle of assuming that neighboring wafers are comparable in terms of the metal content is discussed as a basis for the results presented in chapter 5.

4.1 Vertical distribution in the ingot

The crystallization of a multicrystalline (mc) silicon ingot is an important step from silicon feedstock to wafers. Fig. 4.1 shows one of the first ingots which were crystallized at the Silicon Material Technology research center (SIMTEC) at the *Fraunhofer ISE* in 2008. The feedstock was melted in a quartz crucible and crystallized by unidirectional solidification from the bottom to the top, using the vertical gradient freeze (VGF) method [116].

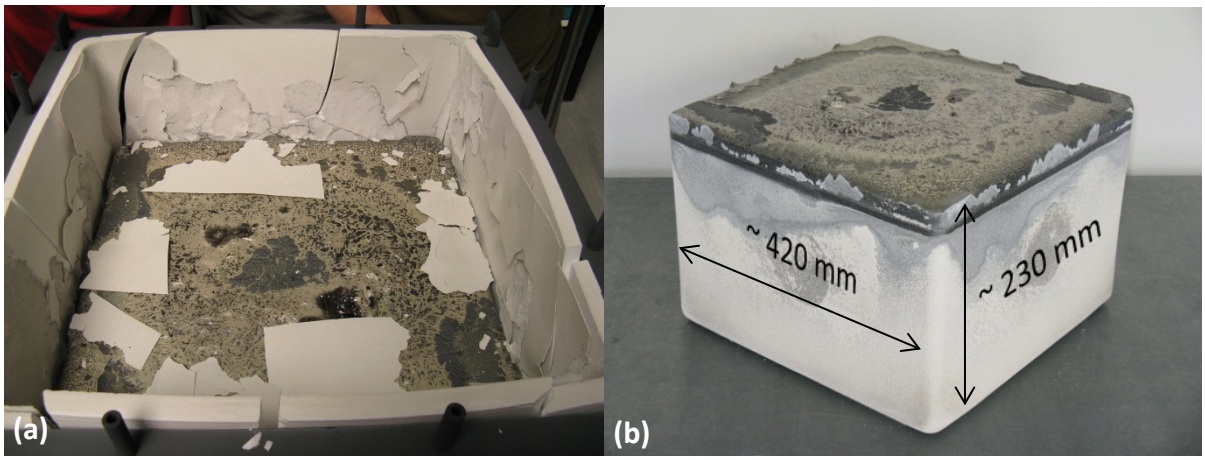

Fig. 4.1 Top view of a multicrystalline silicon ingot in the quartz crucible after crystallization at ISE from 84 kg highly doped silicon (a) and side view after complete removal of the crucible (b).

As described elsewhere [117, 118], most impurities present in the feedstock have equilibrium segregation coefficients k_0 with $k_0 < 1$. Because k_0 is defined as the concentration in the solid C_S divided by the concentration in the liquid C_L (eq. (4-1)), that means that most impurities are accumulated in the liquid phase during the crystallization process and are therefore found with increasing concentrations towards the top of in the solid ingot.

$$k_0 = \frac{C_S}{C_L}. \tag{4-1}$$

The impurity concentration profile in the crystallized ingot should follow eq. (4-2), which is called Scheil equation [119]

$$C_S(x) = k_0\, C_i\, (1-x)^{k_0-1}\,. \tag{4-2}$$

C_i and C_s describe the initial impurity concentration and the impurity concentration in the solid, respectively. x is referred to as the relative ingot height. The measured profile can be described by the Scheil equation quite well for doping elements like B, P, or As. Note that eq. (4-2) is only valid at thermal equilibrium, which is not the case for the actual crystal growth. That's why the effective segregation coefficient k_{eff} was defined by [120], which is dependent on the diffusivity in the liquid D_L, the crystal growth rate V, and the diffusion boundary layer thickness δ

$$k_{\text{eff}} = \frac{k_0}{k_0 + (1-k_0)\exp(-\frac{V\delta}{D_L})}\,. \tag{4-3}$$

Nevertheless, when the growth rate V is low, the exponent in eq. (4-3) tends towards zero and k_{eff} is equal to k_0. This is mostly given for practical silicon crystal growth, as well as for the presented results of this work (V < 1mm/min). An example of a doping profile can be seen in Fig. 4.2. A vertical column with a size of approximately 1x1x20 cm^3 was cut out of an ingot which was crystallized from highly doped UMG silicon. The column was irradiated as a whole and analyzed by INAA in 1 cm steps. Since B and P cannot be detected by INAA, As was selected to determine a doping profile. With a segregation coefficient in silicon of k_0(As) = 0.3 [121] and a measured initial As concentration in the feedstock of C_i = 0.108 µg/g, the data are in good agreement with the theory.

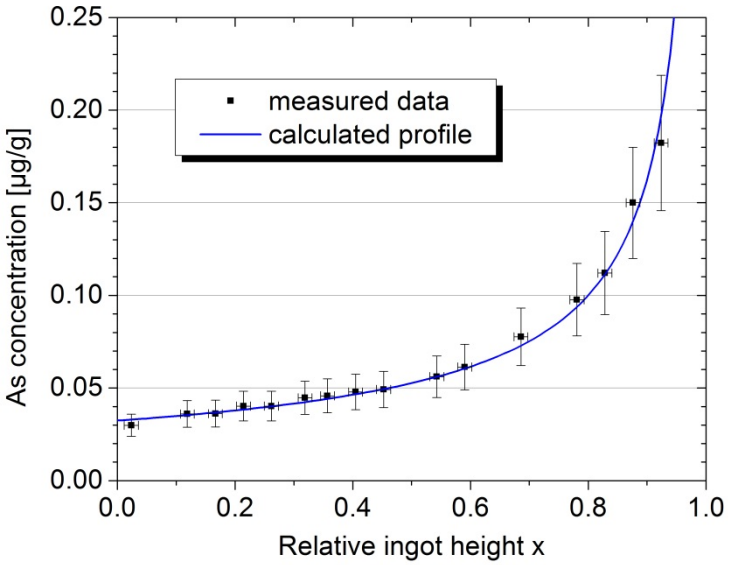

Fig. 4.2 As concentration data in an UMG silicon ingot measured by INAA follows the Scheil equation [122].

Since it cannot be detected by INAA, PGAA measurements were done to determine the B concentration for some positions of the column. With a segregation coefficient in silicon of k_0(B) = 0.8 [4], the data are again in good agreement with the calculated Scheil profile (see Fig. 4.3).

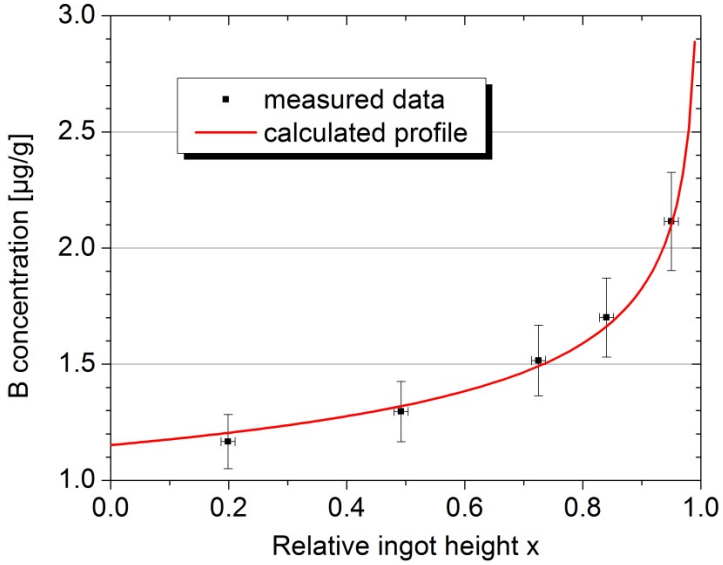

Fig. 4.3 B concentration data in an UMG silicon ingot measured by PGAA follows the Scheil equation.

In contrast to B, P, and As, impurities like transition metals exhibit much lower segregation coefficients. For example, Fe has a segregation coefficient of k_0(Fe) = 6.4x10^{-6} [117]. Therefore, a strong increase in the concentration is expected towards the top of the ingot. But transition metals exhibit much higher diffusivities and much lower solid solubility limits at a given temperature than B, P, and As. That means that they are mobile, and that they can form precipitates during the cooling of the ingot. There is a back-diffusion of impurities from the very top into lower regions of the ingot. At the bottom there is an in-diffusion of impurities from the crucible [123]. That's why transition metals are not necessarily strictly distributed in the ingot as expected from the simple Scheil equation. Riepe et al. [66] investigated ingots which were intentionally contaminated by transition metals and were able to simulate diffusion profiles of Fe and Cu, considering the in-diffusion from the crucible as well as the back-diffusion from the top region. An analysis of transition metal profiles of a SoG mc silicon ingot can be found in [118].

The UMG silicon columns were also investigated in terms of 3d transition metals. A profile of Co was presented in [124], which shows a typical shape. It is depicted in Fig. 4.4. The in-diffusion from the crucible leads to an increased concentration at the bottom. The increasing concentration towards the top due to segregation is also noticeable. However, the increase at the very top of the ingot is not as strong as reported in [118], where the increase of Co between the middle and the top of the ingot was almost two orders of magnitude.

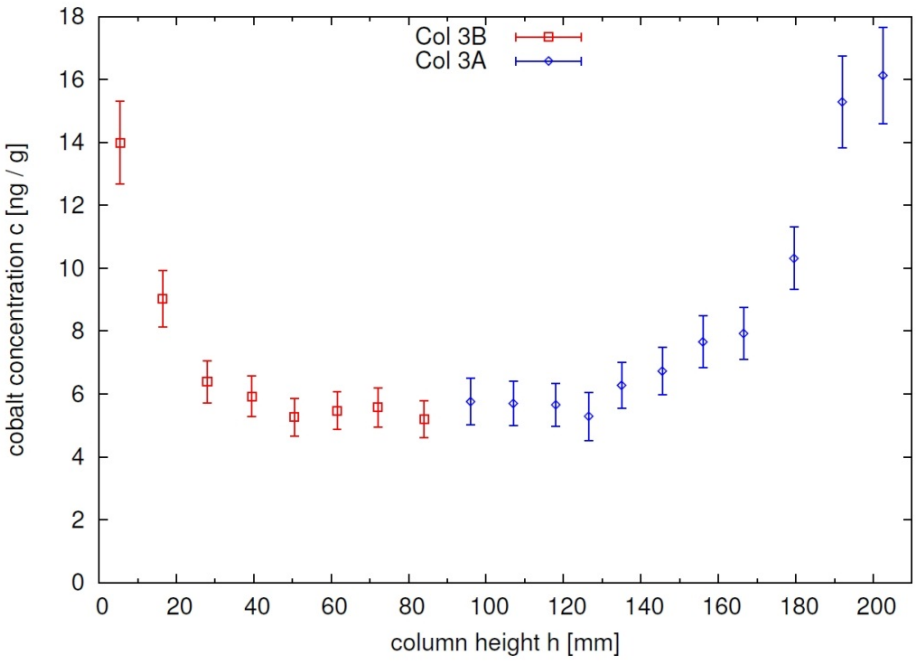

Fig. 4.4 Co concentration profile (in ng/g) of an UMG silicon ingot measured by INAA [124].

Results of an INAA measurement of MG silicon of three different vertical ingot positions (bottom, middle, top) are shown in Fig. 4.5. The concentration at the bottom is several orders of magnitude lower than at the middle which is unusual. However, only values of three positions are available, and the exact positions in the ingot are not known. Comparing the Co concentration level to the level which was measured in the UMG silicon column, it is 2 – 3 orders of magnitude higher in MG than in UMG silicon.

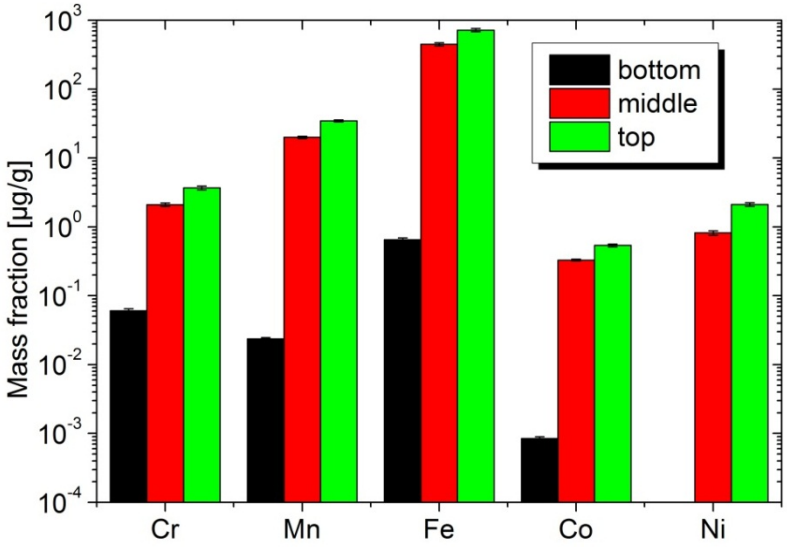

Fig. 4.5 Metal concentration (in µg/g) in MG silicon depending on the position in the ingot measured by INAA [122].

Metal concentration ratios, which were also obtained in [122], are given in Table 4.1, including actual data from this work, which were obtained by further INAA measurements on wafers from a different brick of the same ingot. Especially, the Fe – Mn ratio is in excellent agreement with the earlier publication. Although the values for Fe – Cr and Fe – Co are slightly exceeded, they still support the assumption that rough metal profiles could be calculated from one measured profile. But yet, this has to be investigated also for other silicon feedstock material.

Table 4.1 Transition metal ratios in wafers made from 99.7% MG Si.

Position in ingot	Fe – Mn concentration ratio	Fe – Cr concentration ratio	Fe – Co concentration ratio	Ref
middle	23 ± 2	210 ± 20	1360 ± 110	[122]
Lower middle	22	282	1992	this work

4.2 Horizontal distribution in the wafer

The horizontal distribution of metal impurities can be demonstrated on single wafers which were obtained by usual cutting of bricks by a multiwire saw. UMG silicon wafers in the size of 156x156 mm^2 with a thickness of approx. 280 µm were cut into 6 smaller wafers (A-F) in the size of 65x50 mm^2 (see Fig. 4.6). These wafers were analyzed by ICP-OES. In Table 4.2 the results of wafer 354-B and 354-D are presented. 2 to 6 times higher concentrations can be found in wafer B compared to D, depending on the impurity element. Even larger differences were observed in other experiments in this work. The reason is the mc silicon material as the grain structure of neighboring samples in horizontal direction of the ingot can differ a lot and is usually not comparable between horizontal neighboring samples. In Fig. 4.7 an example of the grain structure of two samples cut from one 156x156 mm^2 sized wafer is presented. It cannot be predicted from the structure or size of the grains, which one of two samples contain higher impurity concentrations. It can only be stated that different impurity contents have to be expected. That's why only a comparison between vertical neighboring wafers with the same grain structure is reasonable. Such samples are investigated in the following section 4.3.

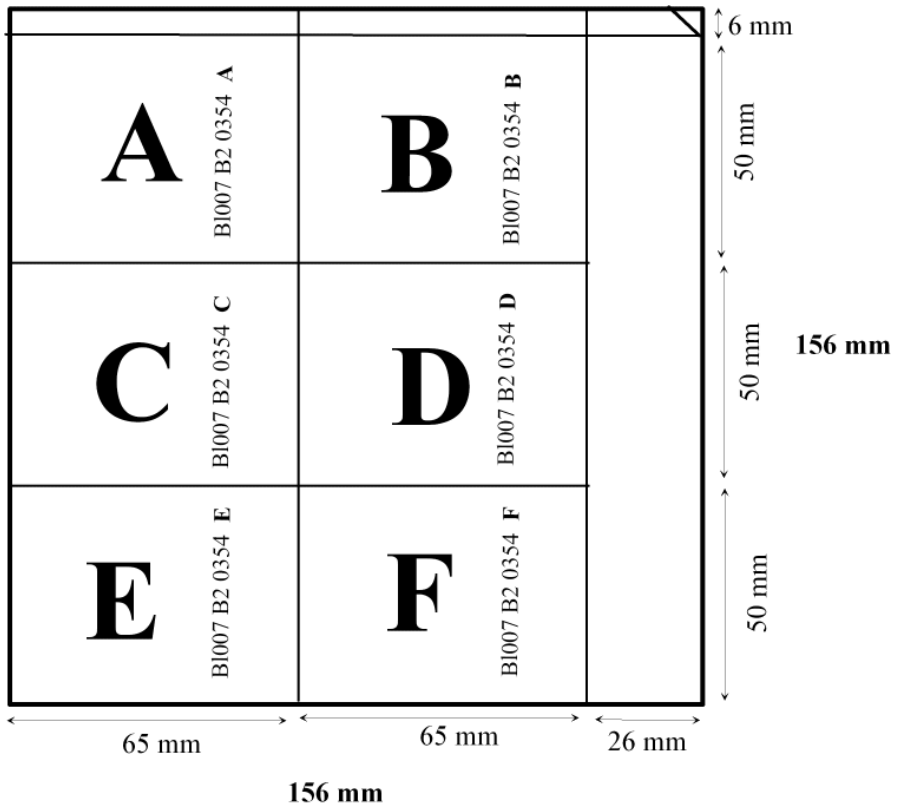

Fig. 4.6 Schematic of the cutting of a 156x156 mm^2 wafer into smaller samples for ICP-OES analysis.

Table 4.2 Metal concentrations of two samples cut from one 156x156 mm^2 sized UMG-Si wafer measured by ICP-OES.

Element	354-B [µg/g]	354-D [µg/g]
Fe	1.22 ± 0.04	0.41 ± 0.08
Mn	0.040 ± 0.002	0.007 ± 0.001
Cr	0.046 ± 0.008	0.027 ± 0.005
Al	3.52 ± 0.16	1.38 ± 0.27

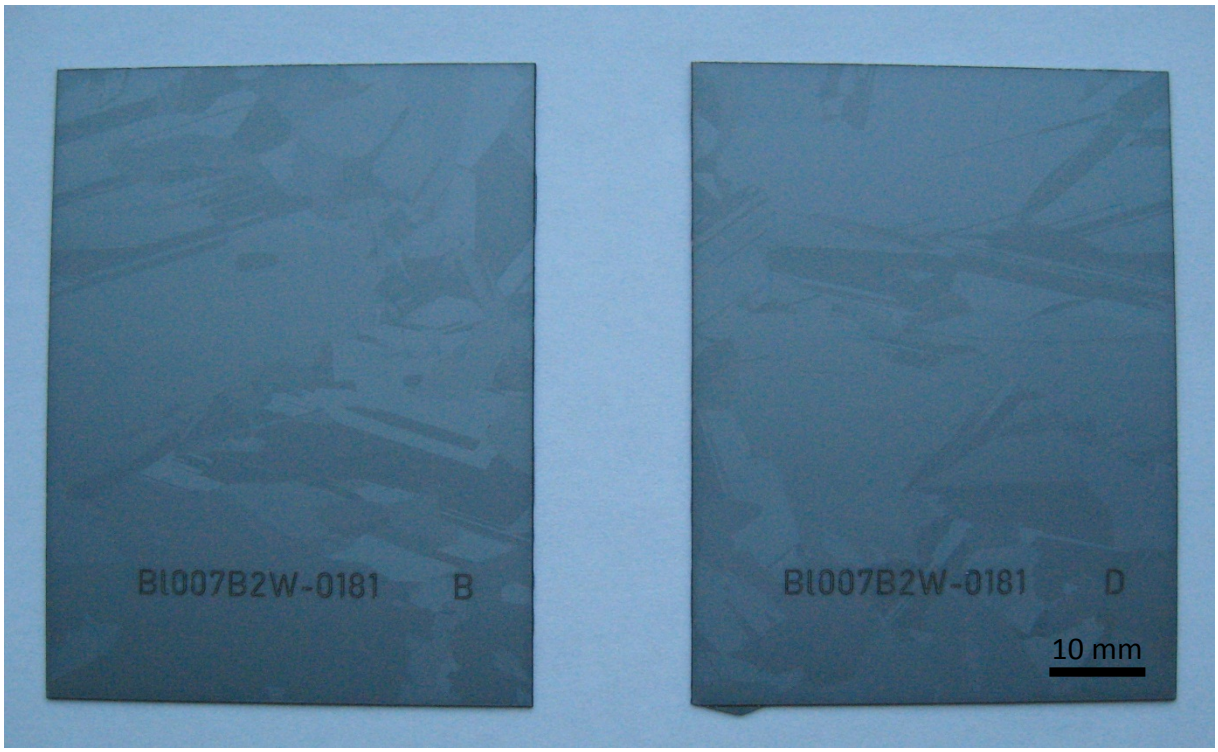

Fig. 4.7 Horizontal neighboring wafers cut from one 156x156 mm^2 sized wafer.

4.3 Vertical neighboring wafers

An example of vertical neighboring wafers can be seen in Fig. 4.8. The grain structure of both samples looks very similar. It is assumed that vertical neighboring wafers with a comparable grain structure contain comparable amounts of impurities. Therefore, vertical neighboring wafers are used in literature to evaluate processes like gettering, e.g., in [85, 125]. However, in most publications mono-c or mc silicon with low impurity content is investigated. Only few reports are found for MG and UMG silicon wafers, e.g., in a recent study [126], where P gettering is applied to UMG silicon wafers and compared with as-grown neighboring wafers without gettering. It is reported that unexpected results were found for Al and Ca. Higher concentrations were measured by ICP-OES in the samples with gettering. It was concluded in

the study that most likely either a contamination occurred during sample preparation or the concentrations were different in the compared sample from the beginning. The assumption that vertical neighboring wafers contain the same amount of impurities is investigated in the following sections of this chapter for MG and UMG silicon wafers.

4.3.1 Definition of d_{max} and f_{max}

To evaluate the magnitude of deviation between neighboring wafers, a parameter d_{max} (given in %) shall be defined. It represents the maximum deviation in neighboring wafers due to fluctuations of impurity concentrations in the silicon material. Also, a maximum deviation factor f_{max} shall be described, which is defined in analogy to the gettering efficiency η_{gett}. The definitions are explained in the following.

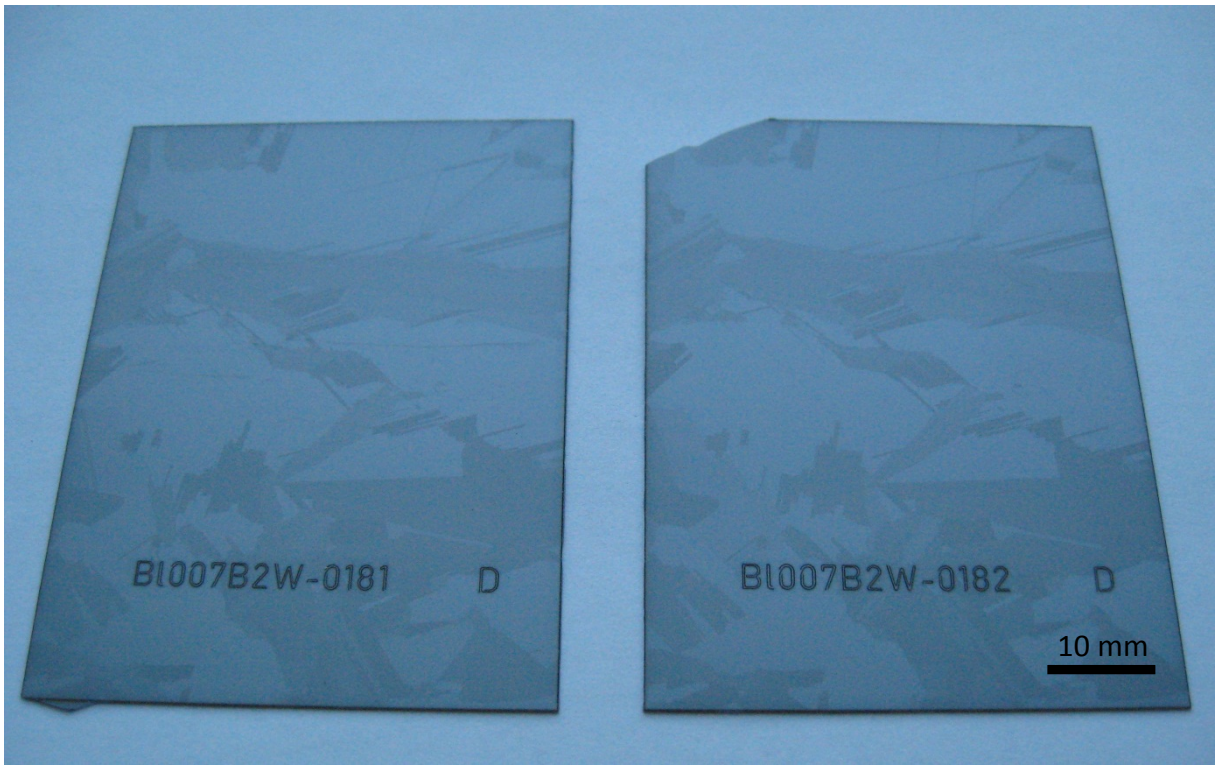

Fig. 4.8 Vertical neighboring wafers with similar grain structures.

The deviation d of the concentration of one wafer “i“ to its direct neighboring wafer “i+1“ is defined by the following equation:

$$d_{i,i+1} = \frac{|C_i - C_{i+1}|}{\max(C_i, C_{i+1})} \cdot 100\% \,. \tag{4-4}$$

C_i is the concentration of wafer "i". C_{i+1} is the concentration of wafer "i+1". The denominator (bottom of the fraction) means the greater of both values C_i and C_{i+1}. Eq. (4-4) can be calculated for several pairs of neighboring wafers. Then, the maximum deviation d_{max} is defined as

$$d_{max} = \max\left(d_{i,i+1}\right), \tag{4-5}$$

and the maximum deviation factor is defined as

$$f_{max} = \frac{100\%}{100\% - d_{max}}. \tag{4-6}$$

An example of the calculation for Fe is given in the following section.

4.3.2 Analysis of MG silicon vertical neighboring wafers

A sequence of 4 neighboring MG wafers near the top of an ingot, which were made from 99.7% (2.7N) MG silicon feedstock, was investigated by means of ICP-OES. The results for Ti, Cr, Mn, Fe, Ni, and Cu are shown in Fig. 4.9. At the first sight, there are only small deviations between the transition metal concentrations of neighboring wafers. To be able to quantify these deviations, d_{max} and f_{max} are calculated. An example is given for Fe. Placing the Fe concentration values into eq. (4-4) leads to:

$$d_{1,2}(Fe) \approx 0.4\%, \tag{4-7}$$

$$d_{2,3}(Fe) \approx 11\%, \tag{4-8}$$

$$d_{3,4}(Fe) \approx 7\%. \tag{4-9}$$

The maximum deviation therefore is:

$$d_{max}(\mathrm{Fe}) = d_{2,3}(\mathrm{Fe}) \approx 11\%. \tag{4-10}$$

Then, the maximum deviation factor is calculated by eq. (4-6):

$$f_{max}(Fe) \approx 1.13. \tag{4-11}$$

d_{max} and f_{max} values for other transition metals in MG silicon wafers are summarized in Table 4.3.

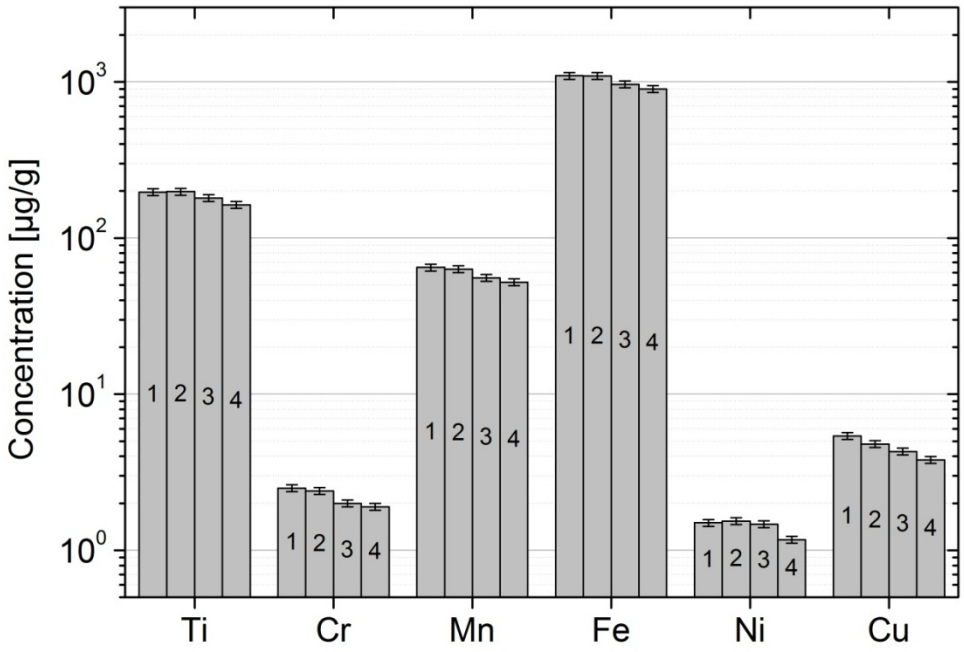

Fig. 4.9 Transition metal concentrations in 4 neighboring wafers made from 99.7% MG Si measured by ICP-OES.

MG silicon neighboring wafers were measured by ICP-OES to evaluate the deviation of the metal content from a wafer to its neighboring wafer. The results of 4 neighboring wafers are shown in Table 4.3. The overall high metal content signifies that the samples come from the very top of the ingot. The proportions are typical for MG silicon [6]: Fe is present with the highest content, followed by Ti and Mn. Other 3d transition metals have lower values. Co could not be detected (detection limit DL = 0.02 µg/g).

Table 4.3 Transition metal concentrations and the maximum deviation of neighboring wafers made from 99.7% MG Si measured by ICP-OES (DL = detection limit).

	C_1 [µg/g]	C_2 [µg/g]	C_3 [µg/g]	C_4 [µg/g]	max. deviation d_{max} [%]	max. deviation factor f_{max}
Ti	197 ± 10	198 ± 10	180 ± 9	163 ± 8	9	1.10
Cr	2.5 ± 0.1	2.4 ± 0.1	2.0 ± 0.1	1.9 ± 0.1	15	1.17
Mn	64.8 ± 3.2	63.3 ± 3.2	55.6 ± 2.8	52.2 ± 2.6	12	1.14
Fe	1095 ± 55	1091 ± 54	967 ± 48	902 ± 45	11	1.13
Co	< DL (0.02)	< DL (0.02)	< DL (0.02)	< DL (0.02)	-	-
Ni	1.50 ± 0.08	1.54 ± 0.09	1.47 ± 0.07	1.17 ± 0.06	20	1.25
Cu	5.4 ± 0.3	4.8 ± 0.2	4.3 ± 0.2	3.8 ± 0.2	11	1.13

From Table 4.3 it can be concluded that the maximum deviation d_{max} of each measured transition metal in the MG wafers is in the range of 10-20%. It lies above the uncertainty of measurement, which is usually around 5 – 10%, and therefore it has to be taken into account when neighboring MG wafers are compared in terms of the transition metal content. The reason for the high deviations will be discussed in the following section.

4.3.3 Analysis of UMG silicon vertical neighboring wafers

Standard vertical neighboring wafers, which were made from 99.97% (3.7N) UMG silicon feedstock, were investigated in terms of their transition metal concentrations. The analysis of the UMG wafers was done in the same way as described in section 4.3.2 for MG wafers. To get improved statistics, a sequence of 10 wafers was investigated instead of 4 wafers. An overview of the results for Ti, Mn, Fe, and Ni is presented in Fig. 4.10. The concentrations of Cu, Cr, and Mn were below the ICP-OES detection limits (DL), which were determined to be DL(Cu) = 25 ng/g, DL(Cr) = 26 ng/g, and DL(Mn) = 25 ng/g, respectively. To gain results at least for one of the above mentioned elements, the samples were also analyzed by the single-element analysis method AAS for the determination of Mn. A detection limit of DL(Mn) = 0.1 ng/g could be achieved, which is far below the actually determined Mn concentrations of 2 – 15 ng/g. The Ni concentration of only one sample was below the detection limit of 23 ng/g. The calculated relative maximum deviations d_{max} as well as the maximum deviation factors f_{max} are shown in Table 4.4.

It is obvious that large deviations between the UMG neighboring wafers occur, especially for Ti. Much higher deviations between neighboring wafers are present in the UMG silicon compared to the MG silicon. For example, the difference between the Fe content of direct neighboring UMG silicon wafers is a maximum factor of 6, while for the MG wafers, analyzed in section 4.3.2, the difference is up to a factor of 1.13, which is a value near the range of the uncertainty of measurement. It is not clear why the deviations between direct neighboring wafers are so much higher than expected, i.e. much higher than the uncertainty of measurement in the case of the UMG silicon. Two possible explanations are discussed.

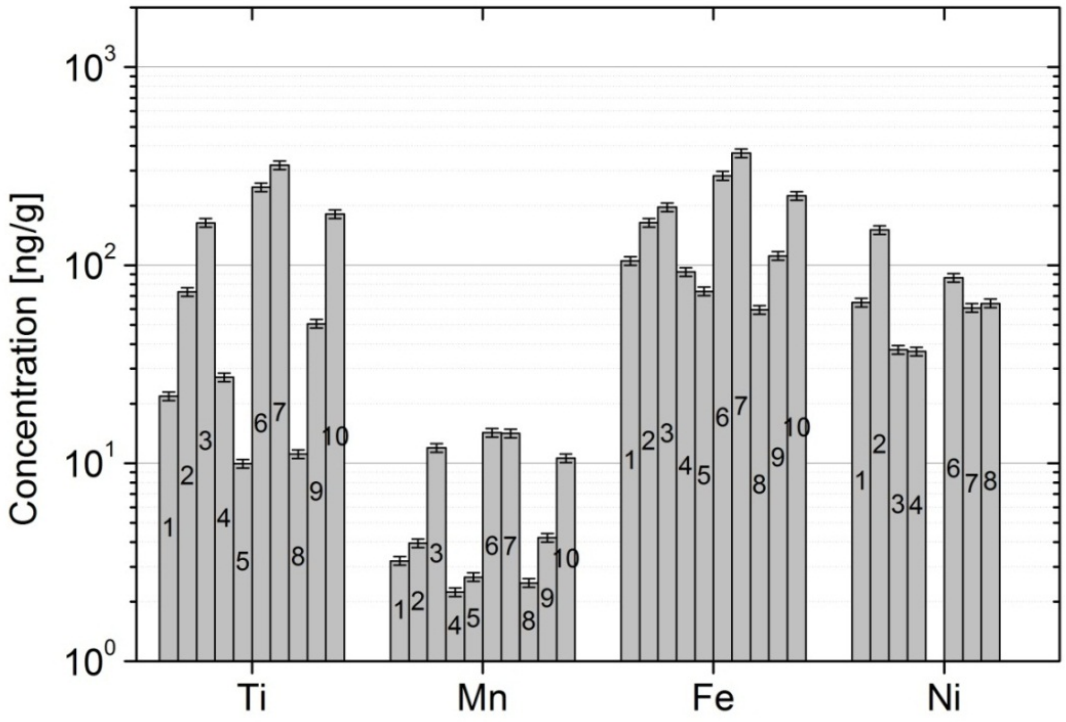

Fig. 4.10 Transition metal concentration in 10 neighboring wafers made from 99.97% UMG Si measured by ICP-OES (Ti, Fe, Ni) and AAS (Mn).

Table 4.4 Maximum deviation of transition metal concentrations of neighboring wafers made from 99.97% UMG Si measured by ICP-OES (Ti, Fe, Ni) and AAS (Mn).

Element	max. deviation d_{max} [%]	max. deviation factor f_{max}
Ti	97	28.7
Mn	82	5.7
Fe	84	6.2
Ni	75	4.0

The first explanation is based on the assumption that the ICP-OES results are valid and show true concentration values. In that case, the high fluctuations of transition metal concentrations already must have been present in the silicon ingot. But the metals in the silicon melt above the crystal are usually homogeneously distributed through convection during the crystallization process. In consequence, they should be incorporated into the crystal rather homogeneously. Fast or moderately diffusing metals like Ni or Fe might be able to diffuse during cooling and precipitate inhomogenously, but it is questionable whether this can lead to such large deviations as presented. It is especially not explainable for slowly diffusing transition metals like Ti, which is presented with deviations of the

concentration of more than one order of magnitude between two neighboring wafers. Only extreme fluctuations of the crystal growth rate could hypothetically lead to fluctuations in the transition metal concentration. Indeed, there were effects observed lately during the crystallization process which lead to a periodic deceleration of the crystal growth due to an incomplete dissipation of thermal heat away from the melt [127]. If this effect actually occurred in the investigated UMG ingot in positions where the wafers were taken from, it could explain some fluctuations. However, the highest frequency of such periodic fluctuations was observed to correspond to around 1 mm crystal growth, which means 3 – 4 wafers for the presented ingot. Unfortunately, the growth rate could not be determined in-situ during the process like the way it is currently carried out at the *Fraunhofer ISE*, since the presented ingot is one of the first ingots, which were crystallized in 2008.

The second explanation is based on a contamination, which could happen between the crystallization step and the ICP-OES measurement. It is indicative that the overall concentration level is rather low, which makes the analysis procedure more sensitive to contamination. The above described first explanation for the high fluctuations of concentrations due to fluctuations of the crystal growth must be further investigated in the future. It is planned to do resistivity measurements of still available neighboring wafers in the same ingot height to evaluate whether similar fluctuations can be also found for doping elements.

Because such large deviations in UMG wafers were not expected, another UMG material was investigated, which was crystallized from 99.995% (4.5N) silicon feedstock. The 3d transition metal concentrations of 12 neighboring wafers are presented in Fig. 4.11. The concentration of Mn was below the DL of 23 ng/g. Co and Cu concentrations are near their respective detection limits.

It can be stated that, compared to the UMG wafers made from 99.97% silicon, the basic fluctuation of transition metal contents in second material is less strong. The maximum deviation d_{max} and the maximum deviation factor f_{max} between neighboring wafers show lower values for the UMG wafers made from 99.995% silicon (see Table 4.5). For example, the difference between the Fe content of direct neighboring wafers is a maximum factor of 3, compared to 6 in the case of the earlier investigated UMG material. However, the fluctuations are still much higher than expected from the uncertainty of measurement (5 – 10%). It means that the fluctuations have to be considered for the results in chapter 5. This is done by using the parameters d_{max} and f_{max}, which were defined and calculated for the results in this chapter.

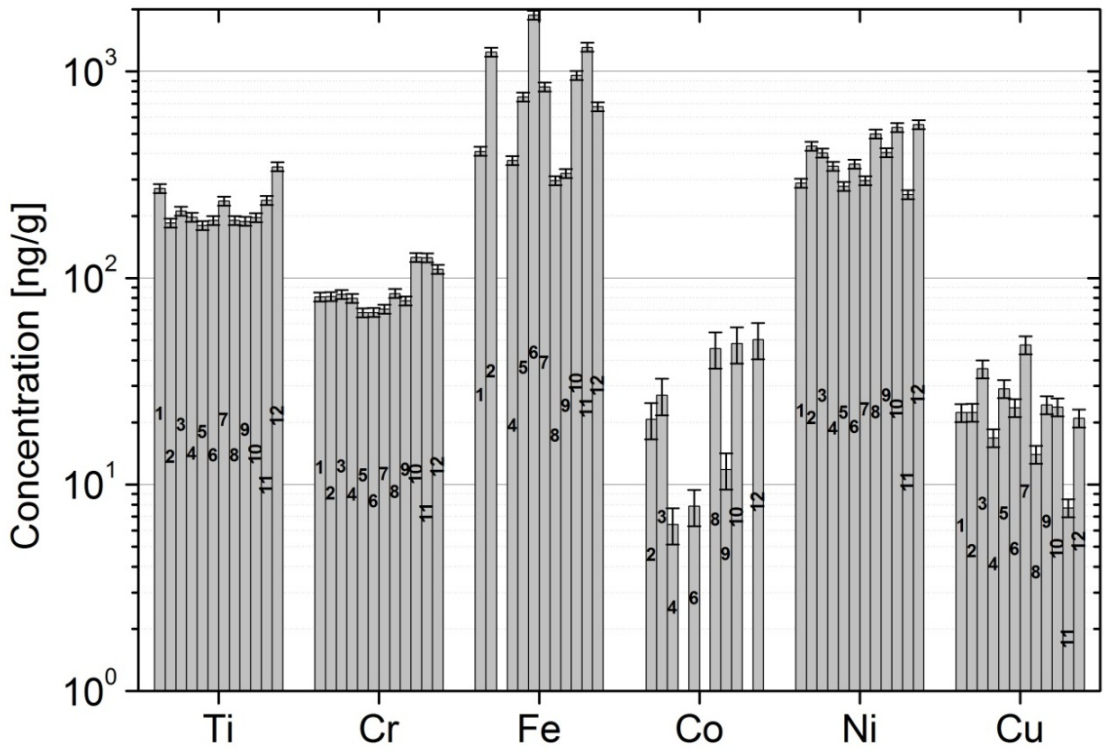

Fig. 4.11 Transition metal concentration in 12 neighboring wafers made from 99.995% UMG Si measured by ICP-OES.

Table 4.5 Maximum deviation of transition metal concentrations of neighboring wafers made from 99.995% UMG Si measured by ICP-OES.

Element	max. deviation d_{max} [%]	max. deviation factor f_{max}
Ti	32	1.47
Cr	39	1.63
Fe	67	3.02
Co	76	4.23
Ni	54	2.19
Cu	70	3.39

Although the feedstock of the second UMG silicon material is of 99.995% (4.5N) purity, after crystallization at least the same or even higher concentrations can be found in the wafers compared to the UMG wafers made from the 99.97% (3.7N) silicon, depending on the transition metal. These higher contents result from the fact that the wafers come from a higher position near the top of the ingot.

4.4 Summary

The basic fluctuation of metal impurities from wafer to wafer is much larger than anticipated in the investigated MG, and especially in the UMG silicon material. In the case of MG silicon, the deviations are more or less in the same range as the uncertainty of measurement. In the case of UMG silicon, much higher deviations from a wafer to its neighboring wafer were found in terms of 3d transition metal concentrations than expected from the uncertainty of measurement. Two explanations were discussed. The first explanation is based on periodic fluctuations of the growth rate during crystallization. As it was discussed in the above section, it is rather unlikely, but cannot be completely excluded. There will be further investigations to evaluate this topic. The second explanation is based on the contamination of the samples with transition metals, which is likely due to rather low concentration levels.

For three silicon materials, which are investigated in this work, the maximum deviation d_{max} and the maximum deviation factor f_{max} were determined for the most relevant transition metals in this chapter. A summarized overview of all d_{max} values is given in Table 4.6. The d_{max} values of MG and UMG silicon will be included into the errors of the gettering results and are visualized in the error bars of the diagrams in chapter 5. For this reasons, the errors of the UMG silicon analyses are extremely large, making it difficult in some cases to evaluate trends for the gettering efficiencies.

Table 4.6 Overview - Maximum deviation d_{max} of transition metal concentrations of neighboring wafers made from Si materials with different purity levels (compilation of Table 4.3, Table 4.4, and Table 4.5).

Si Material \ Element	99.7% MG d_{max} [%]	99.97% UMG d_{max} [%]	99.995% UMG d_{max} [%]
Ti	9	97	32
Cr	15	-	39
Mn	12	82	-
Fe	11	84	67
Co	-	-	76
Ni	20	75	54
Cu	11	-	70

5 Results of HCl gas gettering experiments and solar cells

In this chapter, HCl gas gettering experiments and results are presented with various silicon materials like metallurgical grade (MG), upgraded metallurgical grade (UMG), and solar grade (SoG) silicon wafers. The results of chapter 4 with large deviations of impurity concentrations between neighboring wafers are thereby taken into account. MG and UMG silicon wafers, which can be used as substrates in the epitaxial wafer equivalent (EpiWE) concept, are investigated by varying the gettering parameters of HCl gas gettering and comparing the bulk transition metal concentrations with that of untreated neighboring wafers. EpiWE solar cell results are presented on substrates with and without gettering. Furthermore, HCl gas gettering is also investigated for the application in the standard wafer solar cell concept. First wafer solar cell results with HCl gas gettering in an industrial-type phosphorous diffusion furnace are presented.

5.1 Gettering of MG silicon substrates for the EpiWE cell concept

For gettering experiments with MG silicon, wafers made from 99.7% silicon feedstock were used. The feedstock was crystallized by unidirectional solidification and cut into bricks. One brick was used for other experiments and the other bricks were melted and crystallized a second time. The resulting wafers after the second crystallization are investigated in this work. Former experiments with this material revealed that the wafers still contain an enormous amount of metallic impurities. For example, Fe was measured to be present in concentrations up to 10^3 µg/g [32]. Because of such high impurity contents, this material will still be called 'MG silicon' in this work, although formally it was upgraded by a second crystallization step.

The following sections present HCl gas gettering results of two different ingot positions in terms of the most common transition metal impurities, as well as a summary of the highest gettering efficiencies obtained with MG silicon wafers. For all results, the d_{max} values, which were obtained in chapter 4, are included into the errors and are visualized in the error bars of the diagrams.

5.1.1 Results from a low ingot position

Gettering experiments at 1300°C and 2% HCl in H_2 were performed with MG silicon neighboring wafers, which were taken from a lower position of the ingot (approx. 30% of the total ingot height). Two different gettering times were applied, 5 minutes and 30 minutes.

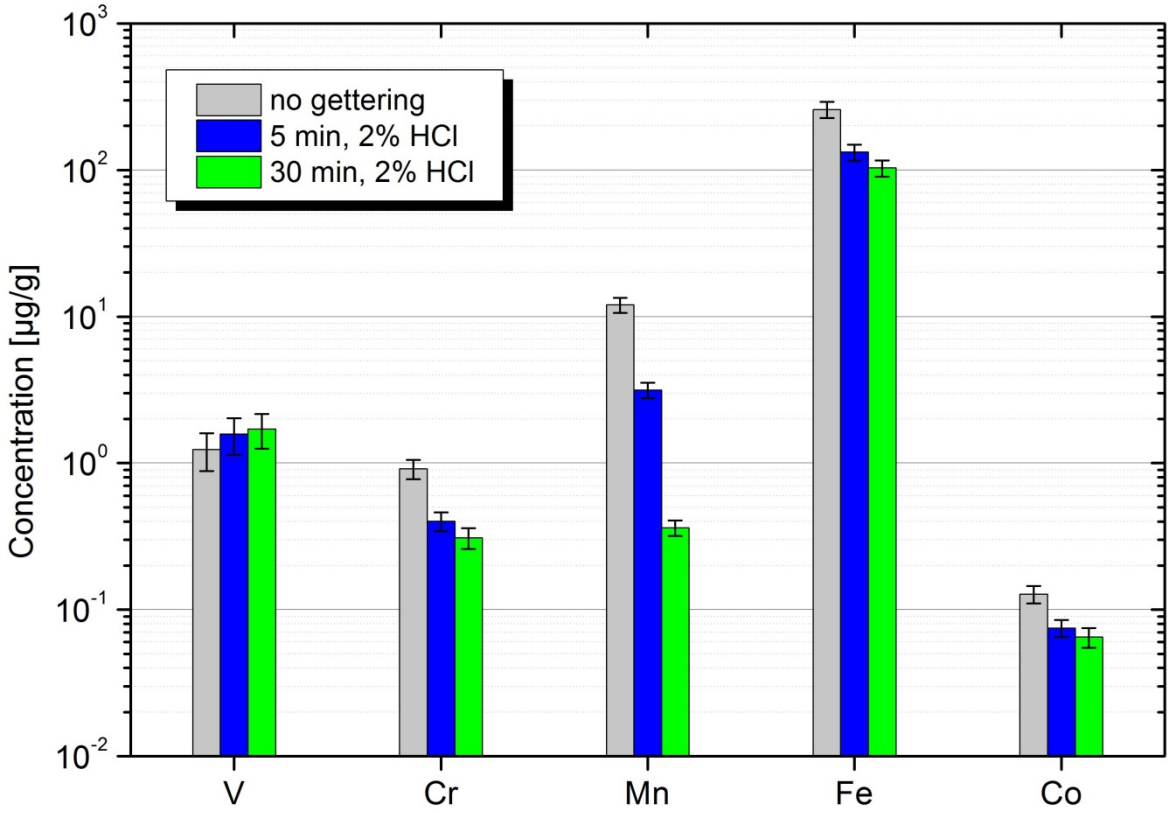

Fig. 5.1 Transition metal concentration in neighboring wafers made from 99.7% MG Si with HCl gettering (1300°C, 2% HCl in H_2) measured by INAA.

Fig. 5.1 shows the concentrations of the measured 3d transition metals V, Cr, Mn, Fe, and Co. Typical proportions of the transition metal concentrations, e.g., also reported in [128], are found in the wafers without gettering: Fe has the highest content, whereby Co has the lowest concentrations. A gettering effect can be seen for all elements, except for V. The reason is that V has the lowest diffusivity of all investigated elements (see section 3.1). Cr, Mn, Fe, and Co can be reduced by HCl gas gettering with different gettering efficiencies, which are presented in Table 5.1. After 30 minutes, Fe, Cr, and Co show gettering efficiencies (η_{gett}) of about 2 – 3, whereas the gettering of Mn is much more efficient (η_{gett} = 33). The assumption that Mn is more selective for HCl gas gettering than other transition metals, at least for a gettering time of 30 minutes, was already stated before [32]. The reason for that is not clear yet. Mn might be present in MG and UMG silicon in a less stable form than other

3d metals. Conclusions that the chemical state of an impurity has a strong influence on the gettering ability were also reported for Fe in polycrystalline silicon, for example [107]. Fe which is present in the form of silicides can be removed with much higher removal rates than in the form of oxides or silicates. This is due to a higher binding energy of Fe to oxides or silicates than to silicides.

Table 5.1 Transition metal concentrations and gettering efficiencies of neighboring wafers made from 99.7% MG Si with 30 min of HCl gettering measured by INAA.

Element	without gettering [µg/g]	30 min HCl gettering [µg/g]	gettering reduction r_{gett} [%]	gettering efficiency η_{gett}
V	1.2 ± 0.4	1.7 ± 0.5	-	-
Cr	0.92 ± 0.14	0.31 ± 0.05	66	3.0
Mn	12.0 ± 1.4	0.36 ± 0.04	97	33
Fe	259 ± 33	103 ± 13	60	2.5
Co	0.13 ± 0.02	0.07 ± 0.01	46	1.9

5.1.2 Results from a high ingot position

Fig. 5.2 shows the transition metal concentration of MG wafers, which were taken from a higher position of the ingot (approx. 60% of the total ingot height) than the wafers shown before. Therefore, higher concentrations for all metals were determined in the untreated wafers. In these experiments, an additional process was included: 15 minutes of annealing in a H_2 atmosphere. The same temperature was applied for annealing as for the gettering processes. The neighboring wafers were annealed in the same reactor and with the same process carrier.

The gettering efficiency for these wafers (see Table 5.2) is only half of the values as compared to the results shown in Table 5.1. It is suggested that a higher amount of transition metals is present in states which are not sensitive to gettering. Again, a gettering effect cannot be measured for V.

Not expected is the fact that for the H_2 annealed wafer similar gettering efficiencies could be determined as for the wafers which were treated by HCl gas gettering. Due to the same temperature profiles as for the gettering processes, the metal precipitates are expected to be dissolved interstitially up to a certain degree like in the wafers treated by gettering, but due to the lack of chloride species no reaction with metals on the surface and therefore no diffusion of metal impurities from the bulk to the surface should take place. No reasonable explanation could be found for the values of the annealed wafer. The only explanation might

be that the bulk of the wafer without gettering was contaminated with transition metals or contained 27 – 38% higher transition metal concentrations as compared to the neighboring wafers, although the d_{max} was determined to be 9 – 20%, depending on the element. This would lead to the conclusion that only for Mn (r_{gett} = 94%) a clear gettering effect could be demonstrated in MG silicon. However, r_{gett} values for Fe above 90% were already demonstrated in HCl gas gettering experiments in [129](see section 5.1.3).

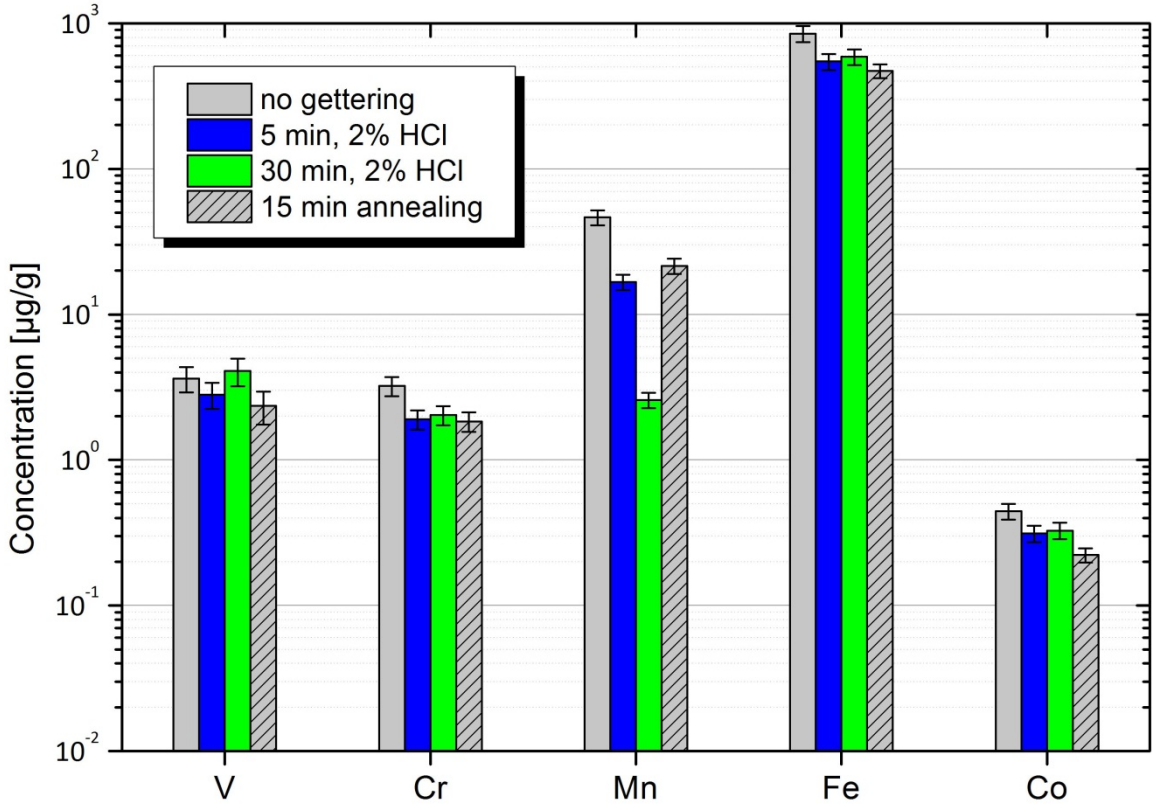

Fig. 5.2 Transition metal concentration in neighboring wafers made from 99.7% MG Si with HCl gettering (1300°C, 2% HCl in H_2) and annealing (1300°C, in H_2) measured by INAA.

Table 5.2 Results of neighboring wafers made from 99.7% MG Si with 30 min of HCl gettering measured by INAA.

Element	without gettering [µg/g]	30 min HCl gettering [µg/g]	gettering reduction r_{gett} [%]	gettering efficiency η_{gett}
V	3.6 ± 0.7	4.1 ± 0.9	-	-
Cr	3.2 ± 0.5	2.0 ± 0.3	38	1.6
Mn	46.5 ± 5.6	2.6 ± 0.3	94	17.8
Fe	849 ± 107	590 ± 74	31	1.4
Co	0.45 ± 0.06	0.33 ± 0.04	27	1.4

5.1.3 Summary of the highest gettering efficiencies

In Table 5.3, the highest so far reached gettering efficiencies on MG silicon applying 1300°C for 30 minutes with 2% HCl are presented for the most prominent 3d transition metal impurities in silicon. The highest gettering efficiency for Fe was presented in [129].

Table 5.3 Highest so far reached gettering efficiencies for Cr, Mn, and Fe in MG Si (DL = Detection Limit).

Element	without gettering [µg/g]	30 min HCl gettering [µg/g]	gettering reduction r_{gett} [%]	gettering efficiency η_{gett}
Cr	0.92 ± 0.14	0.31 ± 0.05	66	3.0
Mn	12.0 ± 1.4	0.36 ± 0.04	97	33
Fe	73.3 ± 10.9	< DL (6)	> 91	> 12

5.1.4 Discussion

HCl gas gettering can reduce the amount of metallic impurities in MG silicon wafers. The gettering efficiency of wafers from a higher ingot position is only half of that of wafers from a lower position, although the wafers without gettering from the higher position show 3 – 4 times higher transition metal concentrations. This finding is in contrast to the simple idea that higher amounts of impurities can be removed from regions with higher initial impurity concentrations. It can be concluded, that metallic impurities in regions of high concentrations are present in a state, e.g., precipitates, which do not respond to external gettering, leading to lower gettering efficiencies. This conclusion will be further discussed in section 5.2.6. It is obvious that the metal concentrations in the presented MG silicon wafers after HCl gas gettering are still far too high for the processing of EpiWE solar cells with a high performance, at least for the absence of a well-functioning diffusion barrier between the substrate and the active thin film. UMG silicon wafers with a lower initial impurity concentration seem to be much more suitable substrates for the EpiWE solar cell concept.

5.2 Gettering of UMG silicon substrates for the EpiWE cell concept

Two types of UMG materials were investigated. Highly p-doped silicon wafers with a resistivity of 0.06 – 0.12 Ωcm made from 99.97% silicon, and highly p-doped silicon wafers with a resistivity of 0.10 – 0.15 Ωcm made from 99.995% silicon.

As described in chapter 4, investigations on UMG silicon wafers revealed that there can be large deviations between neighboring wafers regarding the transition metal contents. To be

able to compare the metal content of neighboring wafers with and without gettering, these basic fluctuations have to be taken into account. That's why it was decided to include the determined maximum deviation d_{max} (see Table 4.6) into the concentration errors for both UMG silicon materials and for each element. This means that the error bars, which are shown in the diagrams in this chapter, are much larger than they would be if only the uncertainty of measurement would be considered.

In the following sections, the results of experiments are presented, in which variations of the most relevant HCl gas gettering parameters were investigated. These parameters are the gettering temperature, the gettering time, and concentration of HCl gas in H_2. Three types of reference samples were included into the experiments. The most important is the reference called "no gettering". This sample was only surface cleaned and then measured together with all samples. Reference samples treated with "annealing" and "P diffusion gettering" are also included for some experiments. Annealing was done at 1300°C with process characteristics comparable to HCl gas gettering, except that H_2 was used as process gas without HCl gas. P gettering as a reference gettering technique was done in an industrial-type P diffusion furnace for 1 hour at 900°C resulting in a sheet resistance of 16 Ω/sq. The gettering experiments were performed with both UMG materials.

5.2.1 Variation of the temperature

Fig. 5.3 shows the results of ICP-OES analysis on neighboring wafers made from 99.995% UMG silicon which were treated by HCl gas gettering at three different temperatures. The gettering was done with a concentration of 2% HCl gas in H_2 for 10 minutes. From these results, it is not possible to draw a conclusion, which temperature leads to the highest gettering efficiency. Actually, a gettering effect cannot be demonstrated. It shows that the difference between wafers with and without HCl gas gettering is smaller than the basic fluctuation of transition metal concentrations in these neighboring wafers and therefore it is not possible to evaluate the gettering efficiencies. Additionally, the general impurity level is very low in this 99.995% UMG silicon material (e.g., 10 – 100 ng/g for Cr, and 100 – 500 ng/g for Fe).

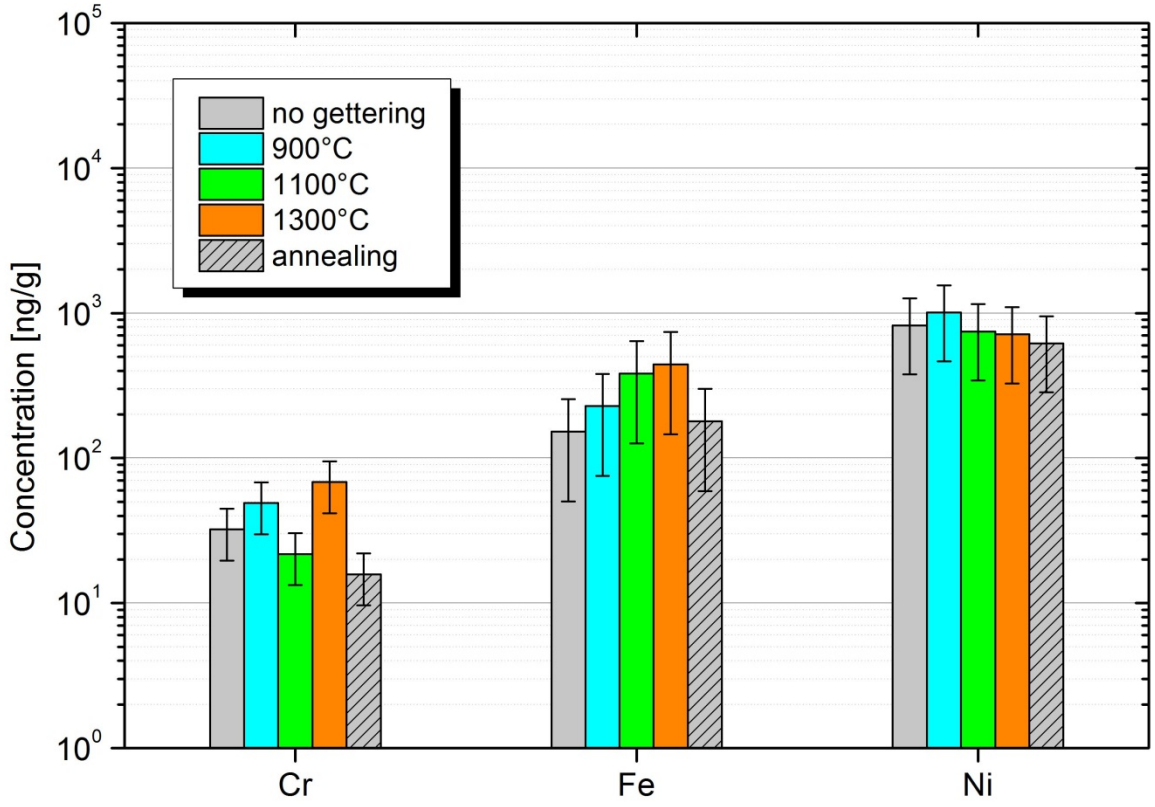

Fig. 5.3 Transition metal concentrations in neighboring wafers made from 99.995% UMG Si after HCl gettering at different temperatures measured by ICP-OES. Gettering was done with a concentration of 2% HCl in H_2 for 10 min. Annealing was done in H_2 at 1300°C for 10 min. Note that the error bars include not only the uncertainty of measurement but also the maximum deviation (d_{max}) defined and determined in section 3.3.

Furthermore, similar experiments were performed on neighboring wafers made from 99.97% UMG silicon. More samples were used to be able to apply a higher number of different gettering temperatures from 650°C to 1300°C. The gettering was again performed with a concentration of 2% HCl gas in H_2 for 10 minutes. Beside the reference wafers without gettering and with annealing, a reference wafer with P diffusion gettering was included. The results can be seen in Fig. 5.4. Again, a clear trend cannot be determined, but there is a slight indication that lower temperatures lead to better results than higher temperatures. A clear gettering effect can be seen for the wafer which was treated at 650°C. Gettering efficiencies of $\eta_{gett}(\mathrm{Cr}) = 4$ and $\eta_{gett}(\mathrm{Fe}) = 9$ can be calculated. High-temperature processing can introduce structural defects into the silicon material [130], which can serve as additional gettering sites for metals in competition with external gettering, as well as may introduce additional contaminants. However, in contrast to this, earlier experiments on the same 99.97% silicon material demonstrated that a temperature of 1300°C lead to rather high gettering efficiencies of $\eta_{gett}(\mathrm{Cr}) > 5$ and even $\eta_{gett}(\mathrm{Fe}) > 45$ [131]. In this work, the highest

gettering efficiencies of η_{gett}(Cr) = 25 and η_{gett}(Fe) = 47 are found only for the reference wafer treated by P diffusion gettering.

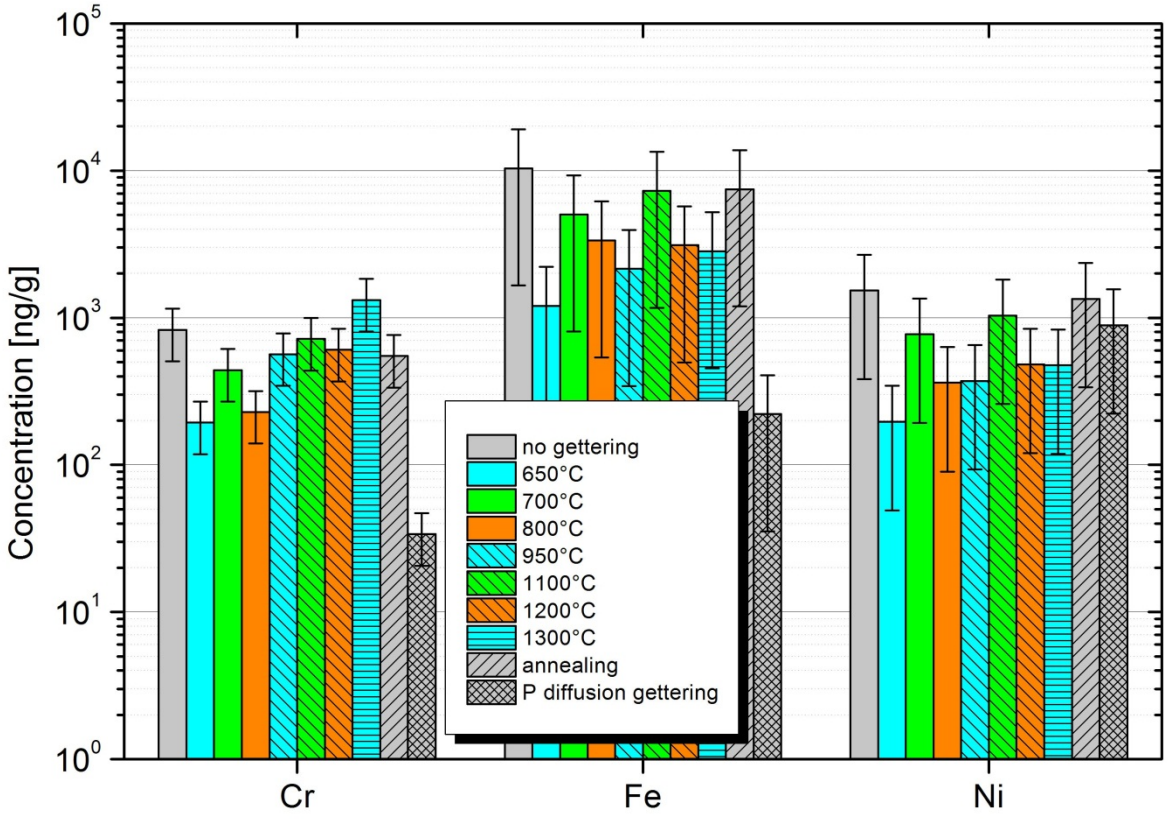

Fig. 5.4 Transition metal concentrations in neighboring wafers made from 99.97% UMG Si after HCl gettering at different temperatures measured by ICP-MS. Gettering was done with a concentration of 2% HCl in H_2 for 10 min. Annealing was done in H_2 at 1300°C for 10 min. Note that the error bars include not only the uncertainty of measurement but also the maximum deviation (d_{max}) defined and determined in section 3.3.

5.2.2 Variation of the time

Taking into account only the diffusion of impurities from the wafers bulk to the surface due to HCl gas gettering, increased gettering times should lead to decreased impurity concentrations. Experiments with HCl gas gettering for microelectronic silicon devices demonstrated, that after 16 hours much higher minority carrier lifetimes in silicon can be obtained compared to 1 hour gettering due to the removal of impurities [95]. However, the conditions are not comparable, as monocrystalline silicon instead of UMG silicon and a different gas mixture including O_2 instead of H_2 was applied.

In this work, gettering times of 10 – 180 minutes were applied, using a concentration of 2% HCl gas in H_2 at 900°C. On the one hand, the used temperature should not be too high,

because with increasing temperatures, an increased silicon etching rate (see section 3.2.2) would etch the whole silicon wafer in the case of long gettering times. On the other hand, the used temperature should not be too low to allow for moderately diffusing metals (e.g., Fe or Cr) to reach the surface. That is why a compromise was made choosing a temperature of 900°C.

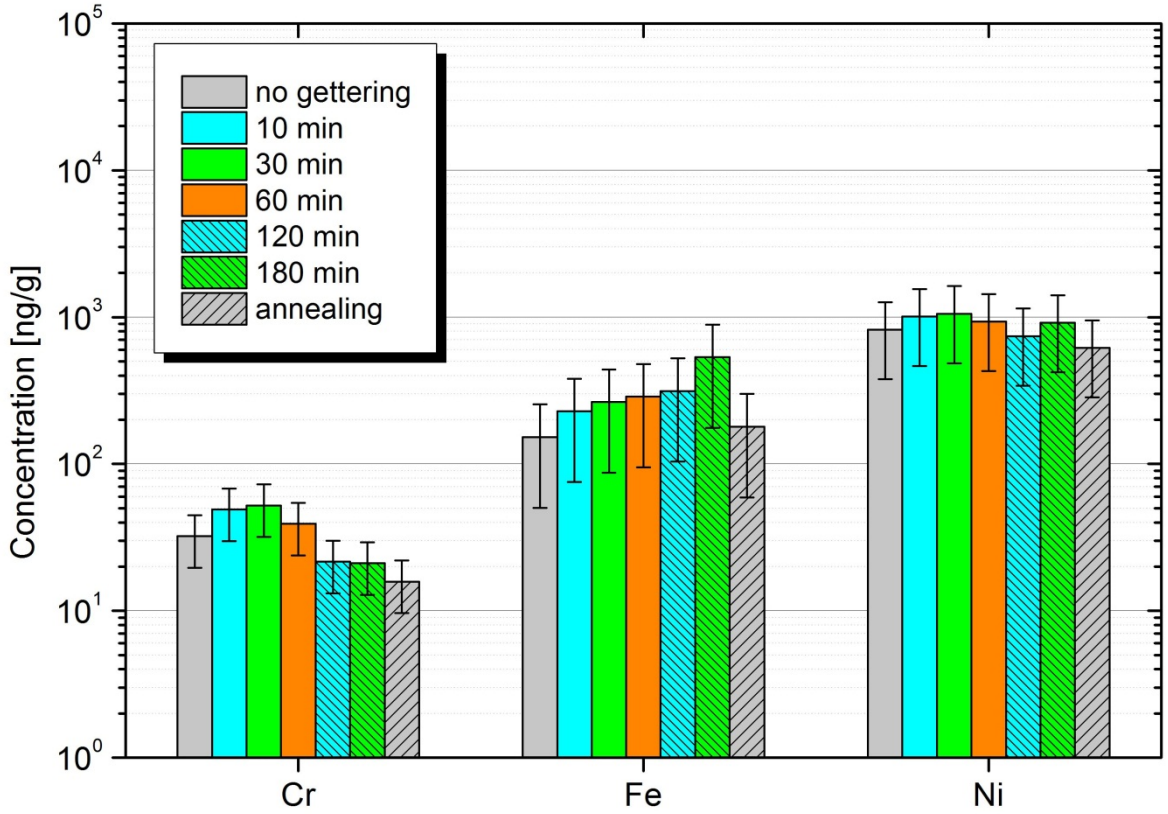

Fig. 5.5 Transition metal concentrations in neighboring wafers made from 99.995% UMG Si after HCl gettering with different gettering times measured by ICP-OES. Gettering was done with a concentration of 2% HCl in H_2 at 900°C. Annealing was done in H_2 at 1300°C for 10 min. Note that the error bars include not only the uncertainty of measurement but also the maximum deviation (d_{max}) defined and determined in section 3.3.

The results of the analysis for Cr, Fe, and Ni are presented in Fig. 5.5. Again, the general impurity level in this material is rather low and the high basic fluctuation of transition metal impurities in the 99.995% silicon material makes no clear trend visible. However, it was demonstrated on MG silicon wafers in section 5.1 that 30 minutes of HCl gas gettering show an improvement compared to only 5 minutes of gettering. This can be observed clearly at least in the case of Mn.

5.2.3 Variation of the HCl concentration

The HCl gas concentrations in H_2 were varied between 2% and 16%. Because of an increasing silicon etching rate with increasing HCl concentrations (see section 3.2.2) no concentrations higher than 16% were used. For the same reason, a relatively short gettering time of 10 minutes was applied, as it was demonstrated that conditions of 10% HCl in H_2 at 1200°C for 30 minutes already lead to etching of almost the complete UMG silicon wafer (see Fig. 5.6).

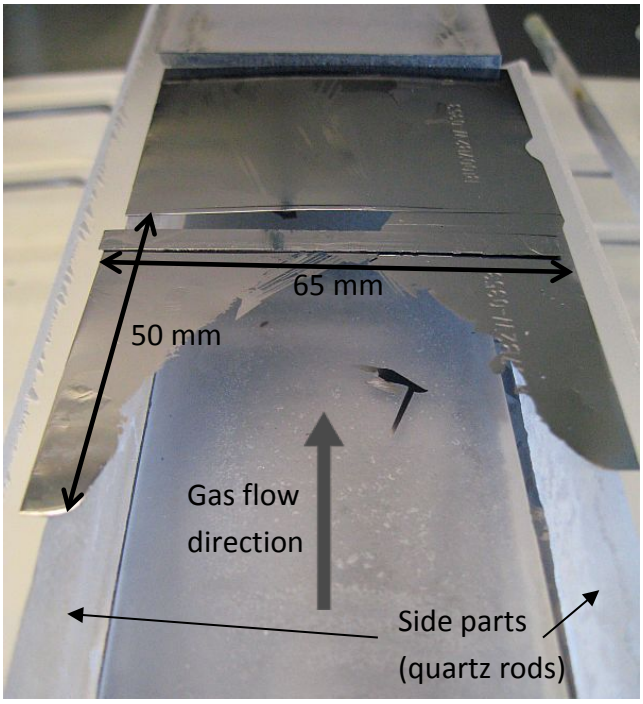

Fig. 5.6 Almost completely etched UMG silicon wafer after HCl gas gettering with 10% HCl in H_2 at 1200°C for 30 min in the RTCVD100 reactor. One can see the bottom and the side parts of quartz sample carrier with two 65x50 mm^2 sized wafers placed on top of the carrier as top wafer row (see Fig. 3.16). The gas flow is directed from the front towards the back. Thus, only the front wafer was strongly etched since the HCl concentration in the process gas decreases towards the back of the carrier due to the reaction with silicon.

Fig. 5.7 shows the results of HCl gas gettering with different HCl concentrations. The values of Cr indicate that lower HCl concentrations lead to better results. A concentration of 2% HCl in H_2 leads to a gettering efficiency of η_{gett}(Cr) = 17.2. The best results are demonstrated for both the annealed and the P gettered sample. The annealing was done in H_2 at 1300°C for 20 minutes. For the annealed sample, this result was not expected as it is not known that there is a gettering effect by H_2 annealing. P gettering though is well-known as a method to reduce the amount of transition metal impurities. The concentration of Cr was below the detection limit (DL) of 5 ng/g.

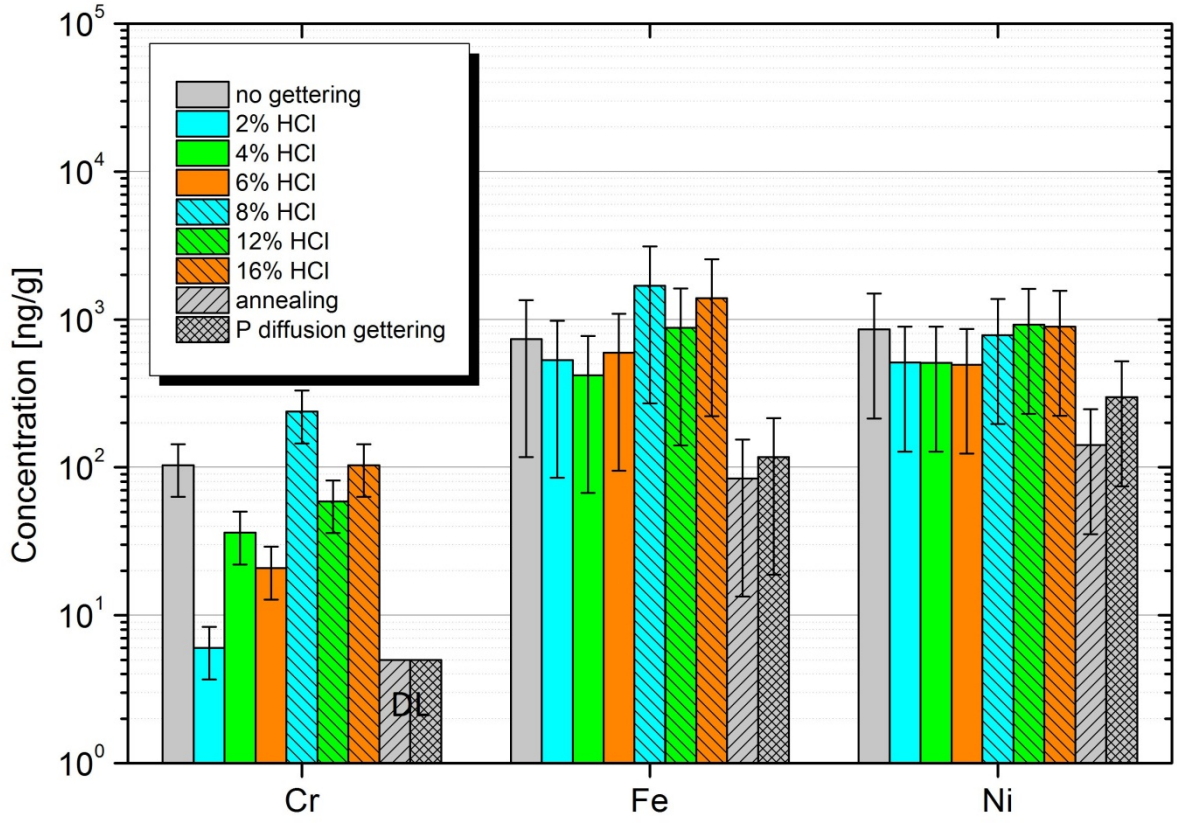

Fig. 5.7 Transition metal concentrations in neighboring wafers made from 99.97% UMG Si after HCl gettering with different HCl concentrations measured by ICP-OES. Gettering was done at 1300°C for 10 min. Annealing was done in H_2 at 1300°C for 20 min. Note that the error bars include not only the uncertainty of measurement but also the maximum deviation (d_{max}) defined and determined in section 3.3. The detection limit (DL) for Cr is 5 ng/g.

5.2.4 Gettering in the continuous reactor ConCVD

First HCl gas gettering experiments were done in the in-line CVD reactor ConCVD (Continuous Chemical Vapor Deposition), which was developed at *Fraunhofer ISE* [113]. UMG neighboring wafers, made from 99.97% silicon, were processed with ~ 1.4% HCl in a H_2 and Ar atmosphere at a temperature of 1180 – 1200°C for 30 minutes. Large-area wafers with a size of 156x156 mm^2 were used, which is the common size in the solar cell industry today. Although it is possible to run the process with a mobile carrier system (continuous), as usual for in-line processes, it was carried out stationary. The samples were weighed before and after the gettering to determine the silicon etching rate. Surprisingly, only a marginal difference in weight was found, which correlates to an etching rate of ≤ 0.01 µm/min. Unintentionally deposited small dark particles were observed on the surface of the silicon wafers after gettering (see Fig. 5.8). They are most probably particles based on C, which derive from the inner setup of the ConCVD, made from graphite. This was also

observed earlier in [132]. When growing epitaxial layers on the silicon substrate, these particles can cause crystal defects. Such defects can cause detrimental shunts in the further processed EpiWE solar cell.

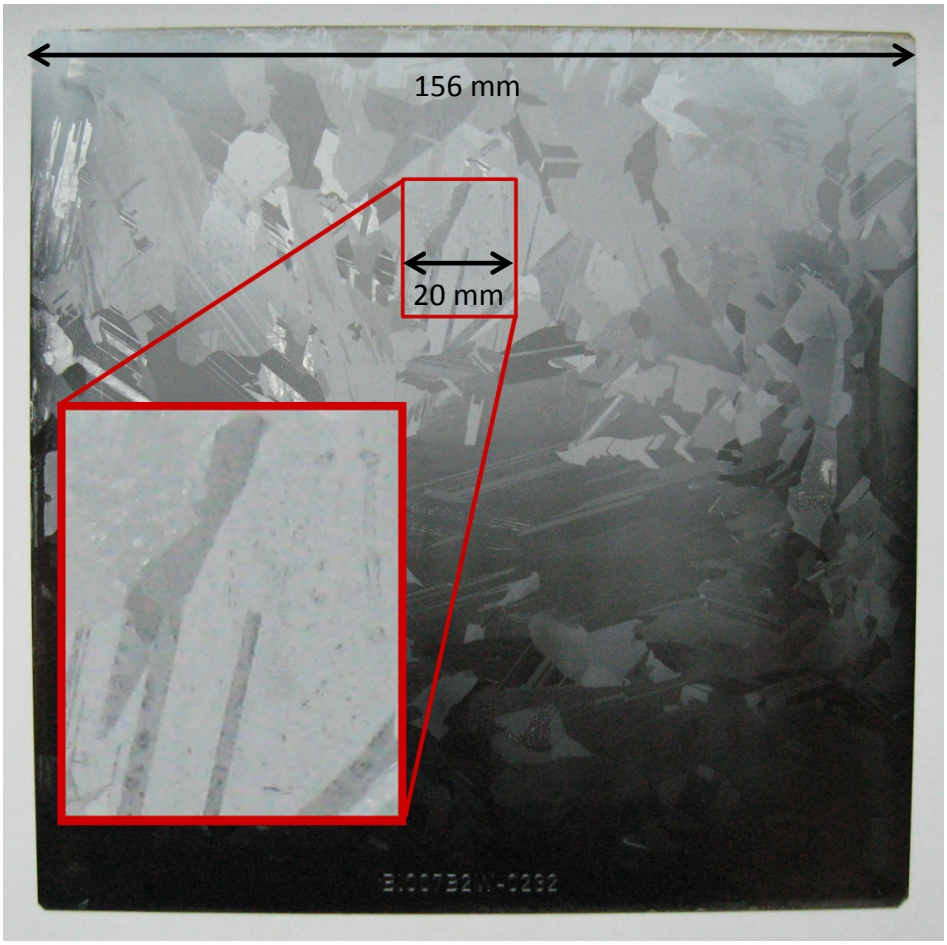

Fig. 5.8 Surface of a 156x156 mm^2 sized silicon wafer made from 99.97% UMG silicon. Small dark particles can be seen on the surface (marked area), most probably C based particles deriving from the graphite setup of the ConCVD.

Nevertheless, ICP-OES measurements were done on neighboring wafers with and without HCl gas gettering. The results, which are presented in Fig. 5.9, reveal that a gettering effect can be demonstrated for Cu and Co. In the case of Cu, an excellent gettering efficiency of η_{gett} = 98.9 was achieved. The Mn concentration after gettering was below the detection limit (DL) of 68 ng/g. In contrast to most results in the sections above, it could be demonstrated that higher temperatures and lower HCl concentrations can lead to high gettering efficiencies, at least for Cu and Co. These results show that HCl gas gettering can also be done in a continuous CVD reactor and is also applicable to large-area UMG silicon wafers.

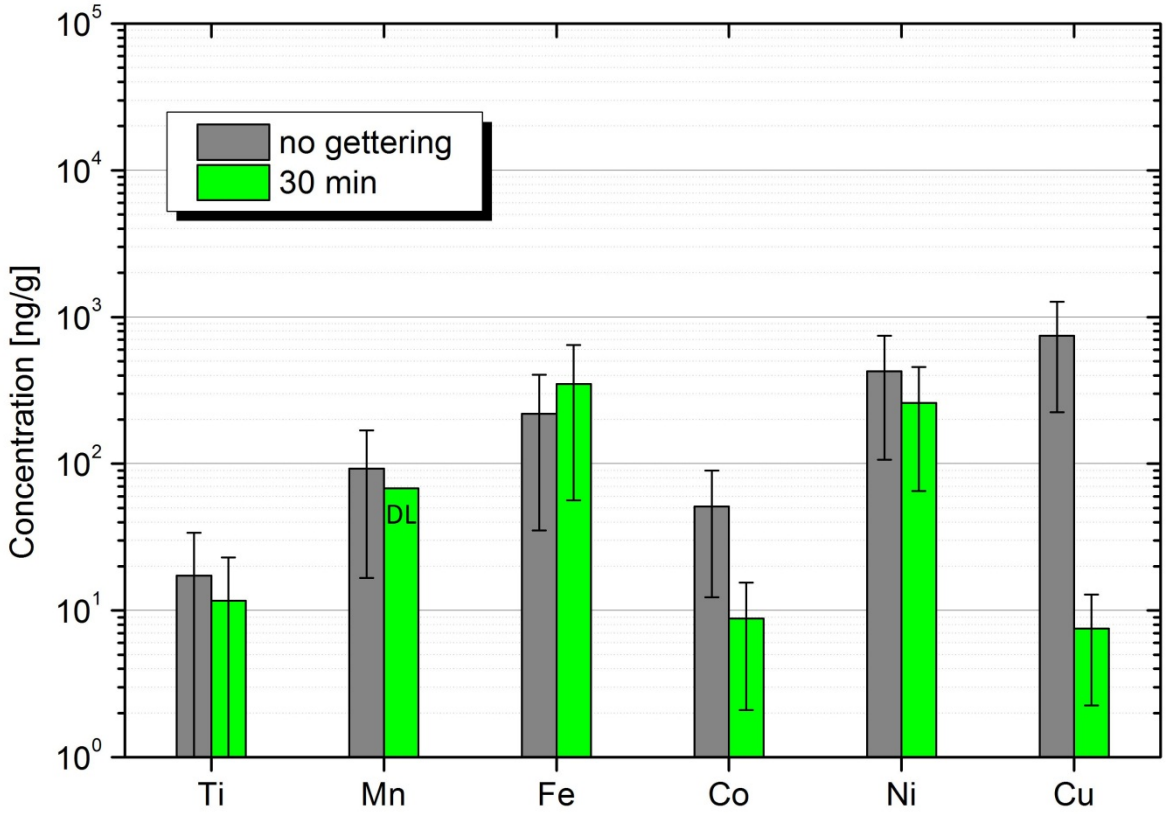

Fig. 5.9 Transition metal concentrations in neighboring wafers made from 99.97% UMG Si after HCl gettering in the ConCVD reactor measured by ICP-OES. Gettering was done with a concentration of ~ 1.4% HCl in H_2 and Ar at 1180-1200°C. Note that the error bars include not only the uncertainty of measurement but also the maximum deviation (d_{max}) defined and determined in chapter 3.3.

5.2.5 Summary of the highest gettering efficiencies

In contrast to the experiments of the sections 5.2.1, 5.2.2, and 5.2.3, where parameter variations were done using more than two neighboring wafers, many further HCl gas gettering experiments were done with two neighboring wafers without parameter variations and most often using 1300°C and 2% HCl. Some results for example are presented in [131], revealing that high gettering efficiencies can be achieved. A summary of the highest HCl gas gettering efficiencies for the most relevant transition metals is presented in Table 5.4.

Table 5.4 Highest gettering efficiencies achieved by HCl gettering on wafers made from 99.97% UMG Si measured by ICP-OES (DL = Detection Limit).

Element	without gettering [µg/g]	HCl gettering [µg/g]	gettering reduction r_{gett} [%]	gettering efficiency η_{gett}	Used gettering parameters
Cr	0.103 ± 0.040	0.006 ± 0.002	94	17.2	1300°C, 10 min, 2%
Mn	0.040 ± 0.002	< DL (0.01)	> 75	> 4	1300°C, 30 min, 2%
Fe	1.216 ± 0.039	< DL (0.027)	> 98	> 45	1300°C, 30 min, 2%
Co	0.051 ± 0.039	0.009 ± 0.006	82.8	5.8	1180-1200°C, 30 min, ~ 1.4%
Ni	1.531 ± 1.148	0.197 ± 0.148	87	7.8	650°C, 10 min, 2%
Cu	0.746 ± 0.522	0.007 ± 0.005	98.9	98.9	1180-1200°C, 30 min, ~ 1.4%

5.2.6 Discussion

The experiments with variation of the HCl gettering parameters, such as temperature, time, and HCl concentration, revealed that no clear trend can be observed. The reasons might be the large deviation of transition metal concentrations in neighboring wafers which are compared. The results can only be considered as significant when the differences are larger than the basic fluctuations in the material (represented by the error bars in the diagrams). Only one reference wafer without gettering was compared to 3 – 8 wafers with gettering in the experiments, although technically, only two neighboring wafers can be compared, as the maximum deviation d_{max} was obtained by comparing direct neighboring wafers. Not only the basic fluctuations of transition metal concentrations, but also the low concentration levels in the UMG materials make it difficult to detect trends in the analysis results, because silicon material of higher purity is more sensitive to the contamination background in the reactor during HCl gas gettering (see section 3.3.4).

Nevertheless, the results indicate, that lower HCl concentrations (~ 2% HCl in H_2) are advantageous. This is also beneficial for practical applications, as the silicon etching rate increases with increasing HCl gas concentration. Furthermore, a small hint was found, that a low temperature of 650°C lead to the best results. However, in contrast to this finding, earlier experiments showed high gettering efficiencies at 1300°C. This conflict leads to the conclusion that the optimum temperature depends on the element. Regarding the highest HCl gas gettering efficiencies summarized in Table 5.4 for each transition metal, it is obvious that Ni shows the highest gettering efficiency at 650°C, which leads to the conclusion that the gettering efficiency of fast diffusing elements (Ni and Cu) is not limited by the temperature, as compared to moderately diffusing elements (Cr, Mn, and Fe), which need

higher temperatures to reach sufficient diffusivities. Unfortunately, there are no analysis results for Cu at low temperatures available in this work. This conclusion will be further investigated by simulations in chapter 6. Due to above explained reasons, it could not be shown that higher gettering times lead to lower impurity levels. However, earlier experiments demonstrated that the gettering efficiency could be increased by increasing the gettering time from 10 minutes to 30 minutes.

Comparing all HCl gas gettering experiments, which were performed on the two UMG materials made from 99.995% and 99.97% silicon, it shows that higher gettering efficiencies can be reached on the 99.97% UMG wafers. However, only few experiments were performed with the 99.995% silicon and the statistics is weak. Furthermore, general metal concentrations are much lower in this material which makes it more sensitive to contaminations (see section 3.3.4).

The reasons why much varying results were obtained with HCl gas gettering may be explicable with the inhomogeneity of low-quality multicrystalline silicon material, such as MG and UMG. The research in the field of gettering for photovoltaic applications was concentrated on monocrystalline silicon in the beginning. While for FZ silicon it is common knowledge, that external gettering techniques, e.g., P gettering, are efficient, the gettering efficiency is reported to be ambiguous for multicrystalline silicon [108] [101] [133] [94]. It was found that external gettering has no efficiency in regions of high dislocation densities. Dislocations act as preferable precipitation sites for transition metal impurities, which in consequence do not respond to gettering. It was also reported, that high concentrations of O and C can limit the gettering efficiency. For example, an initial O concentration exceeding $6x10^{17}$ cm^{-3} in mc silicon lead to a decreasing diffusion length with increasing P gettering time. The reason was found to be O precipitates, which act as efficient internal gettering sites in competition with the external gettering [134]. Higher HCl gettering efficiencies were usually demonstrated on UMG compared to MG silicon wafers in this work, which indicates that the issues described above are more present in MG material, which in fact is expected to be the case.

5.3 Gettering for the standard wafer cell concept

HCl gas gettering is not only a suitable technique to improve EpiWE solar cells, but could also be advantageous to standard wafer solar cells made from UMG silicon. Note that UMG silicon wafers could also be used in the standard wafer cell concepts provided that the resistivity is sufficiently high ($> 0.1\ \Omega$cm), which means a moderate doping concentration and a sufficiently high overall purity (> 99.995%).

The purpose of gettering is the removal of impurities. However, the two cell concepts have different requirements on the electrical quality of the wafers after gettering. While in the EpiWE concept the highly doped low-cost wafer with a resistivity of typically < 0.1 Ωcm, which is treated by gettering, merely acts as a conductive substrate, in the standard wafer cell concept, the moderately doped wafer with a resistivity of typically around 1 Ωcm is electrically active. Therefore, in addition to an efficient removal of detrimental impurities, a high electrical quality of the wafer still after HCl gas gettering is crucial in the standard wafer cell concept. The minority carrier lifetime (see section 2.2.2) can be used to assess the efficiency of HCl gas gettering, at least qualitatively.

Wafers made from different types of silicon were used for HCl gas gettering experiments in two different reactors. In the RTCVD100 reactor mc wafers made from UMG and SoG silicon in the size of 65x50 mm^2 or 50x50 mm^2 were processed, whereas in an industrial-type diffusion furnace mc wafers made from SoG silicon in the size of 100x100 mm^2 were processed. The minority carrier lifetime was monitored with qualitative methods like Photoluminescence imaging (PLI) and quantitative methods like the quasi-steady-state photoconductance (QSSPC) method and the quasi-steady-state photoluminescence (QSSPL) calibrated PLI (see section 2.2.2). No element analysis was performed since the impurity levels were expected to be too low for a comfortable determination of transition metals, especially in the wafers made from SoG silicon.

5.3.1 Gettering in the lab-type RTCVD100 reactor

HCl gas gettering was performed on 99.999% UMG silicon wafers. The gettering was carried out using 2% HCl in H_2 for 30 minutes at a temperature of 1300°C. PLI was done on neighboring wafers with and without gettering to get comparable qualitative results of the minority carrier lifetime. For quantitative comparison, the lifetimes were measured by the QSSPC method. An average lifetime was measured on an area with the size of 12 – 14 cm^2 [41]. This area is marked green in Fig. 5.10, which presents PL images of wafers without (a) and with applied HCl gas gettering (b). The average lifetime results, which are displayed in the green marked area, might be surprising since the lifetime was expected to be increased by gettering due to the removal of metal impurities. However, it is decreased about one order of magnitude from 10.7 µs to 0.4 µs. The reason for that is the applied high temperature of 1300°C. It was reported, e.g., in [135], that a bulk lifetime degradation occurs in mc silicon for high-temperature processes. Two possible explanations are given for this effect, the dissociation of impurity precipitates due to high temperatures and the induced thermal stress at high temperatures coupled with existing strains in the crystal [130, 136]. The latter means that high-temperature processing can introduce structural defects into the material, which serve as additional gettering sites for metals in competition with

external gettering mechanisms. A decreased lifetime in UMG wafers due to annealing at high temperatures was also reported recently in [137], where it was shown that the minority carrier lifetime decreased with increasing annealing temperature. However, it was found that the dislocation density was also decreased by increasing temperature, which leads to the conclusion that rather not the introduction of structural defects is reducing the lifetime but probably high concentrations of interstitially dissolved metals and metallic nano-precipitates. Furthermore, high-temperature processes may introduce additional contaminants into the material. Note that the maximum temperature used in this work (1300°C) was even higher as compared to the respective experiments reported in literature.

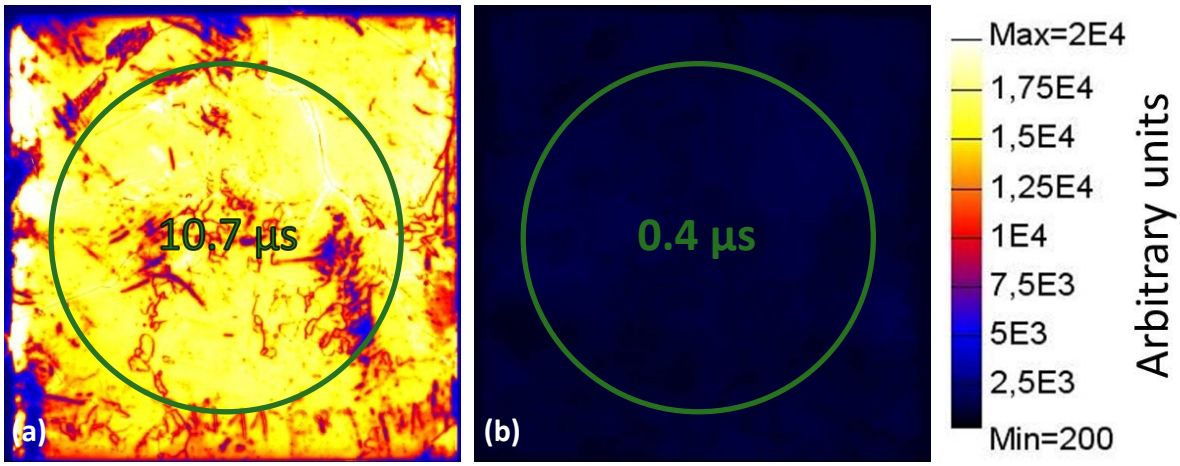

Fig. 5.10 Qualitative comparison of 50x50mm^2 sized UMG wafers without (a) and with HCl gettering (b) measured by photoluminescence imaging (PLI). The marked green circle is the area where minority carrier lifetime measurements were performed by means of quasi-steady-state photoconductance (QSSPC).

The correlation of high-temperature processes and low lifetimes was investigated by further QSSPC measurements on annealed p-type doped mc silicon neighboring wafers made from SoG silicon. A 50x50 mm^2 sized wafer with a resistivity of 0.61 Ωcm was annealed in H_2 atmosphere at 900°C for 15 minutes, while the neighboring wafer was not processed. QSSPC measurement results are presented in Table 5.5. Although the lifetime in the untreated wafer is lower as expected from SoG silicon material (probably due to a position near the very top of the ingot), a significant decrease in lifetime can still be demonstrated by this annealing experiment, even at a comparably moderate temperature of 900°C with an annealing time of 15 minutes.

To compare the conventional P diffusion gettering with HCl gas gettering regarding the minority carrier lifetime, further experiments were performed with 0.40 Ωcm p-type doped SoG silicon and 0.12 Ωcm p-type doped UMG wafers. HCl gettering was carried out with

2% HCl in H_2 at 820°C for 45 minutes, which are similar conditions as used for the P gettering. After gettering, the PSG layer and the emitter of the P gettering samples were etched back and the surfaces of all wafers including the HCl gettering samples were passivated by the deposition of silicon nitride/oxide layers. Thereby, it is assured that the recombination at the wafer surface is not limiting the minority carrier lifetime. Bulk lifetimes of the investigated materials were determined by means of QSSPL calibrated PLI. Space-resolved maps were obtained over a size of ~ 40x50 mm^2. In Fig. 5.11 the results of the SoG silicon wafers are presented. The lifetime map of the sample treated with P gettering (c) reveals areas of higher (~ 200 µs) and lower lifetimes (~ 20 µs). A harmonic mean value of $\tau_{harm} \approx 57.8 \pm 5.8$ µs was calculated for the whole sample area. The lifetime map of the sample treated with HCl gas gettering (d) reveals comparable low lifetimes over the whole sample area ($\tau_{harm} \approx 20.4 \pm 2.0$ µs). The mean lifetime of a neighboring wafer without gettering was measured (not shown) to be $\tau_{harm} \approx 35.2 \pm 3.5$ µs. That means that for P gettering a lifetime improvement could be demonstrated, whereas for HCl gas gettering a decrease in lifetime was observed. SoG silicon might be more sensitive to possible contamination sources during HCl gas gettering or sample preparation. This is why similar experiments were carried out for UMG silicon wafers.

Table 5.5 Minority carrier lifetimes in mc SoG silicon wafers with and without annealing measured by QSSPC.

Material	Resistivity [Ωcm]	Annealing	Minority carrier lifetime τ [µs]
SoG	0.6	(-)	3.7 ± 0.4
SoG	0.6	900°C, 15 min	0.3 ± 0.03

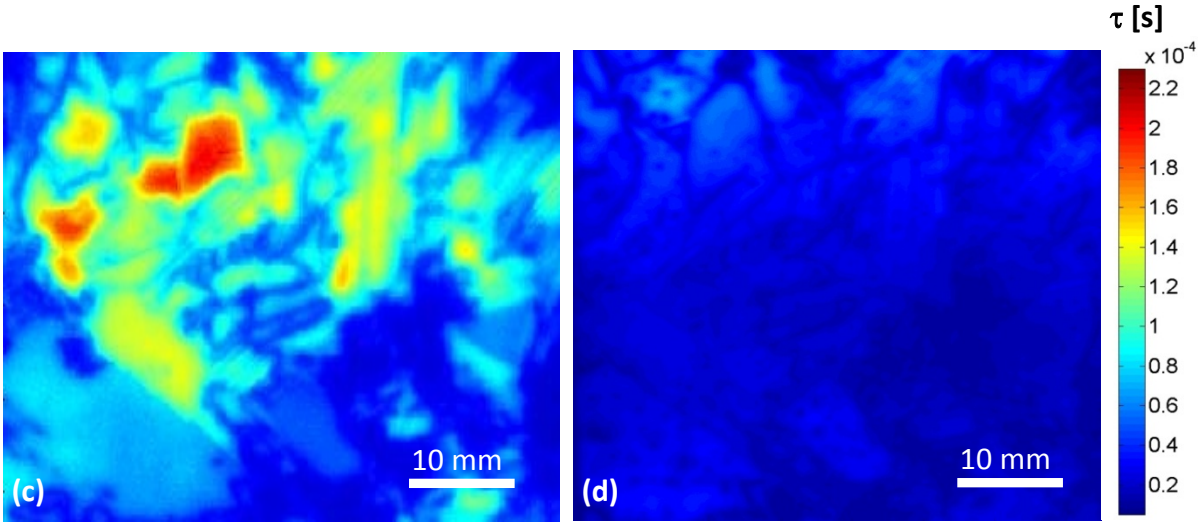

Fig. 5.11 Quantitative comparison of SoG silicon wafers with P diffusion gettering (c) and with HCl gettering (d) measured by QSSPL calibrated PLI.

In Fig. 5.12 the results of the gettering of the UMG silicon wafers are presented. The lifetime map of the sample treated with P gettering (e) again shows higher lifetimes ($\tau_{harm} \approx 4.1 \pm 0.4$ µs) than the sample treated with HCl gas gettering (f) ($\tau_{harm} \approx 2.6 \pm 0.3$ µs). The mean lifetime of an as-grown neighboring wafer without gettering was measured (not shown) to be $\tau_{harm} \approx 2.1 \pm 0.2$ µs. That means that, in contrast to the results for the SoG material, a slight improvement of the minority carrier lifetime by HCl gas gettering could be observed for the UMG material, although the increase in lifetime by P gettering is still stronger than by HCl gas gettering. P gettering is a more established technique, which has been optimized in terms of the gettering parameters for several years. To compare both gettering methods, the HCl gas gettering parameters like temperature, time, and HCl concentration were selected similar to P gettering in the presented experiments. The optimization of the HCl gettering parameters for the standard wafer cell concept is still to come, and the potential of increasing the gettering efficiency is expected to be high.

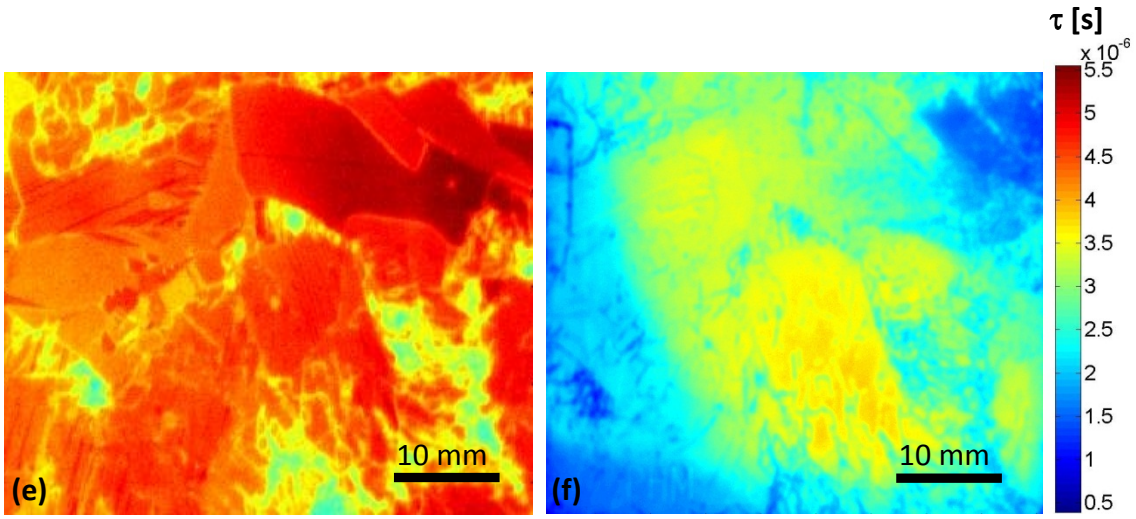

Fig. 5.12 Quantitative comparison of UMG wafers with P diffusion gettering (e) and with HCl gettering (f) measured by QSSPL calibrated PLI.

5.3.2 Gettering in an industrial-type diffusion furnace

HCl gas gettering could be advantageous for wafer solar cells as gettering step prior to the P diffusion. To investigate the potential of such in-situ HCl gettering, an industrial-type P diffusion furnace was prepared with a HCl gas supply. This enables to process standard wafer solar cells with an additional HCl gettering step. However, the sample carrier system is different to the setup of the RTCVD100 reactor which was used for most gettering processes in this work. As described in 3.3.3, the wafers are put in parallel direction with the gas flow in the RTCVD100, whereas in the diffusion furnace the wafers are put in vertical direction to

the gas flow (see Fig. 5.13). With the latter setup, a much higher throughput of wafers can be realized, as well as larger sample sizes can be used (e.g., 100x100 mm^2 or 156x156 mm^2). Another difference is that H_2 gas is not available in the diffusion furnace, which is why N_2 was used as carrier gas for HCl.

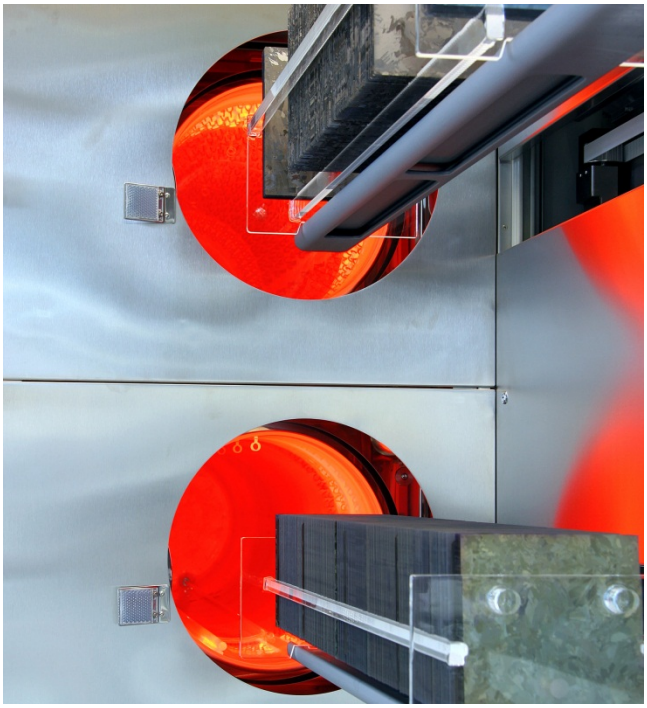

Fig. 5.13 Industrial-type diffusion furnace, which is loaded with 156x156 mm^2 sized mc silicon wafers (© *Fraunhofer ISE*).

First processes in an industrial-type diffusion furnace were performed applying HCl gas gettering, P gettering, and a combination of both techniques. Subsequent minority carrier lifetime measurements were done by the QSSPC method to compare the effect of HCl gas gettering with the conventional P gettering. Neighboring mc silicon wafers made from SoG silicon in the size of 100x100 mm^2 with a thickness of ~ 350 µm and a resistivity of ~ 1 Ωcm were used. The wafers were taken from the very bottom of the ingot, where in general higher impurity contents are present than in the middle of the ingot. For all HCl gas gettering processes, a concentration of 5% HCl in N_2 was used, and a temperature of 850°C and a gettering time of 45 minutes were applied.

In previous experiments, it was demonstrated that the P emitter sheet resistance is not influenced by a prior HCl gas gettering step. Thus, similar emitter profiles are expected for all process variations. Experiments were carried out with four different process variations, which are, HCl gas gettering with subsequent wet-chemical CP etching (A), HCl gas gettering without etching (B), P gettering (C), and consecutive HCl gas gettering with P gettering (D).

For process (A) 5 µm of the silicon surface was removed by CP etching solution after HCl gas gettering. This process variation was included to investigate the influence of contaminants or surface-near impurities after HCl gas gettering, which are removed obligatory in the P gettering by wet-chemical etching of the PSG layer. The P gettering (C) consists of the P diffusion with subsequent PSG and emitter etching. The process (D) includes HCl gettering with additional P gettering, again including PSG and emitter etching. Some unprocessed wafers were measured by QSSPC to compare the minority carrier lifetimes. The results of all wafers are summarized in Table 5.6. The wafer number indicates the position in the ingot starting from the bottom upwards.

Table 5.6 Minority carrier lifetimes in mc silicon wafers made from SoG silicon without process and with different applied gettering processes (A – D) measured by QSSPC.

Wafer No. / Position	Process	Minority carrier lifetime τ [µs]
2	-	4.7 ± 0.5
3	HCl gettering + CP etching (A)	10.1 ± 1.0
4	HCl gettering (B)	15.0 ± 1.5
5	P gettering (C)	18.2 ± 1.8
6	HCl gettering + P gettering (D)	18.6 ± 1.9
10	-	5.9 ± 0.6
12	HCl gettering + CP etching (A)	25.4 ± 2.5
13	HCl gettering (B)	21.3 ± 2.1
14	P gettering (C)	22.5 ± 2.3
15	HCl gettering + P gettering (D)	22.7 ± 2.3
19	-	18.3 ± 1.8
20	HCl gettering + CP etching (A)	28.8 ± 2.9
22	HCl gettering (B)	28.6 ± 2.9
23	P gettering (C)	25.8 ± 2.6
24	HCl gettering + P gettering (D)	23.1 ± 2.3
28	-	35.4 ± 3.5

Regarding the results of only the unprocessed wafers, an increase of the lifetime from the bottom upwards is noticeable. This increase is explicable, as impurities from the crucible diffuse into the bottom of the ingot forming recombination sites, which reduces the bulk lifetime in the wafers. This is why the lifetime of unprocessed wafers increases with increasing wafer number. This effect makes it necessary to interpret the results carefully. It

is reasonable to compare the lifetime values of the four types of processes (A – D) with the respective unprocessed lifetime value of a higher position.

It can be concluded that all gettering processes show a positive effect on the lifetime. Also for the wafer no. 20 – 24, where the highest value is found for the unprocessed wafer no. 28, an improvement is indicated, at least for the HCl gas gettering (no. 20 and 22). Comparing the different gettering processes, HCl gettering (A and B) leads to similar or even higher lifetimes than processes with P gettering (C and D). Only for wafers no. 3 – 6 this is not the case. In general, an improvement by CP etching (A) compared to (B) cannot be found. In the case of no. 12, CP etching gives an improvement, in the case of no. 20, the lifetime is unchanged. It is not clear, why wafer No. 3 including CP etching ends up with a lower lifetime than no. 4 (without CP etching), because CP etching is expected to lead to lower or at least unchanged impurity concentrations. One possible explanation is that at positions very close to the bottom, where a high number of nucleation sites lead to small grain sizes at the beginning of the ingot crystallization [138], the grain structure might be varying to some extent even between direct neighboring wafers and the lifetime is mainly limited not by impurity defects but by the high number of other crystal defects like grain boundaries.

5.3.3 Discussion

The application of HCl gas gettering to the standard wafer solar cell concept requires a focus on the electrical quality of the wafer after gettering. In contrast to the electrically inactive highly-doped silicon wafers which are used as substrates in the EpiWE cell concept, minority carrier lifetime measurements are feasible to assess the electrical quality after gettering. Because the lifetime in a mc silicon wafer is decreased already through simple annealing processes at high temperatures, probably due to the dissociation of metallic precipitates, it is only reasonable to compare the lifetime of the wafer after gettering to the lifetime of an annealed neighboring wafer. In case no annealed neighboring wafer was available, a relative comparison between P gettering and HCl gettering is presented. Nevertheless, if the lifetime after gettering is higher as compared to the lifetime without any treatment (as-grown wafer), the gettering effect is proven.

A slight improvement of the lifetime by HCl gas gettering in the RTCVD100 could be demonstrated in an UMG silicon wafer by comparison to the lifetime of the as-grown wafer. First HCl gas gettering processes in an industrial-type diffusion furnace revealed that similar or even higher lifetimes are achievable as compared to P gettering. This is a promising result, as HCl gas gettering is a simple and cost-efficient process and could be easily applied to industrial-type furnaces. It is also possible to apply a combination of both gettering techniques. An optimization of the HCl gas gettering parameters for the standard wafer cell concept should be done, which should further increase the gettering efficiency.

5.4 Solar cell results

Solar cells with and without HCl gas gettering were processed for both cell concepts. The conditions which were applied to both cell concepts, if not otherwise indicated, are summarized in Table 5.7.

The effect of HCl gettering was not only tested on EpiWE cells with the conventional diffused $POCl_3$ emitter, but also on EpiWE cell structures with an alternative emitter, the heterojunction emitter. These structures were not processed with the same steps as the EpiWE cells with diffused emitter. The differences will be described in section 5.4.3. The cell results without gettering are compared to the cell results with applied HCl gas gettering. For the standard wafer cell concept in addition a combination of HCl and P gettering was applied to some cells, which could also be compared to cells with and without HCl gettering.

Table 5.7 Overview of applied conditions for both used solar cell concepts.

	EpiWE cell concept	**Standard wafer cell concept**
Silicon material	MG, UMG (as substrate)	SoG
Gettering temperature	1300°C	850°C
Gettering time	30 min	45 min
HCl gas concentration	2% in H_2	5% in N_2
Reactor	RTCVD100	Industrial-type diffusion furnace
Cell process	Simplified clean room process (see section 2.1.3)	High-efficiency clean room process (see section 2.1.2)
Cell size	50x50 mm^2	100x100 mm^2

5.4.1 EpiWE solar cells on MG silicon substrates

Although it was concluded in 5.1.4, that the metal concentrations in the presented MG silicon wafers after HCl gas gettering are still too high for cells with high performances, EpiWE cells were processed on MG silicon substrates to evaluate the most crucial issues of processing low-cost substrates. It was done in the frame of the EU project ‘ThinSi’ [139] in

cooperation between several partners of the consortium. The substrates were processed, starting from a highly doped MG silicon powder delivered by *Elkem Solar AS (Norway)*, ingot casting at *SINTEF* (Norway) and wafering at the *Fraunhofer ISE*. An excerpt of the specification of the feedstock and the impurity analysis of the resulted wafers made by means of X-ray fluorescence spectroscopy (XRF) at *IMEC* (Belgium) is given in Table 5.8. Extremely high transition metal concentrations are still present in the wafers, although generally it is expected that they are reduced by segregation during the crystallization step. The concentrations in the wafers are even higher than in the MG silicon substrates, which were presented in section 5.1.

Table 5.8 Transition metal concentrations in MG silicon powder (supplier's specification) and in the wafers measured by XRF at *IMEC* (Belgium).

Element	concentration in MG powder [µg/g]	concentration in wafer [µg/g]
Ti	1.6	8
Cr	3.6	3 – 7
Mn	2.3	7
Fe	150	(108 – 170)*
Ni	2.0	14

* Fe was only detected in 1 out of 4 measured samples

Instead of 30 minutes, the HCl gas gettering was only carried out 15 minutes at 1300°C, because of a relatively low thickness of the substrates. Gettering times of more than 15 minutes resulted in brittle samples, which would lead to a high breakage rate in the subsequent solar cell processing.

After the epitaxial deposition many silicon whiskers could be seen on the surface of the deposited silicon layers. Whiskers are little 'wires', which grow out of the silicon surface. The growth of whiskers is catalyzed by metals, e.g., Fe [140] and Au [141], during the one-directional growth by CVD [142]. It can be explained by the vapor-liquid-solid (VLS) mechanism [143] [144]. The catalyst forms an eutectic phase with silicon. This phase is liquid at temperatures higher than the eutectic temperature, which is around 1200°C for Fe [145]. At temperatures above 1200°C a liquid droplet is formed, which acts as a preferred site for the deposition of silicon from the vapor. The liquid becomes supersaturated with Si and the whisker grows out of the droplet by precipitation of Si. Whiskers can be harmful to solar cells as they shunt the p-n junction and should therefore be avoided during the epitaxial silicon growth.

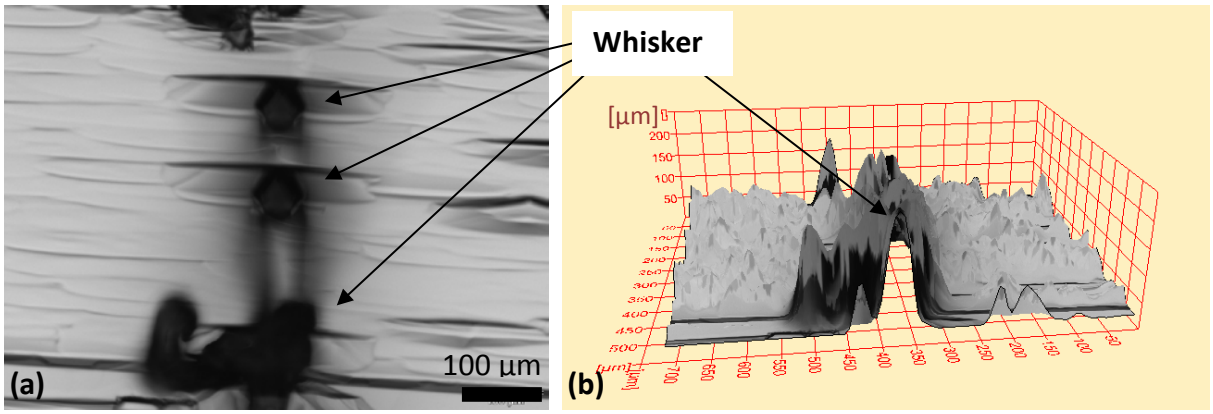

Fig. 5.14 Microscope top view (a) and 3D morphology side view (b) of a Si surface with whiskers growing out of the surface up to 250 µm.

Whiskers could be seen on MG substrates both with and without gettering after the epitaxial silicon deposition. Samples with gettering even showed a higher density of whiskers. This fact was observed before and is due to a longer high-temperature treatment in case of the substrates with HCl gas gettering, whereby metals diffuse out of large precipitates and many distributed smaller precipitates can form nucleation sites for whiskers [18]. Fig. 5.14 shows a microscope image and a 3D morphology side view image of whiskers, which are growing out of the silicon surface. The whiskers have lengths up to 250 µm.

Table 5.9 EpiWE solar cell results on MG Si substrates without (-) and with (+) HCl gettering. The most relevant solar cell parameters are given: V_{OC} = open circuit voltage; J_{SC} = short circuit current; *FF* = fill factor; η_{cell} = cell efficiency (see section 2.1.2).

Substrate material	Number of cells	HCl gettering	V_{OC} [mV]	J_{SC} [mA/cm^2]	*FF* [%]	η_{cell} [%]
MG Si	2	(-)	315 ± 149	21.9 ± 1.1	33.6 ± 7.0	2.6 ± 1.7
MG Si	4	(+)	188 ± 104	19.9 ± 0.6	27.8 ± 3.0	1.1 ± 0.8
Cz Si	2	(-)	600 ± 8	25.0 ± 0.9	64.8 ± 2.7	9.7 ± 0.9

Nevertheless, some EpiWE solar cells were processed. Substrates without or with only a few whiskers visible were chosen for the solar cell fabrication. The *I-V* measurement results are shown in Table 5.9. All cell parameters of the cells on MG silicon substrates are inferior compared to the reference monocrystalline Cz silicon substrate cells. This is due to metallic impurities which are located in the space charge region of the p-n junction and cause recombination of generated electron-hole pairs. That is why the open circuit voltage (V_{OC}) and the fill factor (*FF*) are severely decreased. Cell parameters on MG silicon substrates, which were treated by HCl gas gettering, are even worse than cells without gettering. The

reason is the higher density of whiskers which were observed especially for samples with applied gettering. As mentioned before, high amounts of impurities can initiate the growth of whiskers during the epitaxy, which causes shunts in the later solar cell and decrease the parallel resistance and therefore the *FF*. It must be noted that even the reference Cz substrate cell results are not as good as typically. The best cell efficiencies for EpiWE solar cells with an epitaxial layer thickness of 20 – 30 µm on highly doped Cz substrates reported at ISE are above 16% [146]. This discrepancy can be explained by two reasons: Firstly, as mentioned above, a simplified cell process with a 80 Ω/sq emitter without passivation and a directly evaporated front grid was chosen instead of a 120 Ω/sq emitter with oxide passivation and a photolithographically designed grid in order not to harm the photolithography masks by the whiskers. Secondly, the enormous amounts of impurities, which are present in the MG substrates, are also able to contaminate the Cz substrates through gaseous metal compounds formed during the $POCl_3$ emitter diffusion and lead to degradation of the cell performance, since all samples were treated simultaneously in shared carriers for both wet-chemical and high-temperature processes.

It can be concluded that high amounts of metallic impurities in MG silicon wafers lead to whisker formation during the epitaxial growth. HCl gas gettering even intensifies this effect due to the high-temperature treatment, leading to an increased dissociation of large metal precipitates and finally to many distributed smaller precipitates. On the surface they initiate the growth of silicon whiskers. This effect then exceeds the gettering effect during HCl gas gettering. It means that the impurity level in the investigated MG silicon substrates is too high to fabricate EpiWE solar cells, at least for lack of a diffusion barrier between the substrate and the epitaxial silicon layer. To obtain EpiWE solar cells with acceptable performances, less impure substrates should be used, such as UMG silicon substrates. EpiWE solar cell results on UMG silicon substrates are described in the following sections.

5.4.2 EpiWE solar cells on UMG silicon substrates

EpiWE solar cell results on UMG silicon substrates made from 99.97% silicon are presented in this section. Firstly, EpiWE cell results are shown with applied P gettering as reference. Secondly, EpiWE cell results with applied HCl gas gettering are shown and compared with the first results. For all cells a conventional diffused emitter was applied, in contrast to the following section 5.4.3, where a heterojunction emitter is applied.

P gettering

P gettering was performed using $POCl_3$ at 900°C for 1 hour with the obligatory subsequent wet-chemical etching of the formed phosphosilicate glass (PSG) layer and the P diffused emitter. *I-V* cell parameters of the EpiWE cells with and without P diffusion gettering are

given in Table 5.10. All parameters are low as compared to the reference EpiWE cell on Cz silicon substrate. Especially the fill factor (*FF*) is extremely low. Some parameters of the two-diode model of the solar cell, I_{01}, I_{02}, R_S and R_P, were determined by measuring the dark *I-V* curves, which revealed that the *FF* is mainly reduced because of a comparably low parallel resistance R_P and a high dark saturation current density I_{02}. Thermography measurements revealed that there are shunts present in most cells, which are probably responsible for the low R_P values. Impurities, which diffuse into the space-charge region during the high temperature processes, can form traps for generated carriers, which not only reduces the *FF* but also the open circuit voltage V_{OC}. By gettering, a certain amount of impurities is removed from the substrate, which leads to a less contaminated electrically active epitaxial layer and to higher V_{OC} values of the cell. Thus, an average increase of ~ 47 mV was demonstrated. Also parameters like the J_{SC} and the *FF* were improved, altogether leading to an increase of the cell efficiency by ~ 17% (relative) and by ~ 1.2% (absolute).

Table 5.10 EpiWE solar cell results on 99.97% UMG silicon substrates without (-) and with P diffusion gettering (+). The most relevant solar cell parameters are given: V_{OC} = open circuit voltage; J_{SC} = short circuit current; *FF* = fill factor; η_{cell} = cell efficiency (see section 2.1.2). The uncertainty of a single measurement can be given as: V_{OC} ~ 0.5%; J_{SC} ~ 2.5%; *FF* ~ 1% (rel.); η ~ 2.9% (rel.).

Substrate material	Number of cells	P diffusion gettering	V_{OC} [mV]	J_{SC} [mA/cm^2]	*FF* [%]	η_{cell} [%]
UMG Si	7	(-)	520 ± 30	21.3 ± 1.5	50.7 ± 6.9	5.7 ± 1.2
UMG Si	7	(+)	567 ± 17	24.7 ± 0.8	49.0 ± 6.1	6.9 ± 1.2
Cz Si	1	(-)	608	25.9	70.9	11.1
Cz Si	1	(+)	612	26.0	71.0	11.3

To get an indication what concentrations of impurities were removed, AAS measurements were done for Fe on two neighboring wafers with and without P diffusion gettering. The results are presented in

Table 5.11. It revealed that the Fe concentration was 6 times lower after gettering. The P gettering efficiency for Fe matches with typical values reported in the literature [125], where INAA analyses of low-contaminated mc silicon before and after P diffusion gettering were reported and metal contamination levels could be reduced by 60 - 90%, corresponding to gettering efficiencies of 2 – 10.

Table 5.11 Fe concentration of UMG neighboring wafers made from 99.97% silicon without and with P gettering measured by AAS.

Element	without gettering [ng/g]	P diffusion gettering [ng/g]	gettering reduction r_{gett} [%]	gettering efficiency η_{gett}
Fe	3150 ± 90	490 ± 30	84	6.4

Furthermore, electroluminescence (EL) measurements (see section 2.2.3) were performed on cells with and without P diffusion gettering to demonstrate the improvement by gettering on a visual qualitative level. Fig. 5.15 shows EL images of two EpiWE cells without (a) and with applied P gettering (b). A forward bias is applied to the cells, which leads to radiative recombination of charge carriers. Dark areas are dominated by nonradiative recombination mechanisms like Shockley-Read-Hall (SRH) recombination (see section 3.1.3), which is due to a higher amount of recombination active impurities like transition metals. For this reason dark areas can especially be observed for the cell without gettering.

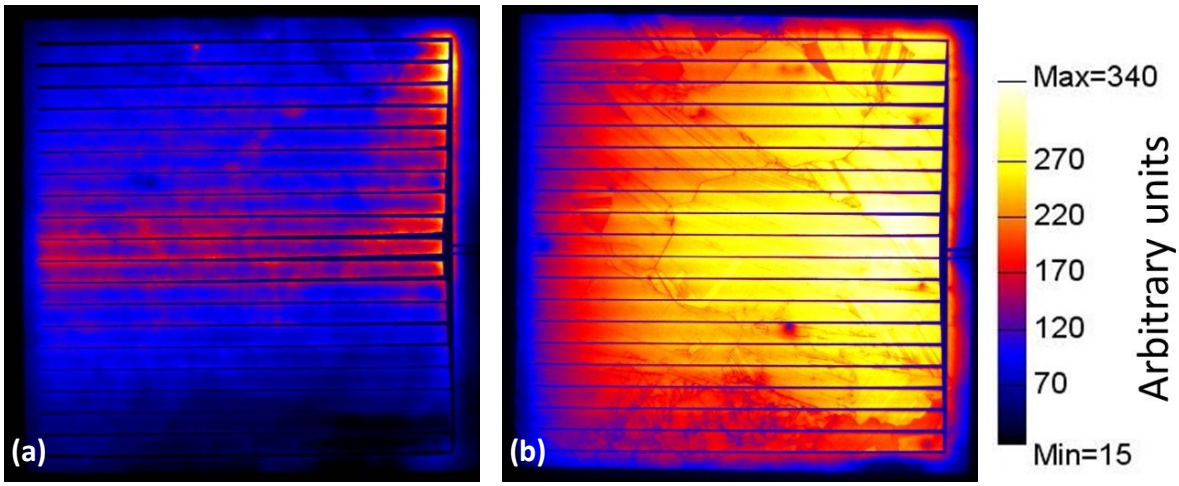

Fig. 5.15 Electroluminescence images (qualitative) of 50x50 mm^2 sized EpiWE cells on 99.97% UMG silicon substrates without (a) and with P diffusion gettering (b).

HCl gas gettering

The same EpiWE cells as presented above were processed, this time replacing P gettering by HCl gas gettering. *I-V* cell parameters of the EpiWE cells with and without HCl gas gettering are given in Table 5.12. It is shown that also HCl gas gettering primarily increases the V_{OC} of EpiWE cells. An average increase of ~ 64 mV is demonstrated. Also parameters like the J_{SC} and the *FF* are improved, altogether leading to an increase of the cell efficiency

by ~ 25% (relative) and by ~ 2% (absolute). The best cell with HCl gas gettering shows a conversion efficiency of 11.1%. Compared to cells with P gettering similar or even stronger improvements are achieved with HCl gas gettering.

ICP-OES measurements were done to assess the HCl gettering efficiency. Fe could be reduced by a factor of ~ 2.2 (see Table 5.13). The gettering efficiency is lower as compared to P gettering results in the previous section. However, only single neighboring wafers to the EpiWE cell substrates were available for analysis, and thus the statistics of the presented analysis results are weak. Furthermore, only Fe concentrations are given, whereas the results of the cell performance include the gettering efficiency of all impurities which can be reduced in the substrate by gettering.

Table 5.12 EpiWE solar cell results on 99.97% UMG silicon substrates without (-) and with HCl gettering (+). The most relevant solar cell parameters are given: V_{OC} = open circuit voltage; J_{SC} = short circuit current; *FF* = fill factor; η_{cell} = cell efficiency (see section 2.1.2). The uncertainty of a single measurement can be given as: V_{OC} ~ 0.5%; J_{SC} ~ 2.5%; *FF* ~ 1% (rel.); η ~ 2.9% (rel.).

Substrate material	Number of cells	HCl gas gettering	V_{OC} [mV]	J_{SC} [mA/cm^2]	*FF* [%]	η_{cell} [%]
UMG Si	7	(-)	501 ± 24	23.6 ± 0.3	63.7 ± 2.2	7.5 ± 0.6
UMG Si	8	(+)	565 ± 28	24.8 ± 0.4	66.8 ± 4.2	9.4 ± 1.1
UMG Si	Best cell	(+)	590	25.3	74.4	11.1

Table 5.13 Fe concentration of UMG neighboring wafers made from 99.97% silicon without and with HCl gettering measured by ICP-OES.

Element	without gettering [ng/g]	HCl gas gettering [ng/g]	gettering reduction r_{gett} [%]	gettering efficiency η_{gett}
Fe	1370 ± 109	610 ± 49	55	2.2

Electroluminescence (EL) measurements were performed on cells with and without HCl gas gettering, just as shown above for the P gettering to demonstrate the improvement by gettering qualitatively. Similarly, nonradiative recombination mechanisms are primarily observed for the EpiWE cell without HCl gettering (see Fig. 5.16). By comparing the EL images with an unprocessed neighboring wafer (see Fig. 5.17), the same grain structure can be identified quite well in some parts of the EL images. It is noticed that certain grains or regions are especially improved while other regions are obviously less affected by gettering. Moreover, there are regions (for example the area marked by a black circle), which are generally improved but exhibit smaller regions of low improvement. These are likely regions of high dislocation densities where large numbers of precipitates are located, probably also

containing metal oxide species, which can hardly be dissociated or removed during gettering.

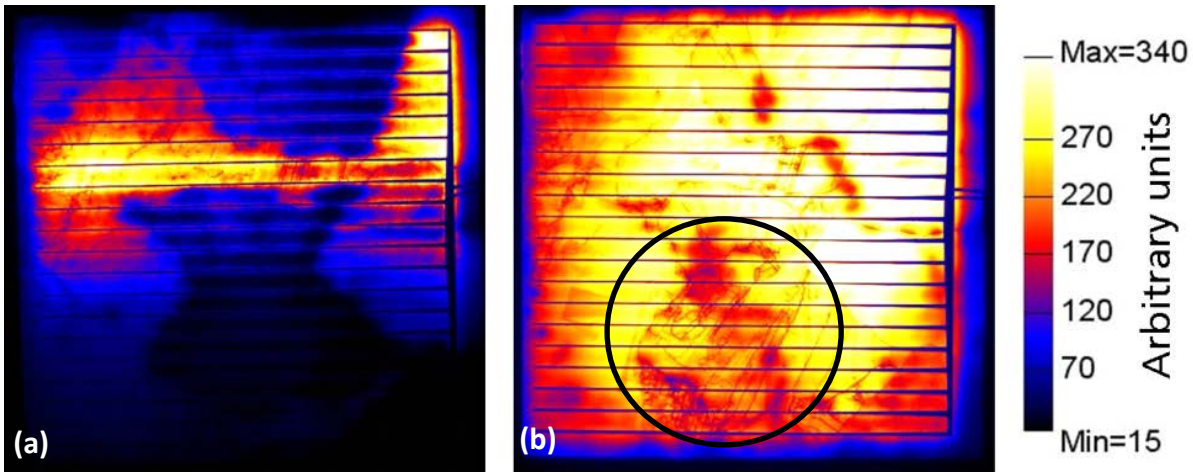

Fig. 5.16 Electroluminescence images (qualitative) of 50x50 mm^2 sized EpiWE cells on 99.97% UMG silicon substrates without (a) and with HCl gettering (b). The marked black circle is likely an area of high dislocation densities.

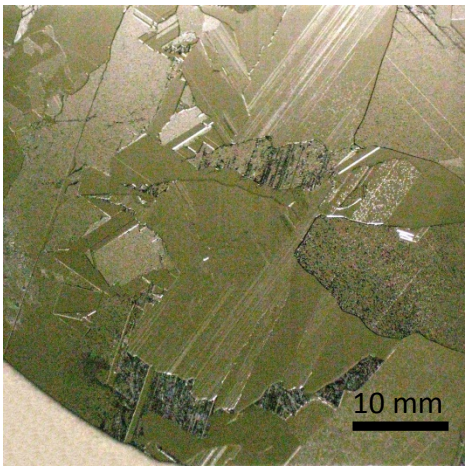

Fig. 5.17 Photograph of a neighboring wafer of the EpiWE cells presented in Fig. 5.16. The wafer was broken in the bottom left corner and thus was not further processed to an EpiWE cell. Some parts of the grain structure can be identified in Fig. 5.16(a).

In Fig. 5.18 the spectrally resolved internal quantum efficiencies (IQE) (see section 2.2.3) are presented for EpiWE cells on UMG silicon substrates with and without HCl gas gettering, for an EpiWE cell on reference mono-c Cz silicon substrate, and for a standard wafer solar cell made from a mono-c FZ silicon wafer. For a better comparison, both types of cells were processed using the same high-efficiency clean room process, which is presented in section 2.1.2 for the standard wafer cell concept. For all wavelengths, the IQE is higher in the UMG EpiWE cell with gettering compared to the UMG EpiWE cell without gettering, thus

indicating that more carriers can be collected in the 30 µm thin active epitaxial layer. The EpiWE cell on Cz silicon substrate shows the highest IQE values of all EpiWE cells. The absorption length in silicon of 30 µm corresponds to a wavelength of $\lambda = 900$ nm [147]. Photons which are absorbed in the highly-doped BSF and substrate of EpiWE cells (in depths of > 30 µm) are lost and cannot contribute to the current. This is why EpiWE solar cells show lower IQE values at higher wavelengths, as compared to wafer solar cells.

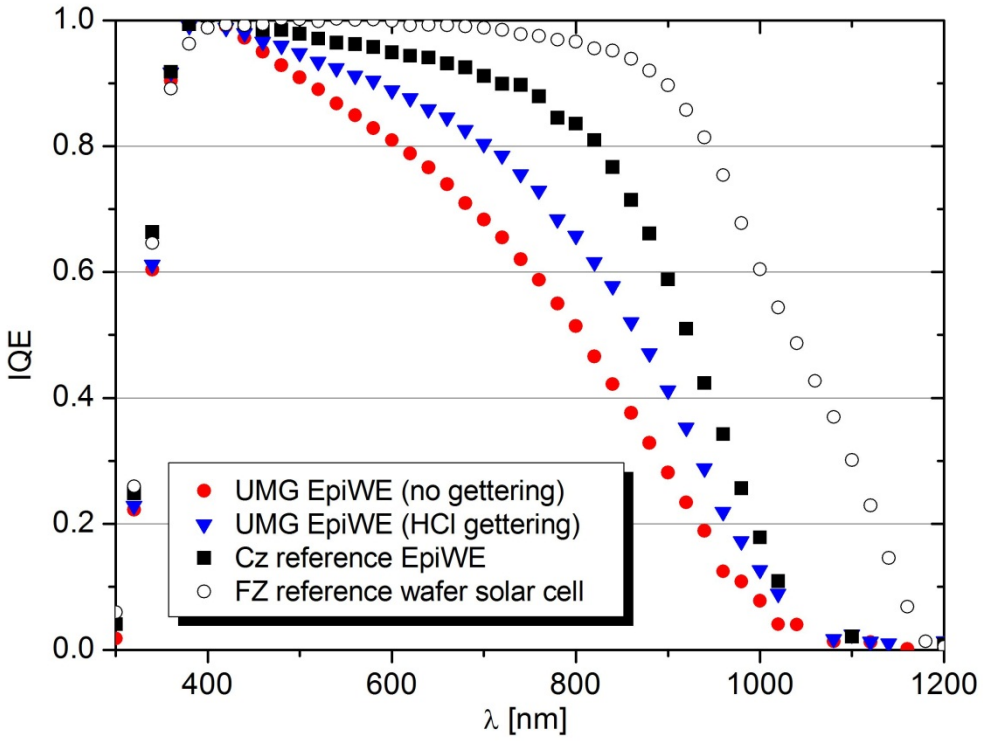

Fig. 5.18 Spectrally resolved internal quantum efficiencies (IQE) of selected solar cells, which are EpiWE cells on UMG silicon substrates with and without HCl gas gettering, an EpiWE cell on a reference mono-c Cz substrate, and a reference wafer solar cell made from a mono-c FZ wafer. Note that all cells were processed by a high-efficiency clean room process (diffused emitter with oxide passivation and photolithographically designed front grid).

Although high efficiencies were not the main goal for the solar cell runs presented in this work, another high-efficiency cell process was carried with the same 99.97% UMG silicon substrates in the frame of the EU project 'ThinSi' in cooperation with the solar cell group of the research institute *IMEC* in Leuven (Belgium), including porous silicon (PoSi) layers [19] and plasma texturing of the surface by *IMEC*. HCl gas gettering, epitaxy and the high-efficiency cell process, similar to that presented for the standard wafer cell concept (see section 2.1.2), were done at the *Fraunhofer ISE*. A clear improvement of the J_{SC} (2 – 3 mA/cm^2) by plasma texturing could be demonstrated. High cell efficiencies were achieved,

although some irregularities occurred during the PoSi etching process, and no improvement could be demonstrated on cell level, neither by PoSi layers nor by HCl gas gettering. In this work, only the results of the best cells are presented (see Table 5.14). They were measured at the accredited calibration laboratory *ISE CalLab*. They are so far the best results of EpiWE solar cells on low-cost UMG silicon substrates, which were processed at the *Fraunhofer ISE*, with 13.6% being the best cell efficiency.

It is not clear why no improvement by HCl gas gettering could be demonstrated for these cells. However, the cell efficiency level is rather high, being in the same range as EpiWE cells on mc EG silicon substrates, indicating that the amount of impurities, which can be removed by gettering, is no longer the main limiting factor. Also other impurities like C, N, or O, which cannot be removed by HCl gas gettering, and which can cause shunts or enhanced recombination in the bulk, can limit the cell performance.

Table 5.14 Best EpiWE solar cell results on 99.97% UMG silicon substrates without (-) and with HCl gettering (+), processed at the *Fraunhofer ISE* in the frame of the EU project 'ThinSi'. The cell process included plasma texturing, $POCl_3$ emitter diffusion, surface passivation by silicon oxide, metallization by photolithography and electroplating, and double layer antireflection coating. The most relevant solar cell parameters are given: V_{OC} = open circuit voltage; J_{SC} = short circuit current; *FF* = fill factor; η_{cell} = cell efficiency (see section 2.1.2).

Substrate material	Number of cells	Cell area [cm^2]	HCl gas gettering	V_{OC} [mV]	J_{SC} [mA/cm^2]	*FF* [%]	η_{cell} [%]
UMG Si	1 (best)*	21.2	(-)	620 ± 2	28.6 ± 0.5	76.6 ± 0.5	13.6 ± 0.3
UMG Si	1 (best)*	21.2	(+)	616 ± 2	28.0 ± 0.5	77.5 ± 0.5	13.4 ± 0.3
mc EG Si	1 (best)*	4.0	(-)	611 ± 2	29.0 ± 0.6	74.8 ± 0.5	13.3 ± 0.3
mono Si	1 (best)*	21.4	(-)	644 ± 2	30.4 ± 0.6	78.4 ± 0.5	15.3 ± 0.3

Independently confirmed by *ISE CalLab

5.4.3 EpiWE structures on UMG silicon substrates with heterojunction emitter

Silicon heterojunction (SHJ) solar cells combine a crystalline silicon base with an amorphous silicon emitter. SHJ cells on the basis of n-type mono-c silicon have shown to reach high open circuit voltages (V_{OC}) of above 720 mV and therefore high conversion efficiencies of above 22% [148, 149]. The application of amorphous silicon emitters on a crystalline silicon base provides an outstanding surface passivation and allows processes at low temperatures (< 200°C), which prevents the degradation of the silicon bulk quality. Higher V_{OC} values than with conventional diffused emitters are possible. However, the low minority carrier diffusion length in the amorphous Si layer and the fact that the transmittance of transparent conducting oxide (TCO) films usually is between 80 - 95% over the visible spectrum, lead to a

decreased J_{SC} value. The TCO layer, e.g., indium tin oxide (ITO), is needed on top of the amorphous silicon layer to improve the carrier transport. It is also used to decrease the reflectance. The Heterojunction with Intrinsic Thin layer (HIT) approach [150] introduces a 4 – 5 nm thin intrinsic layer between the base and the emitter for a further improved passivation. This approach is also investigated and optimized at the *Fraunhofer ISE*. For example, a p-type mono-c FZ silicon with a hydrogenated amorphous silicon carbide (a-SiC:H) emitter and a hydrogenated intrinsic amorphous silicon (a-Si:H) intermediate layer are used [151]. ITO layers are investigated in terms of their optical and electrical properties at the *Fraunhofer ISE* as well [152].

In principle, the heterojunction approach is also possible for EpiWE solar cells. Therefore, EpiWE structures with heterojunction emitter were processed on p+ 99.97% UMG silicon substrates in the size of 50x50 mm^2 with and without HCl gas gettering. As reference substrates p+ Cz wafers without gettering were used. It should be evaluated if the V_{OC} of EpiWE structures can be improved by the heterojunction approach, but more importantly if the V_{OC} of heterojunction EpiWE structures is improved by HCl gas gettering. For that purpose, it was sufficient to fabricate EpiWE cell structures without metallization because V_{OC} values can also be measured on heterojunction structures with TCO layers by means of the SunsV_{OC} method [153].

The sample structure which was used is presented in Fig. 5.19. Compared to the thickness of 10 – 20 nm in common SHJ structures, the thickness of the n+ a-SiC:H layer was chosen to be 40 – 50 nm, because an increasing thickness of the amorphous layer leads to an improved passivation and band bending at the a-Si/c-Si interface, and therefore to an increased V_{OC} [154]. Extremely rough surfaces of the UMG structures and high steps especially at grain boundaries make relatively thick (40 – 50 nm) amorphous silicon layers necessary. However, the J_{SC} decreases with increasing thickness because of a low minority carrier diffusion length in amorphous silicon. But since for the investigation in this work only the V_{OC} value is relevant, the thick doped a-SiC:H layer was used to guarantee that the quality of the heterojunction is not limiting the V_{OC}. The quality of the amorphous silicon layers and the potential to reach high V_{OC} values with this sample structure were tested on p-type FZ wafers. High V_{OC} values over 700 mV proved that the processes are not limiting the performance. The thickness of the intrinsic layer was limited to approx. 5 nm to enable a sufficient carrier transport [150]. ITO layers were used on the front and also on the rear side of the structure.

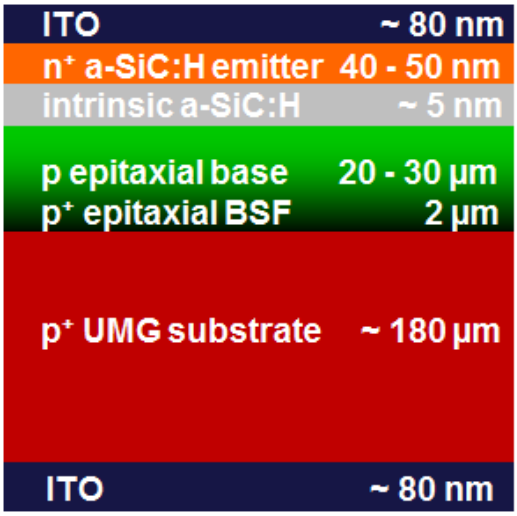

Fig. 5.19 Scheme of the EpiWE sample structure with heterojunction emitter (not to scale).

The whole sequence of process steps is summarized in Fig. 5.20. HCl gas gettering was applied to the UMG substrates prior to the deposition of the epitaxial p+ BSF and the epitaxial p-type base in a single RTCVD process. Gettering was done with the same parameters as for the EpiWE cells with diffused emitter (2% HCl/H_2, 30 min, 1300°C). The deposition of the intrinsic and the n+ doped a-SiC:H layers was performed by means of plasma enhanced chemical vapour deposition (PECVD) at around 200°C, and the deposition of the ITO layers was performed by means of magnetron sputtering at around 100°C.

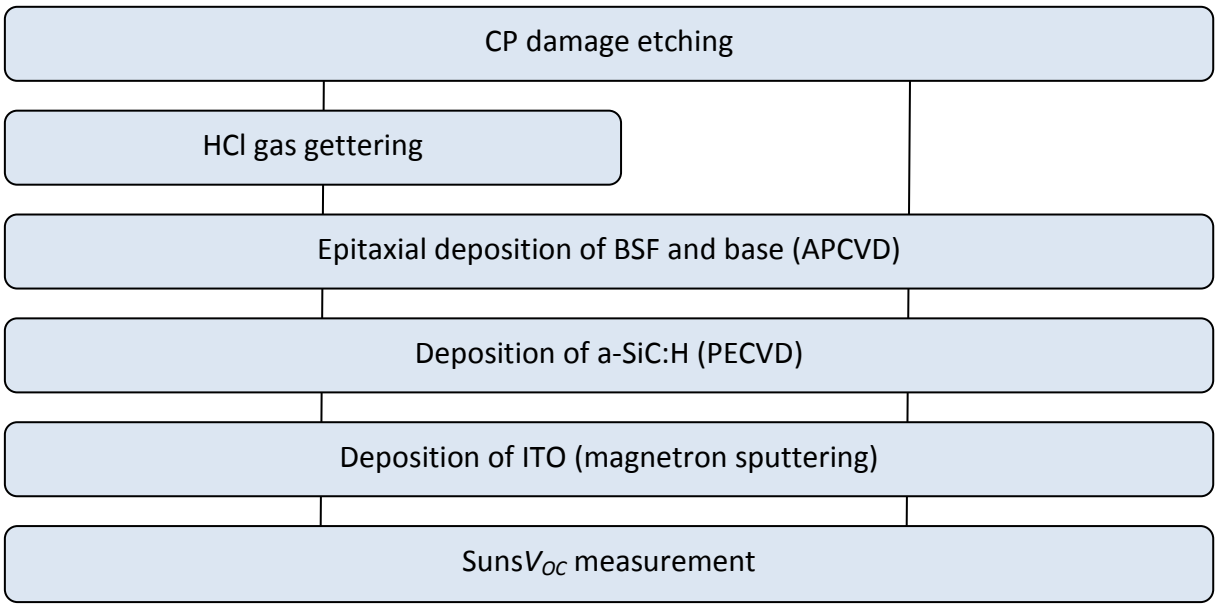

Fig. 5.20 Process steps of the heterojunction crystalline silicon thin-film (c-SiTF) sample structure.

The results of the Suns-V_{OC} measurement are given in Table 5.15. It is demonstrated that HCl gas gettering can improve the V_{OC} of UMG based EpiWE heterojunction structures by approximately 10 mV. The reference EpiWE structure on mono-c Cz substrate achieves about 20 – 30 mV higher values. One reason is the different surface morphology of UMG and Cz samples. The Cz wafers used in this work have a mirror polished surface while UMG is multicrystalline silicon material with rough surfaces. The silicon growth rates during epitaxy of the base varies from grain to grain depending on the grain orientation, and especially is lower at grain boundaries, which leads to relatively high steps at grain boundaries. Such steps are even visible to the naked eye on the surface of the heterojunction EpiWE structures after deposition of the ITO layer (see Fig. 5.21). In consequence, the amorphous silicon layer is thin at the edge of such grain boundary steps leading to an inferior passivation and therefore lower V_{OC}. As already mentioned, this effect was minimized by choosing a unconventionally high (40 – 50 nm) n+ a-SiC:H thickness. But still it cannot be neglected for heterojunction EpiWE structures on UMG silicon.

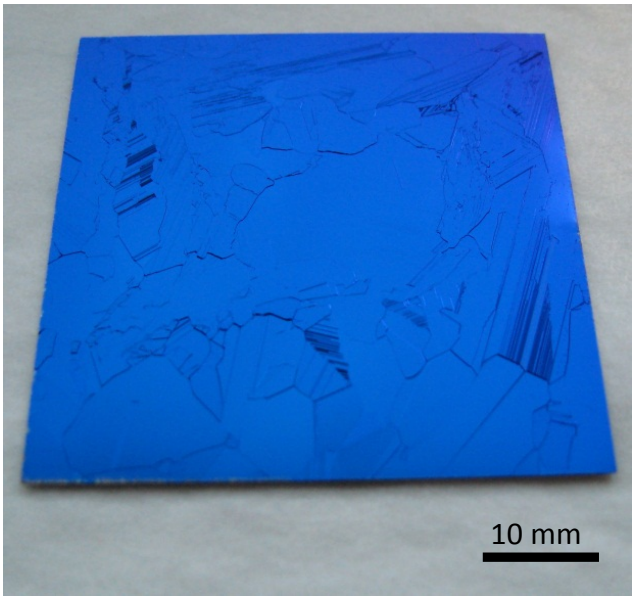

Fig. 5.21 Photograph of a heterojunction EpiWE structure on UMG substrate after the deposition of the (blue) ITO layer.

By comparing the obtained V_{OC} of heterojunction EpiWE structures with typical values of EpiWE solar cells with conventional diffused emitter (see Table 5.16), it can be observed that heterojunction emitters result in similar or even lower V_{OC} values for both types of substrates. The main reason for that is the additional gettering effect of P diffusion. This leads to less minority carrier recombination and thus to higher V_{OC} values compared to

heterojunction emitters. The heterojunction formation process is more sensitive to contamination of detrimental impurities.

Table 5.15 V_{OC} values of heterojunction EpiWE structures with and without HCl gettering of this work, measured by SunsV_{OC} measurement.

Substrate material	Number of cells	HCl gas gettering	V_{OC} [mV]
UMG Si	2	(-)	567 ± 3
UMG Si	2	(+)	577 ± 3
Cz Si	2	(-)	594 ± 4

Table 5.16 Typical V_{OC} values of conventional diffused emitter EpiWE cells with and without HCl gettering.

Substrate material	Number of cells	HCl gas gettering	V_{OC} [mV]
UMG Si	2	(-)	576 ± 12
UMG Si	5	(+)	604 ± 7
Cz Si	4	(-)	629 ± 6

5.4.4 Standard wafer solar cells

The effect of HCl gas gettering on the cell performance was also investigated for wafer solar cells in the same industrial-type furnace, which is described in section 5.3.2. Therefore, neighboring wafers from the same silicon material (100x100 mm^2 sized mc SoG silicon wafers) as used for the presented lifetime measurements were processed to solar cells. For the HCl gas gettering process, the same conditions (5% HCl/N_2, 850°C, 45 min) were applied. Three variations of standard wafer cells were processed: cells without gettering, cell with HCl gas gettering, which was done directly prior to the P emitter diffusion, and cells with HCl gas gettering and an additional P gettering step. The latter process means that the sequence of process steps were as follows: HCl gas gettering directly prior to a P diffusion gettering step (including wet-chemical PSG etching and emitter etching), and finally the P emitter diffusion (which is part of the solar cell process). The cell process described in section 2.1.2 was applied.

The cell results are presented in Table 5.17. Issues occurred during the antireflection coating (ARC), which lead to overall low J_{SC} values. However, an improvement by HCl gas gettering is shown for all solar cells. The best results are achieved for the wafers of the lowest ingot

position (no. 7 – 9). The V_{OC} is increased by HCl gettering by approximately 20 mV. As already discussed for the minority carrier lifetime measurements impurities are able to diffuse from the crucible into the bottom of the ingot, forming recombination sites and thus leading to reduced lifetimes in the wafers. This contamination effect can also be clearly seen for wafer/cell no. 7. It can be significantly improved by HCl gas gettering in contrast to cells of higher ingot positions (no. 16 – 18 and no. 25 – 27), which have already low contamination levels without gettering. It is obvious that an additional P gettering further improves especially V_{OC} and *FF* and thus the cell efficiency.

Table 5.17 Wafer solar cell results without (-) and with gettering (+) techniques applied. Three types of solar cells are shown: without gettering, with HCl gettering, and with both HCl gettering and P gettering. The uncertainty of a single measurement can be given as: V_{OC} ~ 0.5%; J_{SC} ~ 2.5%; *FF* ~ 1% (rel.); η ~ 2.9% (rel.).

Wafer No. / Position	Cell area [cm^2]	HCl gas gettering	P gettering	V_{OC} [mV]	J_{SC} [mA/cm^2]	*FF* [%]	η_{cell} [%]
7	92.2	(-)	(-)	562 ± 3	18.4 ± 0.5	58.8 ± 0.6	6.1 ± 0.2
8	92.2	(+)	(-)	581 ± 3	25.3 ± 0.6	66.7 ± 0.7	9.8 ± 0.3
9	92.2	(+)	(+)	589 ± 3	25.2 ± 0.6	78.0 ± 0.8	11.6 ± 0.3
16	92.2	(-)	(-)	589 ± 3	28.9 ± 0.7	70.2 ± 0.7	12.0 ± 0.3
17	92.2	(+)	(-)	591 ± 3	29.3 ± 0.7	70.8 ± 0.7	12.2 ± 0.3
18	92.2	(+)	(+)	593 ± 3	28.7 ± 0.7	78.5 ± 0.8	13.4 ± 0.4
25	92.2	(-)	(-)	584 ± 3	28.8 ± 0.7	67.6 ± 0.7	11.4 ± 0.3
26	92.2	(+)	(-)	590 ± 3	29.2 ± 0.7	71.9 ± 0.7	12.4 ± 0.3
27	92.2	(+)	(+)	594 ± 3	29.0 ± 0.7	77.9 ± 0.8	13.5 ± 0.4

It can be concluded that the cell efficiencies are increased by HCl gas gettering by 3.7% (absolute), 0.2% (abs.), and 1.0% (abs.). The increase of efficiency by HCl gas gettering is strong, except for the increase between no. 16 and 17 (0.2% absolute), which is not significant regarding the uncertainties. A combination of HCl gettering and P gettering show the most promising standard wafer solar cell results.

5.4.5 Discussion

Solar cells were processed basically applying two solar cells concepts, the EpiWE cell concept and the standard wafer cell concept. The principles of both concepts were already described in chapter 1. The focus was set on the EpiWE cell concept with variation of the types of low-cost substrates and the types of emitters. EpiWE cells were processed on MG and UMG silicon substrates using the conventional P diffused emitter. Furthermore, EpiWE cells on

UMG substrate were also processed with a heterojunction emitter, which is known from high-efficiency wafer based cell concepts and was adapted to the EpiWE cell concept.

EpiWE cells on MG silicon substrates revealed severe issues. It was shown that high amounts of metallic impurities in MG silicon wafers, e.g., several µg/g of each transition metal, lead to whisker formation during the epitaxial growth, thus leading to cell efficiencies < 3%. HCl gas gettering could not improve the cells, but rather even intensified the whisker formation effect due to the high-temperature treatment, leading to an increased dissociation of large metal precipitates and finally to many distributed smaller precipitates. Such precipitates at the surface can initiate the growth of silicon whiskers. It means that the impurity level in the investigated MG silicon substrates is too high to fabricate EpiWE solar cells, at least for the absence of an efficient diffusion barrier between the substrate and the epitaxial silicon layer.

Less impure UMG silicon substrates were used for the processing of EpiWE solar cells with higher performances than cells on MG substrates. HCl gas gettering and as a reference method P gettering was applied, demonstrating that HCl gas gettering improves mainly the V_{OC} (by ~ 64 mV) and thus the cell efficiency (by ~ 2% absolute) in a higher extent than P gettering, which showed an improvement of the V_{OC} by ~ 47 mV and of the cell efficiency by 1.2% (absolute). An exemplary element analysis for Fe on neighboring wafers to the wafers used for the cell processing indicated that the gettering efficiency, meaning the reduction of the Fe concentration, is higher in the case of P gettering, although the improvement on cell level was higher by HCl gettering. However, the cell performance is influenced by the reduction of several detrimental metals, not solely Fe, and the statistics of the analysis is rather weak. Nevertheless, the improvement of the EpiWE cell efficiency by HCl gas gettering is considered to be not only due to the reduction of metal concentrations, but also partly due to a smoother surface after HCl gettering at high temperatures (1300°C). This leads to lower dislocation densities in the subsequently grown epitaxial silicon layer, and thus to higher cell efficiencies. It was shown qualitatively by means of EL measurements of EpiWE cells on UMG substrates, that some regions in a substrate can be significantly improved by gettering while other regions/grains show less improvement, probably regions, which exhibit high densities of dislocations, which are likely decorated with metal precipitates. With a simplified cell process, 11.1% was the best cell efficiency that could be achieved applying HCl gas gettering. The best achieved cell efficiency of EpiWE cells on UMG silicon substrates at the *Fraunhofer ISE* was 13.6%, which was independently confirmed by the accredited calibration laboratory *ISE CalLab*.

For the first time, EpiWE cells on UMG substrates with heterojunction emitter were processed. Since amorphous silicon layers are more sensitive to impurities and a gettering effect is not present during processing of heterojunction structures, which is in contrast the case for conventional P diffused emitters, HCl gas gettering could be advantageous for

heterojunction EpiWE cells. Although it could not be shown that heterojunction emitters are finally advantageous for EpiWE structures, indeed, an increase of the V_{OC} by ~ 10 mV was demonstrated by applying HCl gas gettering.

HCl gas gettering could also be applied to the standard wafer cell concept. Thus, for the first time large-area (100x100 mm^2) mc SoG silicon wafer solar cells were processed in an industrial-type diffusion furnace with HCl gas gettering. Large improvements of the V_{OC} and thus of the cell efficiency were especially demonstrated for wafers near the bottom of the ingot, where elevated transition metal concentrations are assumed as compared to higher positions in the ingot. A significant increase by HCl gas gettering by 3.7% (absolute) was achieved. By a combination of HCl gettering and P gettering the standard wafer solar cell efficiency was even further improved.

5.5 Summary

The aim of this chapter was to assess the gettering efficiencies which can be achieved by HCl gas gettering, with emphasis on the gettering of low-cost silicon substrates for the EpiWE cell concept, but also gettering of conventional multicrystalline silicon wafers for the standard wafer cell concept. Element analyses (e.g., INAA, ICP-OES etc.) were carried out for the EpiWE cell concept in the case of highly-doped low-cost silicon substrates using neighboring wafers with and without gettering to assess the gettering efficiency for the most relevant transition metals. Electrical characterization methods to determine minority carrier lifetimes were preferred for moderately-doped UMG and lower contaminated conventional multicrystalline silicon for the standard wafer cell concept. Furthermore, solar cells were processed for the EpiWE cell concept and also for the standard wafer cell concept. The focus was set on the EpiWE cell concept with variation of the types of low-cost substrates and the types of emitters. EpiWE cells were processed on MG and UMG silicon substrates using the conventional P diffused emitter. Additionally, EpiWE cells on UMG substrates were also processed applying a heterojunction emitter, which had been adapted to the EpiWE cell concept.

HCl gas gettering reduced the amount of metallic impurities in MG silicon wafers. Increased gettering times lead to increased gettering efficiencies. Inferior gettering efficiencies were achieved in wafers from a higher ingot position as compared to a lower position, although for the former, the transition metal concentration was 3 – 4 times higher. It is concluded, that metallic impurities in regions of high concentrations are present in states, e.g., as metal oxide species in precipitates, which do not respond to external gettering like metal silicides, leading to lower gettering efficiencies. The metal concentrations in the presented MG silicon

wafers after HCl gas gettering are still far too high for the processing of EpiWE solar cells with decent performances. Fabricated EpiWE cells on MG silicon substrates revealed severe issues. It was shown that high amounts of metallic impurities in MG silicon wafers, lead to whisker formation during the epitaxial growth, thus leading to extremely poor cell efficiencies. HCl gas gettering could not improve the cells, but rather even intensified the whisker formation effect due to the high-temperature treatment and leading to an increased dissociation of metal precipitates.

UMG silicon wafers with a lower initial impurity concentration, which seem much more promising for the EpiWE solar cell concept, were investigated by the variation of HCl gas gettering parameters like the temperature, the gettering time, and the HCl gas concentration. No clear trends could be observed. One reason might be the large deviations of transition metal concentrations in neighboring wafers, which were presented in chapter 4. The results can only be considered as significant when the differences are larger than the basic fluctuations in the material, which is represented by the error bars in the diagrams. The second reason why no clear trends were observed, are the general low transition metal concentrations, especially in the investigated 99.995% UMG silicon, which is more sensitive to contamination, e.g., in the reactor during HCl gas gettering (see section 3.3.4). Nevertheless, the results indicate a slight trend, that lower HCl concentrations are advantageous (e.g., 2% HCl/H_2). This is also true for practical reasons, as the silicon etching rate increases with increasing HCl gas concentration. Furthermore, the results indicate, that decreased temperatures like 650°C might be advantageous. This would also implicate that no etching of silicon occurred during the gettering process, allowing longer gettering times without the increase of a breakage risk due to a thin substrate. However, earlier experiments at 1300°C showed higher gettering efficiencies. Regarding the highest HCl gas gettering efficiencies summarized in Table 5.4 for each transition metal, it is obvious that Ni shows the highest gettering efficiency at 650°C, which leads to the conclusion that the gettering efficiency of fast diffusing elements (Ni and Cu) is not limited by the temperature, as compared to moderately diffusing elements (Cr, Mn, and Fe), which need higher temperatures to reach sufficient diffusivities. Unfortunately, there are no analysis results for Cu at low temperatures available in this work. Surprisingly, it could not be shown that longer gettering times lead to lower impurity levels. However, this correlation was already demonstrated on MG silicon wafers and should also hold true for UMG silicon. Comparing both investigated UMG materials made from 99.995% and 99.97% silicon, it shows that higher gettering efficiencies can be reached on the 99.97% UMG wafers.

First HCl gas gettering experiments were carried out with large-area 156x156 mm^2 sized 99.97% UMG silicon wafers in the continuous chemical vapor deposition (ConCVD) reactor.

Despite of surface contamination issues due to C particles from the inner graphite setup of the reactor, a gettering effect could be demonstrated, at least for Cu and Co.

Some results of the MG and UMG analyses, which were presented in this chapter, are hardly explicable. MG and UMG silicon is highly contaminated multicrystalline silicon material. It is known that external gettering techniques can show poor gettering efficiency in regions of high dislocation densities. The precipitation of transition metals at dislocations is in competition to the gettering process. Furthermore, high concentrations of O and C, which are present in MG and UMG materials, can also limit the gettering efficiency. For example, O precipitates act as efficient internal gettering sites. In this work, higher HCl gettering efficiencies were generally demonstrated on UMG silicon compared to MG silicon wafers, indicating that the described issues are even more relevant in MG silicon material.

UMG silicon substrates were also used for the processing of EpiWE solar cells with conventional diffused $POCl_3$ emitter. HCl gas gettering and as a reference method P gettering was applied, demonstrating that HCl gas gettering clearly improves the V_{OC} and thus the cell efficiency. The increase was even higher than demonstrated by P gettering, although the Fe concentration was found to be reduced more efficiently by P gettering. However, the cell performance is not only improved by the reduction of Fe, but also by the reduction of several other detrimental metals, which were not analyzed. Futhermore, it is considered, that the smooth surface after HCl gas gettering at high temperatures like 1300°C partly promotes an epitaxial growth with reduced dislocation densities and thus higher cell efficiencies.

The characterization of EpiWE cells on UMG substrates was also done by electroluminescence measurements, revealing some regions in the substrate, which could be significantly improved by gettering while other regions with likely high dislocation and thus metal precipitates densities showed less improvement. With a simplified cell process, 11.1% was the best cell efficiency that could be achieved applying HCl gas gettering. The best achieved cell efficiency of EpiWE cells on UMG silicon substrates at the *Fraunhofer ISE* was 13.6%, which was independently confirmed by the accredited calibration laboratory *ISE CalLab*.

For the first time, EpiWE cells on UMG substrates with heterojunction emitter were processed. Due to the high sensitivity of amorphous silicon layers to impurities and the lack of the P gettering effect, HCl gas gettering could be advantageous for heterojunction EpiWE cells. Although it could not be demonstrated that the heterojunction emitter is advantageous for EpiWE structures compared to the $POCl_3$ emitter, an increase of the V_{OC} by ~ 10 mV was demonstrated by applying HCl gas gettering.

In contrast to the electrically inactive highly-doped silicon wafer which is used as substrate in the EpiWE cell concept, the wafer for the standard wafer cell concept is electrically active. Thus, minority carrier lifetime measurements were carried out on neighboring mc wafers with and without HCl gas gettering to assess the gettering efficiency. It was shown that the lifetime in a mc silicon wafer is decreased through annealing processes at high temperatures, which is likely due to the dissociation of metallic precipitates and the distribution throughout the whole sample. A slight improvement of the lifetime by HCl gas gettering in the RTCVD100 could be demonstrated in an UMG silicon wafer by comparison to the lifetime of the not treated wafer. However, these results have to be considered carefully, since it is not approved for the presented UMG wafers that the lifetime of neighboring wafers is at a comparable level, or if the difference in lifetime is as strong as the metal concentrations, which was shown in chapter 4.

First HCl gas gettering processes in an industrial-type diffusion furnace revealed that similar or even higher lifetimes are achievable as compared to P gettering. HCl gas gettering could be easily applied to industrial-type furnaces and is a simple and cost-efficient process. It is feasible to apply HCl gettering directly prior to the P emitter diffusion for solar cell processing. An optimization of the HCl gas gettering parameters for the standard wafer cell concept must be done in order to further increase the gettering efficiency.

HCl gas gettering was also applied to the standard wafer cell concept. Thus, for the first time large-area (100x100 mm^2) mc silicon wafer solar cells were processed in an industrial-type diffusion furnace with HCl gas gettering. Because mc wafers made from SoG silicon were used, the wafers were taken from the very bottom of the ingot, where the transition metal concentration is usually higher. An increase of the V_{OC} and thus of the cell efficiency up to 3.7% (absolute) was demonstrated. By a combination of HCl gettering and P gettering the standard wafer solar cell efficiency was even further improved.

6 Simulation of HCl gas gettering

A first simulation model was developed for HCl gas gettering, which is based on diffusion equations. The principles of the model are described followed by the discussion of constraints due to simplifications in the model. The results are structured by the most relevant simulation parameters which are the transport coefficient, the temperature, and the gettering time. All input parameters are based on experimental HCl gas gettering data of UMG silicon, which were obtained in chapter 5.

6.1 Simulation model

6.1.1 Principles of the model

For the simulation of HCl gas gettering the simulation program *Sentaurus Process*© from *Synopsys*© was used [155]. One-dimensional (1D) process simulation was applied with the only dimension being the wafer depth. The simulation model is based on diffusion equations starting with Fick's first law in a 1D environment

$$J = -D\frac{\partial c}{\partial x}\ , \tag{6-1}$$

where *J* is the flux of particles, *D* is the diffusivity, *c* denotes the particle concentration and *x* denotes the wafer depth. With the 1D continuity equation, involving the time *t*, which is

$$\frac{\partial c}{\partial t} = -\frac{\partial J}{\partial x}\ , \tag{6-2}$$

Fick's second law is obtained:

$$\frac{\partial c}{\partial t} = D\frac{\partial^2 c}{\partial x^2}\ . \tag{6-3}$$

It is valid for *D* being constant (not depending on *x*), which is the case in good approximation. The temperature dependence of the diffusivity *D* was already described in eq. (3-1). The concentration c is calculated in the simulation using eq. (6-3) for a user-

defined number of x-values. Only at the surface an additional condition is introduced, which is described in the following.

When the metal arrives at the silicon surface it reacts with HCl to form volatile chloride compounds. The mass flux of the chloride compounds away from the surface into the gas phase shall be denoted by J_{gas} and described by

$$J_{\mathrm{gas}} = k_t(c_{\mathrm{back}} - c_{\mathrm{surf}}), \tag{6-4}$$

whereby k_t denotes the transport coefficient, c_{back} is the background concentration of the metal impurity, and c_{surf} is the surface concentration of the metal impurity. Eq. (6-4) is introduced for the x-value at the surface ($x = 0$) to describe how the surface reaction rate may influence the concentration profile. k_t is nondimensional and simulates finite reaction rates of the metal-HCl reaction at the surface to form volatile chloride compounds. It is a measure for the removal rate of the volatile products away from the surface. Only in the case of $k_t = 1$, the surface reaction rate is infinite, leading to a maximum concentration gradient. In this case only the diffusion through the silicon to the surface and the background concentration is limiting the gettering efficiency and not the reaction rate at the surface. In the case of $k_t << 1$, the reaction rate plays an important role and the gettering is not only limited by the diffusion. $k_t = 0$ corresponds to the case, in which the reaction products are not removed from the silicon surface and no concentration gradient and thus no diffusion occurs. It can be concluded that $0 < k_t \leq 1$.

Even if the boundary condition of $k_t = 1$ was close to the reality, the metal concentration at the surface would never be zero, because there is always a metal concentration background. Therefore, a fixed metal background concentration c_{back} of 10^{10} cm^{-3} was assumed and implemented in the simulation model, which means for example that the background concentration of Fe in the reactor and in the silicon sample cannot be below 0.4 pg/g (pptw).

6.1.2 Assumptions and simplifications

As it is the first simulation model for HCl gas gettering, there are still several assumptions and simplifications which the model is based on. The simulation can only be done for one metal element at the same time and interactions between various metals in one silicon wafer are neglected. All metals are present in interstitial form and homogeneously distributed. It is assumed that precipitates and defects like dislocations and grain boundaries are not influencing the diffusion in any way. The assumption that only interstitial metals are present and the role of precipitates is neglected is rough and might be causing the highest discrepancy between simulation and experimental results. Diffusion in the wafer is only 1D in the direction of the wafer depth and the grains are columnar, so that diffusing metals do

not interact with grain boundaries. This assumption is more likely the case for samples with large grains compared to the wafer thickness and might be the case in good approximation. Moreover, the input HCl concentration is not included into the model. The gettering efficiency must be considered to be not dependent on the HCl concentration. Alternatively, it can be considered to play a role in the transport coefficient. Furthermore, thermodiffusion is neglected, which is due to a temperature gradient. The most crucial assumptions and simplifications, which were applied to the simulation, are again summarized:

- Only one metal impurity species is present in the silicon wafer at once.
- All metal impurities are present in interstitial form and precipitates are neglected
- In case of multicrystalline silicon diffusing metals do not interact with grain boundaries.
- Input HCl concentration is not included

The simulation model has to be extended and improved to get a precise agreement between simulation and experiment. Especially, the second of the above listed simplifications is too rough and has to be considered in the model. The modeling of precipitates in mono- and multicrystalline silicon was successfully integrated into *Sentaurus* for the simulation of P diffusion gettering and Al gettering [106]. Yet it was not adapted to the HCl gas gettering simulation program but will be implemented in future HCl gas gettering simulation models. This would involve the distribution of the number and the size, and also the dissolution of metal precipitates in the silicon wafer and should allow predictions, which are much more precise than the existing HCl gas gettering simulation model.

6.1.3 Simulation parameters

The most relevant simulation input parameters are the impurity starting concentration c_0, the gettering time t, the temperature T, and the nondimensional transport coefficient k_t (see section 6.1). Values for t were selected between 0 and 120 minutes, values for T between 650°C and 1300°C, values for k_t between 10^{-9} and 1. There are also fixed parameters, which were used for all simulations in this work with the following values:

- Wafer thickness: 300 µm
- Background impurity concentration c_{back} (see section 6.1.1): 10^{10} cm^{-3}

6.2 Simulation results

One goal of the simulation was to obtain concrete values of the transport coefficient k_t. Results of the HCl gettering experiments on UMG silicon wafers, which are presented in

chapter 5 for different gettering times and temperatures, should lead to values of k_t through a fitted simulation. However, the experimental results revealed neither a clear trend by varying the gettering time *t* nor by varying the temperature T, as explained in section 5.2.6. This makes it difficult to determine values of k_t, which are valid for a whole set of experimental data. However, k_t values could be obtained for few experimental data. Although the k_t values were not valid for all experimental data it was still possible to draw qualitative conclusions by the simulation model. Simulations were done for Ni and Fe, which represent fast diffusing transition metals, and moderately diffusing transition metals, respectively.

6.2.1 Transport coefficient

As described above, the transport coefficient k_t is a measure for the reaction rate of the surface reaction. Fig. 6.1 and Fig. 6.2 show the simulated concentration profiles of Ni and Fe. The starting concentration c_0 was selected to be 3.6×10^{16} cm^{-3}. A low temperature (T = 650°C) and a short gettering time (t = 10 min) were used. The results demonstrate that in the case of fast diffusing metals like Ni, even at low T and for short t, the concentrations can be reduced by higher transport coefficients (k_t close to 1), which means that the surface reaction rate and not the diffusion from the wafer bulk to the surface is limiting the gettering efficiencies. This is not the case for Fe at the same process parameters. It is demonstrated by the simulation results that the Fe concentration cannot be reduced efficiently, even if the surface reaction is infinitely fast (k_t = 1). Thus, the diffusion is limiting the gettering efficiency.

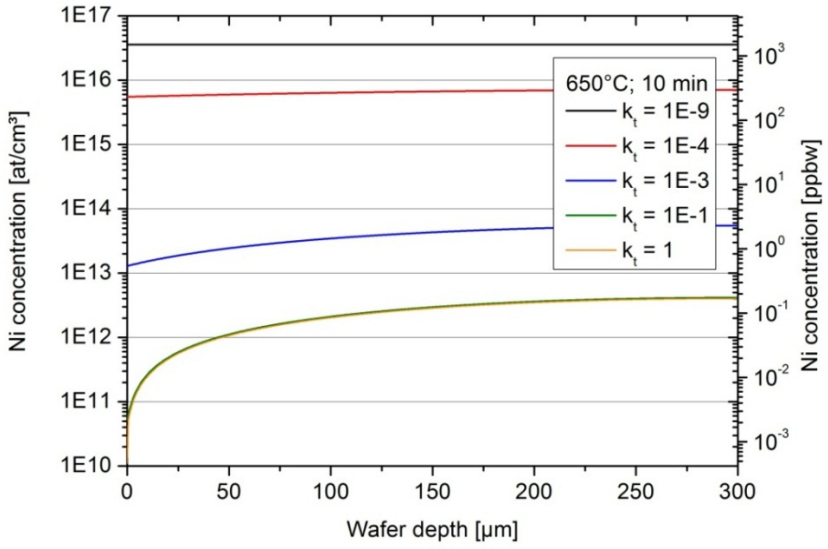

Fig. 6.1 Simulation of the Ni concentration after HCl gas gettering at T = 650°C for t = 10 min with variation of the transport coefficient k_t.

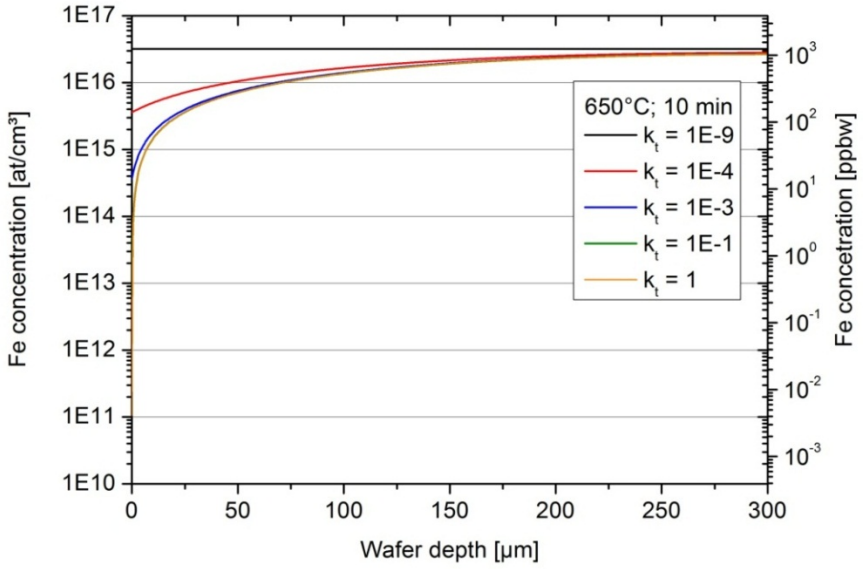

Fig. 6.2 Simulation of the Fe concentration after HCl gas gettering at T = 650°C for t = 10 min with variation of the transport coefficient k_t.

Experiments (shown in section 5.2.1) revealed a slight indication that lower temperatures lead to better results than higher temperatures. Higher gettering efficiencies were obtained for the wafer which was treated at 650°C as compared to 1300°C. This trend is tested by the simulation now. Fig. 6.3 shows the Fe concentration profile which was simulated at 1300°C and is compared to the previous simulation at 650°C (see Fig. 6.2). It reveals that the diffusion is not limiting any more at high T (1300°C) and higher gettering efficiencies can be obtained in the simulation for all values of k_t. It means that there is a strong discrepancy between experiment and simulation. There are two different explanations which are the possible reason for this observation. The first explanation is the prediction that the transport coefficient is strongly depending on the temperature and $k_t(T)$ decreases with increasing T [84]. An indication is the exothermic nature of the surface reaction. For higher temperatures the reverse reaction is preferred and the production of volatile metal chlorides is suppressed after Le Chatelier's principle [110]. However, the reaction rate of the forward reaction is still considered to be rapid for high temperatures and the vapor pressures of transition metal chlorides are rather high at high temperatures [98]. The second explanation is that there are other temperature depending effects, which are not yet accounted for in the simulation model but which are limiting the gettering efficiency, such as reactions with other impurities, especially in highly contaminated wafers made from MG and UMG silicon.

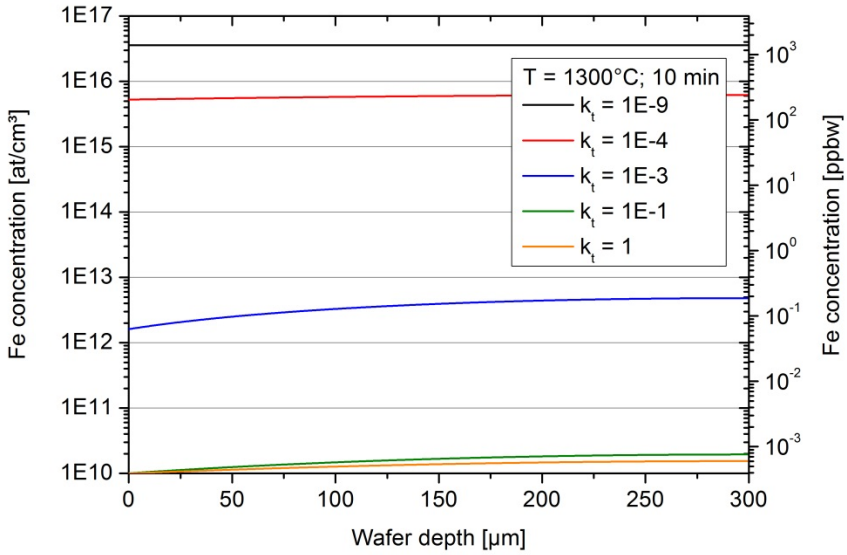

Fig. 6.3 Simulation of the Fe concentration after HCl gas gettering at T = 1300°C for t = 10 min with variation of the transport coefficient k_t.

6.2.2 Temperature and gettering time

In the previous section it was discussed that k_t could be considered to depend on T. If this was the case, the choice of T would be a trade-off between the positive impact of an increasing T on the diffusion and the negative impact of an increasing T on the transport coefficient. As explained before, the experimental results could not be used to determine k_t values, which are valid for all HCl gettering experiments and can generally be applied to HCl gettering simulations. But the influence of T and t on the simulation results will be described in the following, using some exemplary data of HCl gas gettering experiments on UMG silicon wafers at different T between 650°C and 1300°C, which were presented in Fig. 5.4. Ni concentrations without gettering and with HCl gas gettering at 650°C and 1300°C were used, and transport coefficient values of $k_t(650°C) \approx 1.3 \times 10^{-4}$ and $k_t(1300°C) \approx 5.5 \times 10^{-5}$ were finally obtained. On the basis of these values Ni profiles were simulated for different gettering times between 10 and 120 minutes at a temperature of 650°C and 1300°C. The results for Ni are shown in Fig. 6.4 and Fig. 6.5. Again, it can be seen that the diffusion is not a limiting factor for Ni. Higher gettering efficiencies can be achieved at the lower T due to the higher surface reaction rate (k_t is doubled from 5.5×10^{-5} to $k_t = 1.3 \times 10^{-4}$). After 120 minutes Ni can be completely removed from the wafer at 650°C. The residual Ni concentration of 10^{10} cm^{-3} correspond to the surface background concentration, which was applied in the simulation model. At 650°C, a gettering time of 30 minutes it sufficient to reduce the Ni concentration

from above 1 ppmw to a value of 2-3 ppbw. At 1300°C, the gettering time has to be doubled (60 min) to achieve the same gettering efficiency.

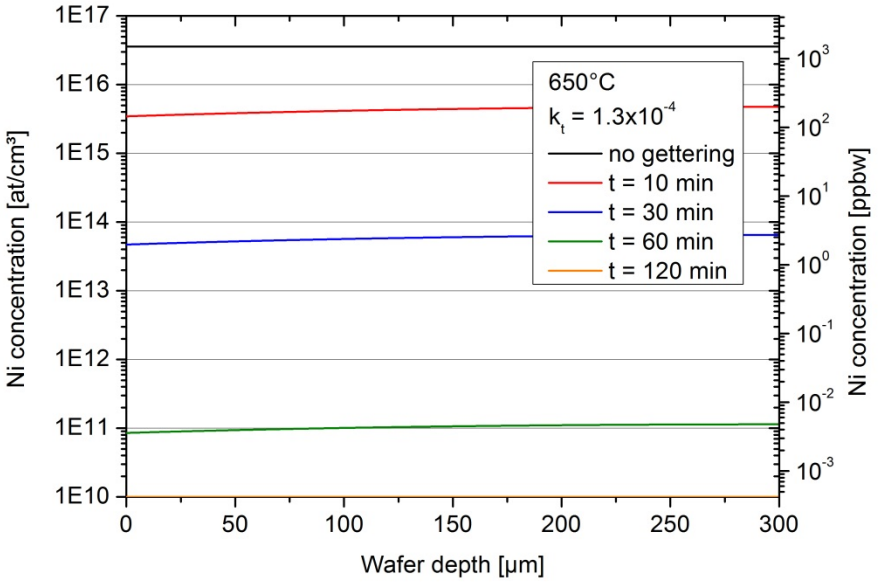

Fig. 6.4 Simulation of the Ni concentration at T = 650°C with variation of the gettering time t.

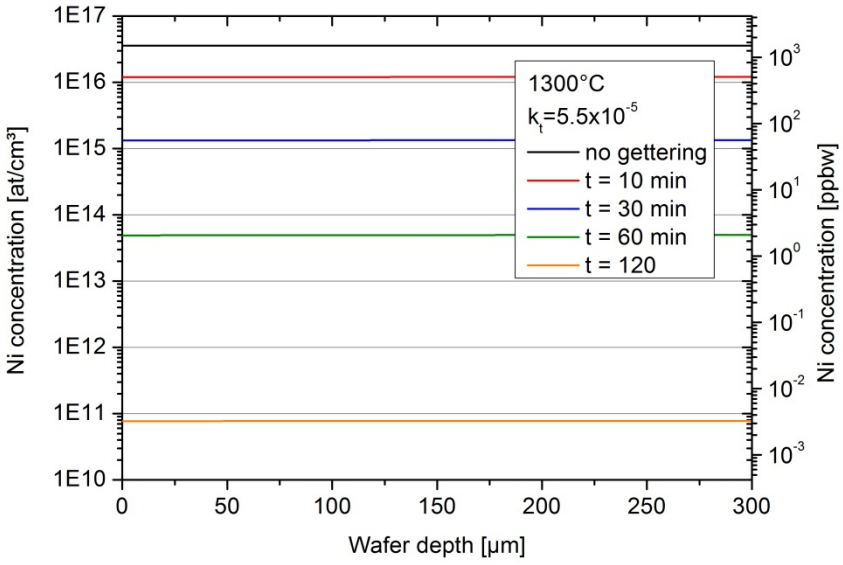

Fig. 6.5 Simulation of the Ni concentration at T = 1300°C with variation of the gettering time t.

The same simulations were done for Fe. The same k_t values were used for Fe as well. Thus it is required to assume that k_t is not depending on the transition metal. The results for Fe are

presented in Fig. 6.6 and Fig. 6.7. If the Fe concentrations at both process temperatures are compared, it is obvious that the advantage of a higher transport coefficient at 650°C disappears for gettering times higher than 10 minutes and the diffusion is the limiting factor, whereas at 1300°C the diffusion is not limiting and lower Fe concentrations can be achieved. This leads to the conclusion that higher temperatures should preferentially be used for moderately diffusing metals like Fe with gettering times of 30 minutes or more.

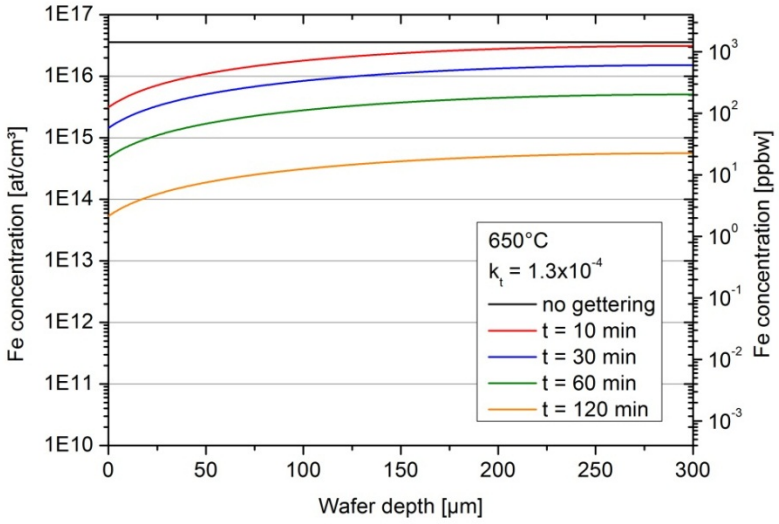

Fig. 6.6 Simulation of the Fe concentration at T = 650°C with variation of the gettering time t.

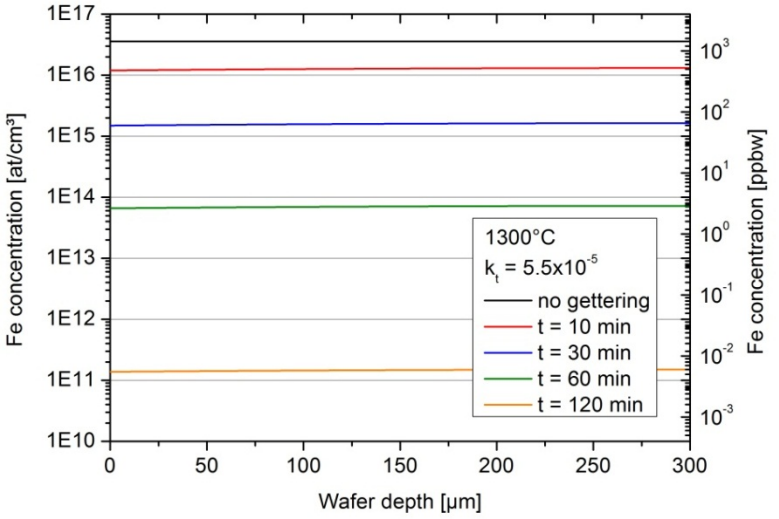

Fig. 6.7 Simulation of the Fe concentration at T = 1300°C with variation of the gettering time t.

6.3 Summary

In this chapter a simulation model for HCl gas gettering processes was introduced, which is based on the diffusion of impurities in silicon, depending on the applied gettering temperature and gettering time, and the removal rate of the impurities at the silicon surface, which is represented by the transport coefficient. It is a first model and still is based on several assumptions and simplifications. The most crucial simplifications are based on the assumption that monocrystalline silicon is used and the presence of precipitates can be neglected. This is a rough assumption, especially in the case of UMG silicon. Furthermore, unhindered diffusion of metals is assumed in the model, not regarding the possibility of interactions, such as metal-boron reactions and the interactions with oxygen or metal precipitates. Nevertheless, simulations could be done using some experimental data, which were obtained in HCl gas gettering experiments presented in chapter 5.2. Ni and Fe concentration profiles were obtained, which allow qualitative conclusions. The gettering efficiency of fast diffusing transition metals like Ni is not limited by the diffusion, even at low temperatures and short gettering times. For moderately diffusing transition metals like Fe higher temperatures and gettering times above 30 minutes should preferentially be applied due to the limiting diffusion at low temperatures. The simulation model has to be improved further. Especially, the presence of metal precipitates has to be included. Involving the distribution of number and size, and also the dissolution of metal precipitates in the silicon wafer through temperature treatments should allow predictions, which are more precise than that of the existing HCl gas gettering simulation model.

7 Summary

The aim of this work was to find the optimum process parameters for HCl gas gettering of 3d transition metals in low-cost silicon in order to improve the cell efficiency of solar cells for the EpiWE cell concept and also for the standard wafer cell concept. MG and UMG silicon materials with various purity grades were used in HCl gas gettering experiments and neighboring wafers with and without gettering were analyzed and compared by element analysis or minority carrier lifetime characterization methods, depending on the applied cell concepts. Solar cells were processed for both concepts to demonstrate an improvement of the cell efficiency by HCl gas gettering. A first simulation model was set up to support or disprove conclusions which were drawn from experimental results.

HCl gas gettering for the EpiWE cell concept

To be able to compare neighboring wafers with and without HCl gas gettering, some 3d transition metal concentrations were determined in several neighboring wafers of the investigated MG and UMG silicon material by means of trace element analyses like ICP-OES. The fluctuation of 3d transition metal concentrations from wafer to wafer was much larger than anticipated, especially in the UMG silicon material. Other than the MG silicon, which showed deviations in the same range as the uncertainty of measurement, the UMG silicon revealed large deviations up to one order of magnitude from wafer to wafer. Whether the reason can be found in the crystallization of the ingot due to periodic fluctuations of the growth rate or in a rather likely contamination of the samples after crystallization could not yet finally be clarified. Nevertheless, parameters (d_{max} and f_{max}), which are intended to describe the maximum deviation in the investigated silicon materials, were defined and applied to the further gained results as errors.

It was demonstrated that HCl gas gettering can significantly reduce 3d transition metal concentrations in MG and UMG silicon. In the case of Fe, a reduction of more than 91% in MG silicon and more than 98% in UMG silicon was achieved after 30 minutes of gettering at 1300°C. As expected, results for MG silicon indicated that longer gettering leads to a higher reduction. However, the processing of EpiWE solar cells demonstrated that the transition metal content is still too high to fabricate efficient solar cells on MG silicon substrates. The formation of whiskers was observed, which was even intensified by HCl gas gettering, leading to lower solar cell efficiencies. UMG silicon wafers with lower initial 3d transition

metal concentrations, which seem much more promising as substrates for the EpiWE solar cell concept, were investigated by the variation of HCl gas gettering parameters like the temperature, the gettering time, and the HCl gas concentration. No clear trends could be observed which is due to the presented large deviations of the initial concentrations in neighboring wafers. Furthermore, the general low 3d transition metal concentrations increased the sensitivity to contamination. Nevertheless, a slight indication could be deduced from the analysis results that lower HCl concentrations (2% HCl in H_2) are advantageous, which is relevant for practical reasons, as the silicon etching rate increases with increasing HCl gas concentration. A slight indication was found that decreased temperatures like 650°C might be advantageous. This would also be relevant for practical reasons, as the threshold temperature of significant UMG silicon etching with a concentration of 2% HCl in H_2 was determined to be 720°C ± 30°C. Below this temperature longer gettering times could be applied without the risk of a substrate breakage due to silicon etching. The indication that low temperatures are advantageous however conflicts with the fact that further experiments at 1300°C, each using two neighboring wafers showed the highest gettering efficiencies in UMG silicon in this work. This leads to the conclusion that the optimum temperature depends on the element. It is obvious that Ni shows the highest gettering efficiency at 650°C, which leads to the conclusion that the gettering efficiency of fast diffusing elements (Ni and Cu) is not limited by the temperature, as compared to moderately diffusing elements (Cr, Mn, and Fe), which need higher temperatures to reach sufficient diffusivities.

First HCl gas gettering experiments were carried out with 156x156 mm^2 sized UMG silicon wafers in the continuous chemical vapor deposition (ConCVD) reactor, demonstrating that it is also a feasible gettering technique for large-area in-line reactors. Despite of process issues due to C particles from the inner graphite setup of the reactor, a gettering effect could be demonstrated in the case of Cu and Co.

EpiWE solar cells with conventional diffused $POCl_3$ emitter were processed on UMG silicon substrates. HCl gas gettering and as a reference P gettering was applied, demonstrating that HCl gas gettering clearly improves the open circuit voltage and thus the cell efficiency. The increase was even higher as compared to P gettering. The average increase of the cell efficiency by HCl gas gettering was almost 2% (absolute). 11.1% was the best cell efficiency that could be achieved with HCl gas gettering, using a simplified cell process. The record cell efficiency of EpiWE cells on UMG silicon substrates at the *Fraunhofer ISE* was 13.6%, which was independently confirmed by the accredited calibration laboratory *ISE CalLab*. For the first time EpiWE cells on UMG substrates with a heterojunction emitter were processed. It could not be shown that a heterojunction emitter is advantageous also for EpiWE structures

compared to the conventional diffused P emitter, but an increase of the open circuit voltage by HCl gas gettering by 10 mV was demonstrated.

In this work, higher HCl gettering efficiencies were generally demonstrated on UMG compared to MG silicon wafers. Comparing both UMG materials, higher gettering efficiencies were reached for the lower grade UMG silicon. This indicates that the gettering efficiency does not only depend on the 3d transition metal concentration level but also on the distribution and the chemical states of the metals. Gettering techniques can show poor gettering efficiencies in regions of high dislocation densities in highly metal, O and C contaminated MG and UMG silicon materials. The precipitation of transition metals at dislocations or transition metal oxides, which are already present in the raw material, reduce the gettering efficiency. This could be indicated by electroluminescence measurements of EpiWE cells on UMG substrates in this work, demonstrating that some regions in the substrate could only be slightly improved, while other regions showed higher sensitivity to gettering.

HCl gas gettering for the standard wafer cell concept

In contrast to the electrically inactive highly-doped silicon wafer which is used as a substrate in the EpiWE cell concept, the wafer for the standard wafer cell concept is electrically active. Thus, minority carrier lifetime measurements were carried out on neighboring wafers with and without HCl gas gettering to assess the gettering efficiency. It was shown that the lifetime in a multicrystalline silicon wafer is decreased through annealing processes at high temperatures, which is due to the dissociation of metallic precipitates and the distribution throughout the whole sample. A slight improvement of the lifetime by HCl gas gettering in the lab-type RTCVD100 could be demonstrated in UMG silicon wafers. However, these results are based on the assumption that the lifetimes of neighboring wafers are truly at a comparable level. This is a common assumption, which is applied for gettering investigations on multicrystalline silicon in the literature, but has to be approved for the presented UMG, since the fluctuations in the 3d transition metal concentrations were also much higher than expected.

First HCl gas gettering processes in an industrial-type diffusion furnace revealed that similar or even higher lifetimes are achievable by HCl gettering compared to P gettering. HCl gas gettering could be easily applied to industrial-type furnaces and is a simple and cost-efficient process. It is feasible to apply HCl gettering directly prior to the P emitter diffusion for solar cell processing. An optimization of the HCl gas gettering parameters for the standard wafer cell concept must be done in order to further increase the gettering efficiency.

Nevertheless, for the first time large-area (100x100 mm^2) standard wafer solar cells were processed in an industrial-type diffusion furnace with HCl gas gettering. An increase of the

open circuit voltage and thus of the cell efficiency up to 3.7% (absolute) was demonstrated for wafers near the bottom of a multicrystalline silicon ingot. Using the combination of HCl gettering and P gettering, the standard wafer solar cell efficiency was even further improved.

Simulation of HCl gas gettering

A first simulation model for HCl gas gettering processes was set up, which is based on the diffusion of 3d transition metals in silicon, depending on the applied gettering temperature and gettering time. The removal rate of the impurities at the silicon surface was included and is represented by the transport coefficient in the model. Several assumptions and simplifications were introduced. The most limiting simplifications are based on the neglecting of defects like dislocations and grain boundaries, and also precipitates (monocrystalline silicon). This is a rough assumption, especially in the case of UMG silicon. Therefore, unhindered diffusion of metals is assumed in the model, not regarding the possibility of interactions, such as metal-boron reactions and the interactions with oxygen or metal precipitates. Nevertheless, simulations could be done using some experimental HCl gettering data of this work. Ni and Fe concentration profiles were obtained, allowing qualitative conclusions. The gettering efficiency of fast diffusing transition metals like Ni is not limited by the diffusion, even at low temperatures and short gettering times. For moderately diffusing transition metals like Fe, higher temperatures and gettering times above 30 minutes should preferentially be applied due to the limited diffusion at low temperatures. The simulation model has to be improved further to allow more precise predictions about HCl gas gettering, taking account of the distribution and dissociation of the 3d transition metal precipitates, which are especially present in low-cost silicon like MG and UMG silicon.

Nomenclature

Abbreviation	Description
a-Si	Amorphous silicon
c-Si	Crystalline silicon
a-SiC:H	Hydrogenated amorphous silicon carbide
EL	Electroluminescence
Ag	Silver
Al	Aluminum
AlG	Aluminum gettering
APCVD	Atmospheric pressure chemical vapor deposition
Ar	Argon
ARC	Antireflection coating
As	Arsenic
Au	Gold
B	Boron
BSF	Back surface field
C	Carbon
Ca	Calcium
Cl	Chlorine
Co	Cobalt
ConCVD	Continuous chemical vapor deposition
CP	Chemical polishing (wet-chemical treatment by HF/HNO_3)
Cr	Chromium
cSiTF	Crystalline silicon thin-film
Cu	Copper
CVD	Chemical vapor deposition
Cz	Czochralski
DL	Detection limit
DL-ARC	Double layer antireflection coating
EG	Electronic grade
EpiWE	Epitaxial wafer equivalent
F-AAS	Flame atomic absorption spectroscopy
Fe	Iron
FT-IR	Fourier transform infrared spectroscopy
FZ	Float zone
GF-AAS	Graphite furnace atomic absorption spectroscopy
H	Hydrogen
HCl	Hydrogen chloride
HFR	High flux reactor
HZB	Helmholtz-Zentrum Berlin

ICP-MS	Inductively coupled plasma mass spectrometry
ICP-OES	Inductively coupled plasma optical emission spectrometry
INAA	Instrumental neutron activation analysis
IQE	Internal quantum efficiency
ITO	Indium tin oxide
mc	Multicrystalline
MG	Metallurgical grade
MgF_2	Magnesium fluoride
Mn	Manganese
mono-c	Monocrystalline
MOS	Metal oxide semiconductor
N	Nitrogen
n+	Highly n-type doped
NAA	Neutron activation analysis
Ni	Nickel
O	Oxygen
OES	Optical emission spectroscopy
P	Phosphorus
p+	Highly p-type doped
Pd	Palladium
PDG	Phosphorus diffusion gettering
PECVD	Plasma-enhanced chemical vapor deposition
PGAA	Prompt gamma activation analysis
PLI	Photoluminescence imaging
$POCl_3$	Phosphoryl chloride
PoSi	Porous silicon
ppba	Parts per billion atoms
ppbw	Parts per billion by weight (corresponds to ng/g)
ppma	Parts per million atoms
ppmw	Parts per million by weight (corresponds to µg/g)
ppta	Parts per trillion atoms
pptw	Parts per trillion by weight (corresponds to pg/g)
ProConCVD	Production continuous vapor deposition
PSG	Phosphosilicate glass
Pt	Platinum
PV	Photovoltaic
QSSPC	Quasi-steady-state photoconductance
QSSPL	Quasi-steady-state photoluminescence
RTCVD	Rapid thermal chemical vapor deposition
SEM	Scanning electron microscope
Si	Silicon
$SiCl_4$	Silicon tetrachloride
$SiHCl_3$	Trichlorosilane
SiO_2	Quartz

SoG	Solar grade
SRH	Shockley-Read-Hall
SRP	Spreading resistance profiling
TCO	Transparent conducting oxide
Ti	Titanium
TiO_2	Titanium dioxide
TRIGA	Training, research, isotope production, General Atomics
UMG	Upgraded metallurgical grade
V	Vanadium
VGF	Vertical gradient freeze method
Xe	Xenon
XRF	X-ray fluorescence spectroscopy
Zn	Zinc

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