Hysteresis in Graphene Nanoribbon Field-Effect Devices

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Hysteresis in the current response to a varying gate voltage is a common spurious effect in carbon-based field effect transistors. Here, we use electric transport measurements to probe the charge transport in networks of armchair graphene nanoribbons with a width of either 5 or 9 carbon atoms, synthesized in a bottom-up approach using chemical vapor deposition. Our systematic study on the hysteresis of such graphene nanoribbon transistors, in conjunction with temperature-dependent transport measurements shows that the hysteresis can be fully accounted for by trapping/detrapping carriers in the SiO_2 layer. We extract the trap densities and depth, allowing us to identify shallow traps as the main origin of the hysteresis effect.

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Introduction

Hysteresis in carbon-based Field-Effect Transistors (FET) such as Graphene FETs and Carbon Nanotube (CNT) FETs is known to be a key feature that impacts the device performance [1,2]. While hysteresis allows for the possibility to build memory devices, it also causes an instability in the state of the FET which makes it highly undesirable in electronic and optoelectronic applications. Furthermore, it gives rise to uncertainty in determining fundamental properties such as the carrier mobility and the conductivity. It is therefore of scientific as well as technological importance to investigate the cause and effect of the hysteresis to improve the stability and reliability of carbon-based FETs.

Charge trapping/detrapping around the active layer is often considered as the cause for the hysteresis effect in such FETs. Defects in the SiO2 layer [3], adsorbed molecules from air [4], a water layer [5] or so-called silanol (Si-OH) groups [5] have been claimed to impact the hysteresis. Among these, the two most broadly accepted are charge traps originating from the SiO2 layer as well as adsorbed water layers on the interface. In contrast to the most published work, we combine room temperature measurements with low temperature measurements. In this approach, the temperature acts as an external control factor that enables us to unambiguously determine the cause of the hysteresis.

Despite the extraordinary properties of graphene such as its high mechanical strength [6] and excellent thermal properties [7], the lack of a bandgap prevents its use in digital logic circuits [8]. It has been predicted by theory that narrow graphene nanoribbons (GNRs) exhibit semiconducting behavior due to quantum confinement resulting in the opening of a bandgap [9,10]. Furthermore, GNRs show a strong response to external electric fields [11], rendering them suitable for field effect devices.

Common top-down approaches to fabricate GNRs include unzipping of carbon nanotubes [12] or lithographic patterning of graphene sheets [13]. While promising results have been obtained [14,15] using these approaches, they do not allow for a precise control over GNR edge and width. Bottom-up GNR synthesis methods have been developed to remedy these shortcomings [16-20], allowing for not only a controlled atomic and resulting electronic structure, but also the possibility of large-scale fabrication of ribbons all sharing the same structure and properties. While there is promising work on the use of hexagonal boron nitride (hBN) flakes as substrates for GNRs [21], hBN does not allow for a possible large-scale fabrication aimed with the bottom-up synthesis [22]. Hence, we focus on exploring the charge transfer properties on standard silicon oxide wafers.

Nowadays, a plethora of different bottom-up nanoribbons exist. For the use in any scalable digital devices, two main prerequisites, (i) a bandgap compatible with CMOS (e.g. higher than 350 meV [23]) and (ii) a comparative easy fabrication without expensive UHV-synthesis routines need to be fulfilled. Hence, we focus our effort on ultra-narrow GNRs with an armchair edge for their stability under ambient conditions as well as the available synthesis via an ambient-condition CVD routine [19]. Especially interesting are ribbons with a width of 5 carbon atoms (5-AGNR) for their high conductivity as well as 9-aGNR which possess a bandgap of ~1 eV, suitable for the use in infrared photodetectors [24]

5-AGNR is roughly 100 times more conductive than 9-AGNR, which makes the former one the most promising candidate for the use in applications so far, showing very promising results [25,26] for both network and single ribbon devices.

Hysteresis effects in single-ribbon bottom-up GNR FETs have been observed in previous reports [27,28], without, however, further insights into the origin of the hysteresis. Furthermore, the low device yield of single-ribbon devices [28] limits their practical use in applications.

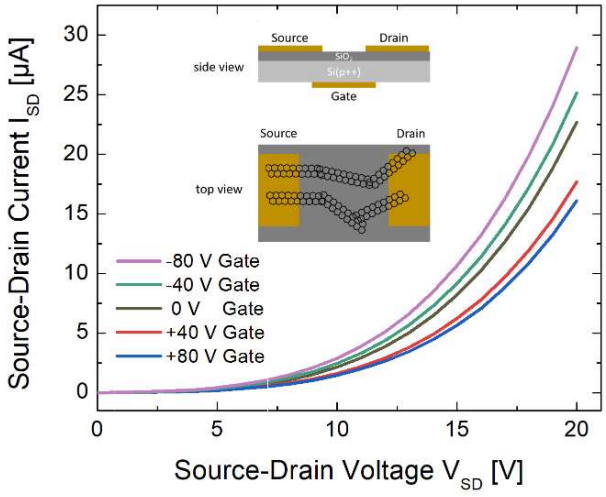

Fig 1 Output curves for a 5-AGNR network FET, measured at T = 262K for five different gate voltages. A clear modulation of the conductivity is seen. The inset shows schematically the side and top views of our devices.

We have recently reported the development of a reliable fabrication routine for GNR-network FETs with a device yield of almost 100% and very promising charge carrier characteristics [25]. This allows us to systematically study the charge transport properties of networks of AGNRs with different widths.

A fundamental understanding of the physics underlying the hysteresis is a prerequisite for further device development. Here, we systematically study the hysteresis in FETs based on CVD-grown GNR networks in order to enable further improvements of device performance. Via temperature-dependent measurements, we extract both the activation energy and the density of charge traps causing the hysteresis. These insights obtained for two distinct types of AGNRs (5-AGNR and 9-AGNR) are important for further efforts aimed at the successful implementation of GNR networks in working devices.

Results and Discussion

The inset of figure 1 shows a schematic top and side view of our GNR-network FET where we employ a bottom-gate structure to probe the charge transport through the monolayer network of GNRs which is indicated in the top view. Further details are found in the experimental section. Figure 1 shows output curves (source-drain current I_{SD} at a fixed backgate voltage V_G while sweeping the source-drain voltage V_{SD}) of a 5-AGNR FET. Different gate bias voltages clearly modulate the conductance of the network. For V_{SD}<1V, we find a linear behavior indicating an Ohmic contact behavior. For larger source-drain voltages, the current grows with a power law. This peculiar behavior indicates a charge transport governed by inter-ribbon hopping mediated by nuclear tunneling, as discussed in ref. [25]

Transfer curves, i.e. measuring the source-drain current I_{SD} at a fixed source-drain voltage V_{SD} while sweeping the backgate voltage V_G from −80 V to +80 V (up sweep) and vice versa (down sweep) are shown in Figure 2. We find that the conductivity is higher for negative bias voltages, indicating a *p*- doping of the ribbons. We cannot resolve a

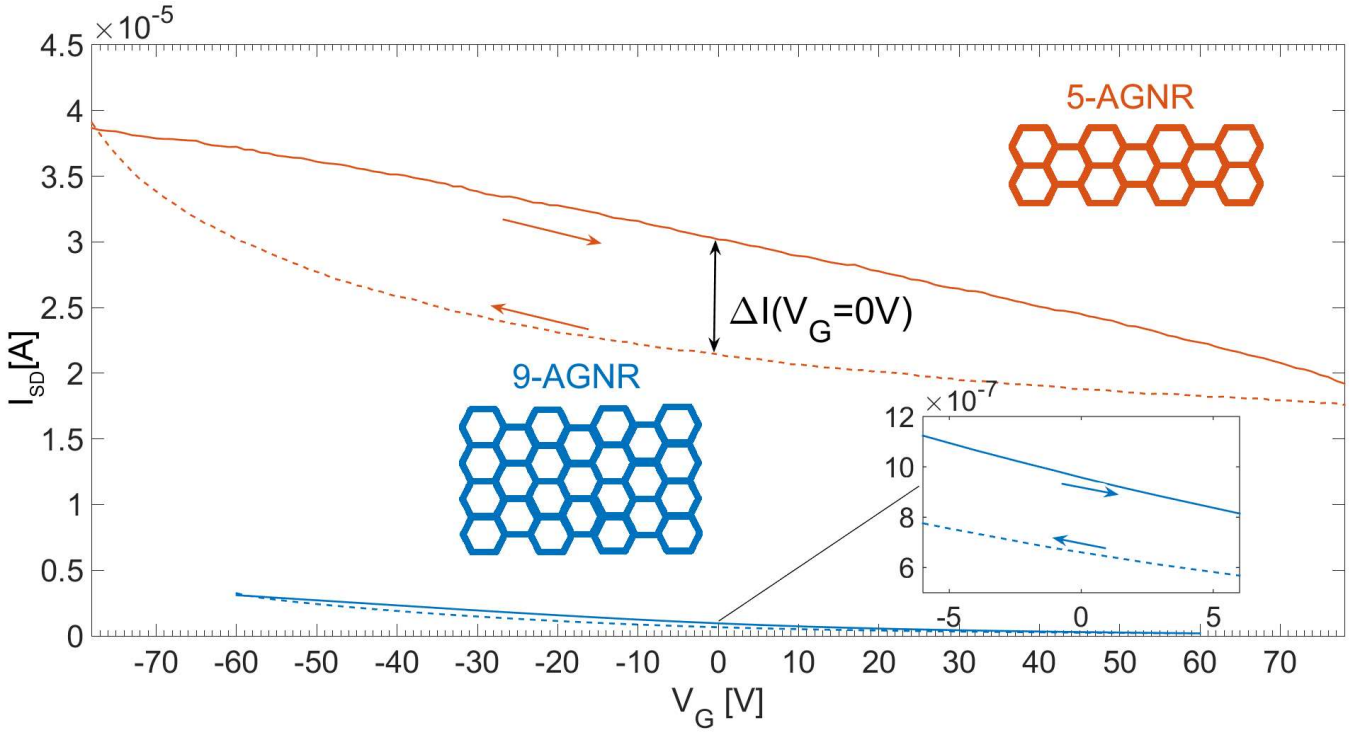

Fig. 2 Transfer curves of an 5-AGNR FET (orange) and an 9-AGNR FET (blue) measured at T = 262 K and a Source-Drain Voltage VSD = 20 V for two different gate sweep directions (down: +80 V → −80 V and vice versa). The hysteresis effect, a current difference in the transfer curves measured for the different sweep directions is visible. The inset shows a magnification for the 9-AGNR FET. The amount of hysteresis is quantified by the current difference between up sweep and down sweep measurements at zero gate voltage as indicated by the black bar.

conductivity minimum attributed to the Dirac points of the GNR as the sweep range of the gate is limited to ±80V in order to not break the oxide layer and to minimize gate leakage currents.

Note the clear hysteresis effect, both in 5-AGNR- and 9-AGNR-based FETs. We quantify the size of the hysteresis loop by calculating the current difference between the up-sweep and the down-sweep measurements at V_G = 0 V [29]. While different approaches such as using the voltage difference at a fixed source-drain current are in use to quantify the hysteresis [1-3], using the current difference eases further analysis done in this paper and is therefore used throughout in this work. For T = 262 K and V_{SD} = 20 V, we measure $\Delta I_{SD,9\text{-AGNR}}$ = 297 nA and $\Delta I_{SD,5\text{-AGNR}}$ = 8.7 µA. Considering the intrinsically lower conductivity of 9-AGNR FETs compared to 5-AGNR, a better comparison on the size of hysteresis can be done by normalizing ΔI_{SD} to the total current measured in the down sweep direction. Following this method, we see that the relative change of the hysteresis effect is 41% for the 5-AGNR FET, versus 45% for the 9-AGNR FET. Similar values are obtained for all applied V_{SD}.

As described above, both 5-AGNR and 9-AGNR devices exhibit comparable relative hysteresis. Similarly, in CNT FETs [30], the size of the normalized hysteresis has been shown to be comparable for two different diameters of CNTs. In combination with the fact that both FETs have been fabricated in the same way, we therefore conclude that the hysteresis is most likely caused by extrinsic factors as it would otherwise likely to be different for different ribbons.

Mobility extraction

To determine the cause of the hysteresis in our GNR-FETs, we first start with the determination of the field effect mobility. Afterwards, we analyse the hysteresis in detail and determine its origin. From the measured transfer curves, we were able to calculate the transconductance $g_m = \frac{\partial I_{SD}}{\partial V_G}$ from a linear fit to the average between up and down sweep below V_G = −20 V, yielding $g_{m,5\text{-AGNR}}$ (2K) = $3 \cdot 10^{-7}$ AV^{-1} and $g_{m,9\text{-AGNR}}$ (5K) = $3 \cdot 10^{9}$ AV^{-1} The field effect mobility can then be calculated from [31] $\mu_{F_{E_T}} = \frac{dL}{\varepsilon\varepsilon_0 W} \frac{g_m}{V_{S_D}}$ (1) where d = 300 nm is the gate oxide thickness, L and W the channel length and width and ε = 3.9 is the relative dielectric constant of SiO_2. The mobilities are thus estimated to be $\mu_{9\text{-AGNR}} = (3 \pm 0.1) \cdot 10^{-4}$ $cm^2 V^{-1} s^{-1}$ and $\mu_{5\text{-AGNR}} = (1.27 \pm 0.03) \cdot 10^{-2}$ $cm^2 V^{-1} s^{-1}$. These mobilities are in the high range of previously reported values [25], indicating a successful and reliable transfer process without harm to the ribbons. Thus, we can use these devices and measurements to extract useful insights on the cause of the hysteresis in GNR FETs.

Origin of the hysteresis

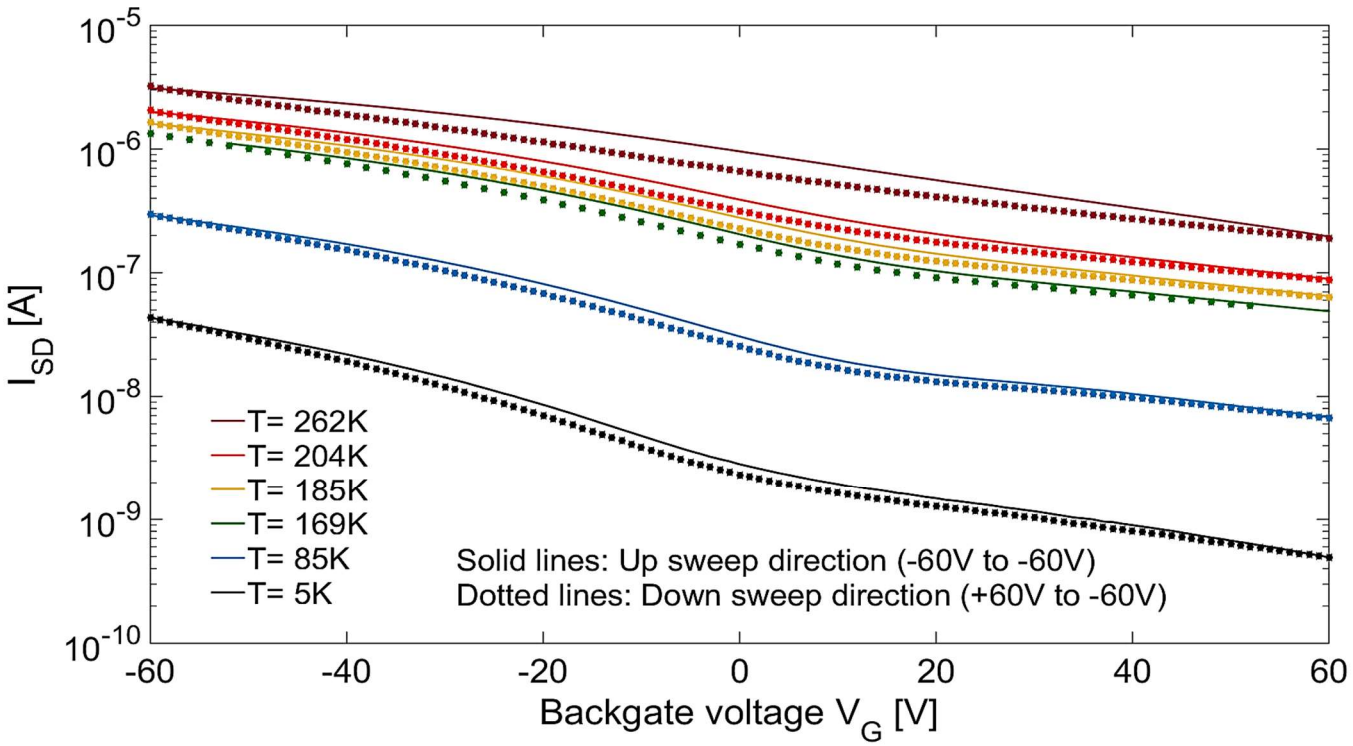

Fig. 3 Temperature-dependent transfer curves of an 9-AGNR FET. The backgate was swept from +60 V → −60 V, while the source-drain voltage was fixed at VSD = 20V. The shape of the curves between T = 204 K and T = 169 K are all similar which indicates that water/ ice formation is likely not the main source of the hysteresis.

As discussed in the introduction, there is no consensus for the origin of the reported hysteresis and multiple explanations for the hysteresis effect in carbon-based FETs have previously been proposed. Hysteresis measurements performed at room temperature are common practice to study the hysteresis in FETs. As the most discussed causes for the hysteresis (Charge trapping and water layers) both possess characteristic temperature dependencies, low temperature measurements are a key factor in determining the cause of the hysteresis. By varying the temperature, one can distinguish between different factors such as the influence of water adsorbates or charge trapping centers, which possess a characteristic activation energy that can be quantified by our temperature dependent measurements. With this temperature-based approach, there is no need to change other external factors that can possible permanently change the device properties such as varying the atmospheric composition. Figure 3 shows six transfer curves of our 9-AGNR FET measured at temperatures between T = 262 K and T = 5 K at a fixed source-drain voltage of V_{SD} = 20 V. Most likely, the hysteresis results from either charge transfer from adsorbates such as water molecules or charge injection intro trap states of the dielectric substrates. Assuming the former, we would expect step-wise changes in the transfer characteristics as a function of temperature due to temperature-dependent properties of water/ice such as the presence of a quasi-liquid water layer on the ice for temperatures higher than 237 K [32] or the immobility of protons in the ice below 190 K [33].

As shown in Figure 3, we see a smooth transition of the shape of the measured transfer curves for temperatures between T = 262 K and T = 5 K, where the absence of any abrupt changes indicates that charge transfer to adsorbed water molecules plays no significant role in the hysteresis. Thus, we can rule out this first scenario. We next consider charge traps at the SiO_2/GNR interface as the reason for the hysteresis. It is commonly accepted that electron traps in SiO_2 are formed due to the hydration of the silanol (Si-OH) groups [5] or due to defects in the SiO_2 layer [3]. If indeed those charge traps are responsible, we should be able to determine the density and trap depth from our electrical transport measurements. Indeed, this is borne out by our experiments. When sweeping V_G from positive to negative bias (down sweep) and back to positive bias (up sweep), the source-drain current I_{SD} of the up sweep is higher than that of the initial sweep thus resulting in a clockwise hysteresis loop. This leads to the assumption that negative charges accumulate at the interfaces while sweeping downwards to negative gate voltages [34].

Assuming a temperature-activated process for $\Delta I_{SD}(T)$

$$\Delta I_{S_D}(T) = A\, exp\left(-\frac{E_A}{kT}\right) \quad (2),$$

where A is a fitting constant and k the Boltzmann constant, we can extract the activation energy E_A of the trap states. Using the 9-AGNR-FET temperature-dependent transfer curves from Figure 3, we obtained $\Delta I_{SD}(T)$ for each

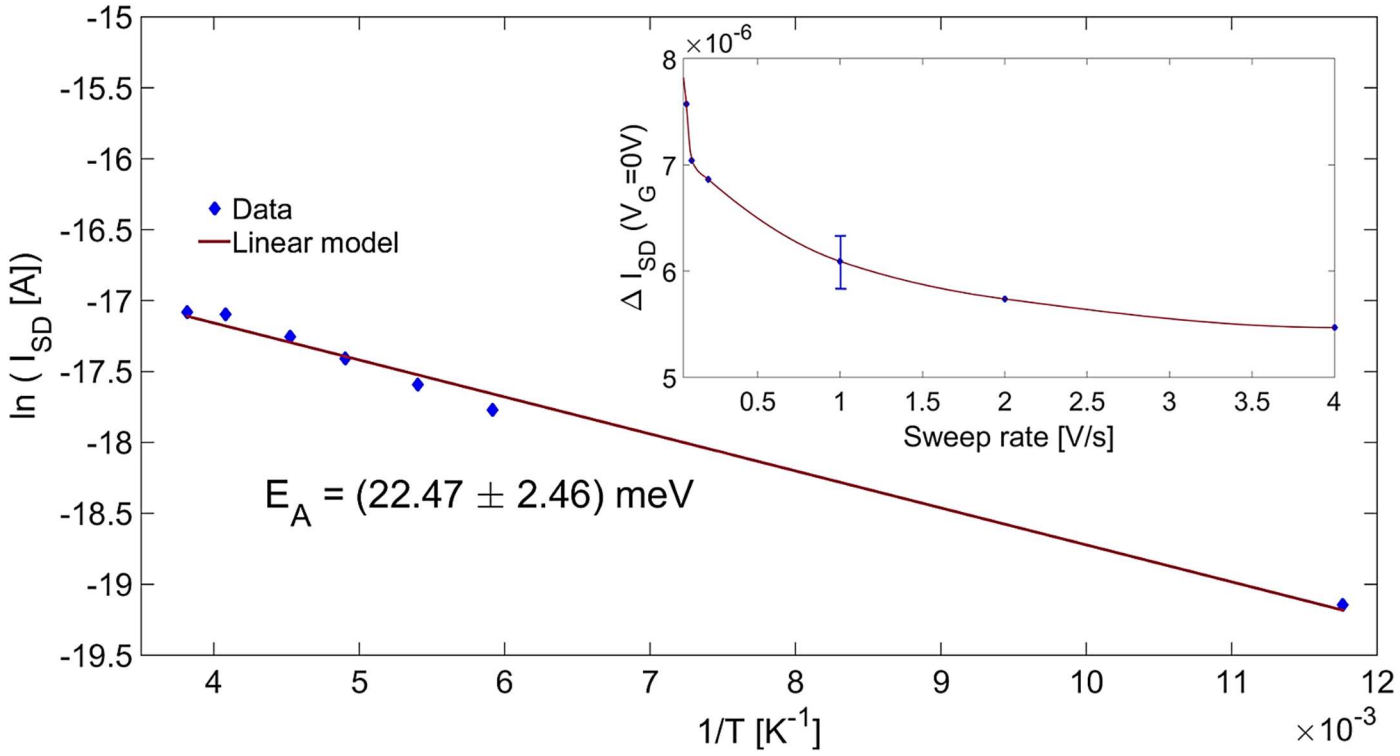

Fig. 4 Temperature dependence of the current difference ΔISD from a 9-AGNR FET, shown in an Arrhenius plot. The yellow dashed line shows the fit of the data to a linear model, resulting in an activation energy of EA = (22.47 ± 2.46) meV. The inset shows a sweep rate-dependent measurement of the hysteresis loop for an 5-AGNR FET. ΔISD (VG = 0V), an indicator of the size of the hysteresis loop, is measured as a function of the backgate sweep rate, which is varied between 0.1 V/s and 4 V/s. The size of the hysteresis is larger for slower sweep rates, indicating that a process on time scales >1 s is the cause for the hysteresis. The data points were measured at T = 300 K and VSD = −20 V. For each individual measurement, the error is negligible small (≈ 10^{-12} A). The error bar indicates the variation between multiple measurements. The line is a guide to the eye.

temperature. By using an Arrhenius plot (Figure 4) and a fit to a linear model, we can obtain an activation energy of E_A = (22.47 ± 2.46) meV. This energy agrees with previous reported trap state activation energies in SiO_2 [35-37]. Q_0^3 and Q_4^1 defects of the oxide [38] possessing one under-coordinated silicon and oxygen atom,respectively will likely act as a trap centers for the charge carriers [39].

Extraction of the trap state density

We can use the measured current differences and mobilities in a simple model to estimate the density of trap states n_{traps}(T) as [29]

$$n_{traps}(T) = \frac{L}{eW}\frac{\Delta I_{S_D}}{\mu_{FET} V_{S_D}}, \quad (3)$$

yielding $n_{traps,5\text{-}AGNR}$ (2K) = (2 ± 0.09) ·10^{10} cm^{-2} and $n_{traps,9\text{-}AGNR}$ (5K) = (3.8 ± 0.4) ·10^{10} cm^{-2}. This similarity corroborates the notion of charge traps as a cause for the hysteresis. The differences between the two values could be due to the presence of two layers and therefore two transfer processes for 9-AGNR rather than a single layer (for 5-AGNR) or the wafer-to-wafer variations of the structural heterogeneity of the oxide layer. Therefore, it is interesting to calculate the number of traps per ribbon. By extracting the average geometrical sizes of the GNRs from scanning tunneling microscopy measurements (9-AGNR: 1.2 nm × 20 nm, 5-AGNR: 0.8 nm × 15 nm) [19,24], we find that the extracted trap densities correspond to less than 0.01 traps per GNR. This implies that small differences in the oxide quality on dimensions comparable to the channel length can play a significant role in the size of the hysteresis.

Time-dependent trapping

Capturing charge carriers into the trap states is a time-dependent process. Therefore, we study the sweep-rate $\left(\frac{\partial V_G}{\partial t}\right)$ dependence of ΔI_{SD}. The inset of fig.4 contains $\Delta I_{SD,5\text{-}A\text{-}GNR}$ obtained at T = 300 K, V_{SD} = −20 V and measurement rates between 0.25 s and 10 s per data point, yielding sweep rates between 0.1 V/s and 4 V/s.
The inset of fig.4 shows that ΔI_{SD} is larger for smaller sweep rates, indicating that the trapping/detrapping process takes longer than several seconds [1]. If the rate of the charge trapping/releasing is comparable to the sweep rates, the filling process of the traps cannot reach thermal equilibrium immediately. Hence, a hysteresis effect occurs. For

sufficiently fast sweep rates$\left(\frac{\partial V_G}{\partial t}\right)$, trapping of a significant amount of charge carriers from the GNR channel into the trap states is negligible, whereas slower sweep rates allow for the trapping/detrapping of a substantial number of carriers during the timescales of the measurements.
Therefore, ΔI_{SD} is larger for the latter case. For sweep rates larger than > 1 V/s, it seems that the size of the hysteresis levels off and reaches a finite value. After a reduction of 41 %, the size of the hysteresis reaches a value of $\Delta I_{SD,5\text{-}A\text{-}GNR} = 5.5 \cdot 10^{-6}$ A. No further reduction of the hysteresis is measured. Faster sweep rates are limited by the experimental setup. Hence, one way to decrease the impact of the hysteresis is to use faster sweep rates > 1 V/s which are also more promising in terms of applications.

Conclusions

Our measurements are indicating that the origin for the hysteresis is a carrier trapping/detrapping at the GNR–SiO_2 interface. In our systematic study of transfer curves of 5-AGNR and 9-AGNR FETs, we find smaller hysteresis in the latter, which can be attributed to its overall lower conductivity. By temperature-dependent transport measurements, we were able to calculate both the density of trap states n_{traps} as well as the activation energy E_A. We find that both extracted trap depths and density agree with reported values of shallow traps in SiO_2. Therefore, the hysteresis effect in our AGNR FETs can be fully accounted by the trapping and detrapping of carriers at defects in the oxide layer. We find no hint that molecular adsorbates such as water have an influence on the hysteresis, in contrast to previous claims for related systems [40].
Understanding the cause and implications of the hysteresis paves the way for a future broader use of AGNR-FETs in electronic applications such as digital logic circuits or optoelectronic devices.

Experimental Section

Bottom-up grown AGNR with a lateral size of N = 5 and N = 9 were synthesized using a chemical vapor deposition [19,24]. The procedure of the field effect device production was previously reported by us elsewhere [25]. Briefly, 25nm Au contact pads with a 5nm Cr adhesion layer were deposited by conventional electron beam lithography on 300nm SiO_2 (thermally oxidized) on a highly p-doped Si−Wafer for backgate measurements. Afterwards, GNRs were transferred onto the devices using a well-established wet transfer technique [20]. For 5-AGNR, a single layer was transferred, while for 9-AGNR, two layers were found necessary to reduce the resistance to a level measurable at low-temperatures. Furthermore, we use a channel length of L=2µm for 9-aGNR and L=5µm for 5-aGNR, for the same reason, optimizing the current at low temperatures. Measurements were performed in a variable temperature cryostat from Oxford Instruments using a Keithley 238 High Current Source Measuring Unit and a Keithley 2400 Sourcemeter. A stable temperature is achieved by balancing the flow of cold helium gas against a resistive heater. Hence, the measurements were conducted in a helium atmosphere with the exception of datasets obtained at T=169K. These sets were measured also in vacuum as this is the equilibrium-temperature of the cryostat with the variable temperature insert used. A current guarding method was used to accurately measure high resistivity samples in this setup.

Conflicts of interest

There are no conflicts to declare.

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