Device Physics and Nanostructuring of Organic Ferroelectric Memory Diodes

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SUMMARY

Organic ferroelectric memory diodes are promising candidates for data storage devices, which are required for many of the envisioned applications of flexible electronics. The active layer is stacked between two electrodes and consists of a blend of an organic semiconductor and the ferroelectric copolymer of vinylidene fluoride and trifluoroethylene, abbreviated as P(VDF-TrFE). In the memory diode, the bistable polarization states of P(VDF-TrFE) provide the binary memory information, while resistive and non-destructive read-out is governed by the organic semiconductor.

Although the exact operational mechanism is not fully understood, it is common sense that the interface between the ferroelectric and the semiconducting polymer is decisive. Therefore, in this work, a patterning technology is established that allows the fabrication of memory diodes, where the interface between P(VDF-TrFE) and the organic semiconductor is well-defined. Based on the experimental results, a device physics model is developed that explains the operation of memory diodes in detail.

In Chapter 1, the motivation and the objectives of this work are outlined. Moreover, the state of the art of the memory diodes is reviewed. Chapter 2 briefly describes the theoretical framework of this work. This includes basic concepts of ferroelectric polymers as well as charge transport in and charge injection into disordered polymer semiconductors. The materials and experimental methods are described in Chapter 3.

In Chapter 4, solution micromolding, the key technique of this work, is used to fabricate capacitors, which contain line gratings of P(VDF-TrFE). The idea is to establish the technology first before adapting it to the memory diodes. In solution micromolding, a structured elastomeric stamp is hot-pressed onto a substrate covered with P(VDF-TrFE) solution. This yields a line grating of the ferroelectric polymer, which can be backfilled with a non-ferroelectric polymer, here poly(vinyl alcohol) (PVA). Therefore, the PVA solution is poured onto the grating followed by hot-pressing with a flat unstructured stamp.

The resulting ferroelectric capacitors with the bilinear array of P(VDF-TrFE) and PVA as the dielectric exhibit reduced remanent polarization probably due to the topography of the bilinear array. P(VDF-TrFE) protrudes with respect to PVA, as it was patterned first. The problem of the reduced polarization can be overcome by fabricating the inverted array, where a micromolded line grating of PVA is backfilled with P(VDF-TrFE). The resulting microstructured capacitors show excellent performance.

Chapter 5 makes use of the inverted structure, too. For the patterned memory diode, a line grating of the semiconducting poly(9,9-dioctylfluorene) is first obtained by solution micromolding followed by backfilling with P(VDF-TrFE). The comprising memory diodes with Au as injecting bottom contact show a high On/Off ratio of 10^3, which is retained for more than 10^4 s.

Using stamps with smaller feature sizes for solution micromolding, the pitch width of the bilinear arrays can be scaled down systematically. Interestingly, the On-state current density shows an exponential increase, although the effective interface length between P(VDF-TrFE) and PFO increases only linearly upon downscaling. This might be related to an improved order of the organic semiconductors when processed into nanogratings.

Chapter 6 investigates the device physics of organic ferroelectric memory diodes. The well-defined arrangement of the polymers in the bilinear array facilitates the modeling of the patterned diode with a numerical device simulator. Since the two-dimensional ferroelectric polarization is particularly taken into account, complete current-voltage characteristics can be accurately predicted. The device model is also successfully applied to memory diodes, where the active layer is made of a random phase separated blend of PFO and P(VDF-TrFE). Moreover, a range of temperatures is considered. In all cases, a remarkable agreement between experimental and calculated characteristics is obtained confirming the validity of the device model.

The derived operational mechanism can be summarized as follows: since the injecting electrode forms a Schottky contact with the semiconducting polymer, the current density is normally low. Charge transport is injection limited and the diode is in the Off-state. Upon polarization of P(VDF-TrFE), a stray electric field between the polarization charges and the resulting image charges in the electrode rises. This enables efficient charge injection into the semiconducting PFO despite the huge energy barrier. The dominant injection mechanism is barrier tunneling. The injected charges then form an accumulation channel of only 2.5 nm width along the entire interface of PFO and P(VDF-TrFE). The origin for the accumulation is the lateral component of the P(VDF-TrFE) polarization. The diode is in the On-state and the high current density is completely governed by the interface. Although being a two-terminal device, the memory diode works like a transistor.

The polarization of P(VDF-TrFE) determines the current density through PFO in the memory diode. Based on that, a novel concept for a thin film thermistor with positive temperature coefficient (PTC) is demonstrated in Chapter 7. P(VDF-TrFE) depolarizes at the Curie temperature leading to a drop of the On-state current density of a memory diode at a fixed voltage. This is equivalent with a strong rise in the resistance and means that a memory diode is simultaneously also a switching-type PTC thermistor.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Motivation

Since the discovery of conductive polymers in the 1970ies [1], which was awarded the Noble Prize in Chemistry in 2000 [2], the field of Organic Electronics has developed rapidly. First of all, the focus has moved from conducting to semiconducting polymers as well as small molecules, and both were successfully implemented into organic solar cells [3], light emitting diodes [4], and thin-film transistors [5].

While organic light emitting diodes based on small molecules have reached commercialization being the essential component of smartphone displays, the situation for transistors and solar cells is different. The mobility of silicon is orders of magnitude higher than those of typical semiconducting polymers yielding organic transistors very slow compared to CMOS technology. A major drawback for plastic solar cells is that organic semiconductors are excitonic materials. Light absorption does not directly lead to a separated electron-hole-pair and thus, the solar conversion efficiency is limited [6].

Hence, organic semiconductors cannot compete with silicon as far as ultimate electronic performance is concerned. However, Organic Electronics has been recognized to open up novel application opportunities such as flexible active matrix displays [7], artificial skin [8], paper electronics [9], and wearable electronics [10], which can even be used for medical sensing [11] and treatment [12].

For these devices, properties like mobility are much less important than for instance softness, low weight and flexibility [13, 14]. These features can hardly be achieved with silicon. By contrast, organic semiconductors can be processed at temperatures compatible with flexible plastic substrates and are thus ideal candidates for the field of flexible electronics.

Moreover, organic semiconductors can be processed from solution using functional inks that contain the polymers or small molecules. Processes like inkjet printing have already been demonstrated to yield high-performance organic transistors [15], which can comprise even single-crystalline semiconductors [16]. Additionally, the compatibility with coating and printing techniques enables low-cost and large area manufacturing [17, 18]. As an example, roll-to-roll printing, as it is known in the production of newspapers, can be used to fabricate organic solar cells with high throughput [19, 20].

Combining solution processability and their mechanical behavior [21], the vision for organic semiconductors (and Organic Electronics in general) is that they will be part of a future key technology - printed flexible electronics - which poses the potential to bring electronic devices to our everyday lives [22, 23].

Most of the foreseen applications and devices of flexible electronics have one thing in common: the ability to store data is of great importance. Radio-frequency identification (RFID) tags for example have to send and receive stored information that is transmitted by a radio signal [24, 25]. Therefore, a memory technology is desired that is compatible with printable and flexible electronics and that simultaneously is non-volatile, *i.e.* the stored information is retained even if the power is turned off.

Ferroelectric polymers are specifically suited for flexible electronics, as they can be easily processed from solution at temperatures compatible with flexible substrates [26]. Moreover, thin films of organic ferroelectrics are bendable without compromising their properties [27]. The most widely investigated organic ferroelectric is the random copolymer of vinylidene fluoride and trifluoroethylene, abbreviated in the following as P(VDF-TrFE). Thin-film capacitors with P(VDF-TrFE) as dielectric exhibit stable polarization states [28] that can be used as non-volatile memories [29, 30].

However, implementation of capacitors into integrated circuits is hampered by the read-out of the information being destructive. As a consequence, the information has to be re-written after every read-out [31]. This problem can be overcome by combining P(VDF-TrFE) with a semiconducting polymer. In the resulting organic ferroelectric memory diode, the active polymer thin film is stacked between two electrodes. The microstructure of the phase separated blend film typically consists of semiconducting columns embedded in the ferroelectric matrix.

Depending on the orientation of the ferroelectric polarization, the current density through the semiconductor is either low or high corresponding to the Boolean logic states '0' or '1'. While programming of the states is performed at voltages higher than the coercive voltage, the information read-out can be carried out at much lower voltages and is thus non-destructive.

1.2   State of the art of memory diodes

The first organic ferroelectric memory diode was demonstrated in 2008. The phase separated blend film contained P(VDF-TrFE) and the semiconducting poly(3-hexylthiophene), abbreviated as P3HT [32]. Using silver as electrode, which forms a Schottky contact with P3HT, the current transport is normally injection limited and low. However, the current density through the semiconductor can be increased by orders of magnitude if the ferroelectric P(VDF-TrFE) is fully polarized and the dipoles are aligned in one direction. For the reverse polarization orientation, the current density is low (comparable to the unpolarized state). Hence, the memory diode can be switched between a low current Off-state (Boolean '0') and a high current On-state (Boolean '1') by reversing the polarization of P(VDF-TrFE). Both states are stable over time and can be repeatedly addressed many times [32].

Figure 1.1a shows the morphology of a phase separated blend thin film. Columnar domains of the semiconductor are distributed in the ferroelectric matrix. The columns are bicontinuous [33], meaning that they penetrate the entire film thickness from the bottom to the top electrode. This is illustrated in Figure 1.1b, which presents a schematic of a memory diode in cross section. Current density-voltage characteristics of a memory diode are presented in Figure 1.1c. As expected, the memory diode shows hysteresis for a positive voltage sweep (blue curve). Starting in the Off-state, the current density is first low, but then rises significantly if P(VDF-TrFE) is polarized and the diode switches into the On-state. Subsequent read-out at low bias yields a high current density On-state (red curve). If the polarization is switched
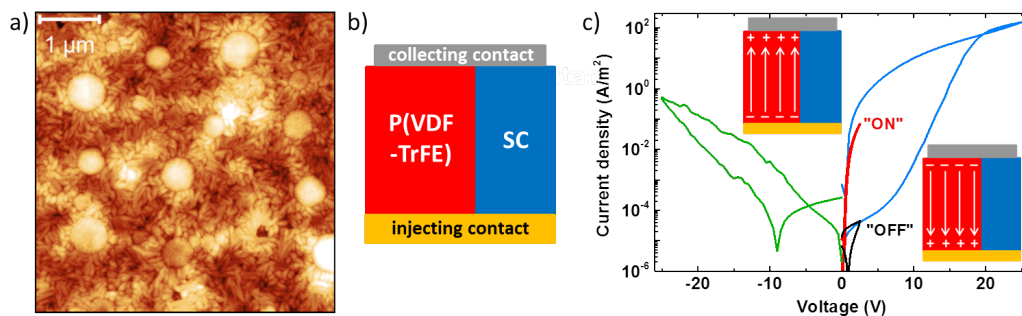
Figure 1.1: a) Morphology of a phase separated blend of P(VDF-TrFE) and a semiconducting polymer. Note that details on the morphology measurement will be given later. b) Cross-sectional scheme of a memory diode, where the polymer blend film is sandwiched between two electrodes (charge injection from the bottom). c) Current density-voltage characteristics of an organic ferroelectric memory diode. If the polarization of P(VDF-TrFE) is pointing upwards, the diode is in the high current density On-state. If the polarization points downwards, the diode is in the Off-state.

off by performing a negative voltage sweep (green curve), read-out at low
bias renders a low current density Off-state (black curve). As indicated in
the inset images of Figure 1.1c, the two polarization states of P(VDF-TrFE)
provide the binary information (Boolean states '0' and '1'), which can be
read-out non-destructively via the semiconducting polymer.

A crucial requirement for a memory technology is that single devices can
be integrated into large arrays. The simplest and most desired array struc-
ture is the cross-bar array, which could be realized with organic ferroelectric
memory diodes [34, 35]. Using appropriate top electrodes, a single memory
diode can be rectifying, as it is the case in Figure 1.1c: the diode is not
switching for negative bias and the current density at low (negative) bias is
always low. The important consequence for cross-bar arrays is that cross-talk
is significantly reduced, if each single diode is rectifying [34].

The exact working principle of organic ferroelectric memory diodes has
been the subject of investigations right from the start. Originally, it was
suggested that the ferroelectric polarization leads to band bending in the
semiconductor at the injecting contact [32, 36, 37]. Consequently, charge
transport was proposed to be bulk-limited when the diode is in the On-state,
while it is injection-limited, when the diode is in the Off-state [38]. However,
this mechanism requires a particular 3D morphology showing an undercut
of the ferroelectric slab, which was not observed in thorough morphological
analyses of various phase separated blend films [39, 40].

Later, numerical simulations were carried out to elaborate the device
physics of the memory diodes [41, 42]. Therefore, the polarization in P(VDF-
TrFE) was taken into account artificially by placing fixed charges at 1.5 nm
distance from the electrode. For the two polarization orientations the current
density could be calculated and the resulting ratio between On-state current
and Off-state current as a function of the Schottky injection barrier height
could be compared with an experimental data set [38].

As key result of these numerical simulations [41], a new mechanism was
proposed for the resistive switching: if P(VDF-TrFE) is fully polarized, a
stray electric field rises between the polarization charges of the ferroelec-
tric polymer and the compensating image charges in the electrode. This
stray field lowers the injection barrier at the Schottky contact yielding space-
charge-limited current transport, if the diode is in the On-state.

The performed numerical simulations exhibit severe limitations. Since
the polarization is only artificially taken into account, it is not possible to
describe entire current-voltage curves. Therefore, it is difficult to demon-
strate the validity of the model. Moreover, the mobility of the semiconduct-
ing polymer was taken as constant. On the contrary, the mobility depends
strongly on the charge carrier density and also on the electric field and the

temperature [43, 44]. Despite these issues, the proposed model has been state of the art, partly because it leads to one important conclusion, namely that organic ferroelectric memory diodes are interface devices. The interface between P(VDF-TrFE) and the semiconducting polymer determines the memory performance.

Based on these findings, the morphology of P(VDF-TrFE) blends with different semiconducting polymers was studied extensively [39, 40, 45–49]. As the random orientation of semiconducting columns in a P(VDF-TrFE) matrix is undesired, various approaches, such as side chain modification of the organic semiconductor [50] or temperature controlled spin coating [51], were investigated to gain more control over the morphology of the blends. Furthermore, by locally controlling the surface energy of the substrate with self-assembled monolayers patterned by microcontact printing, the self-assembly of the polymers upon phase separation could be directed to some extent leading to an enhanced On-state current density [52].

Instead of manipulating the phase separation process, the polymers can also be patterned directly. For instance, P(VDF-TrFE) was patterned with e-beam lithography followed by filling the empty spaces with P3HT [53]. While the patterning of the ferroelectric copolymer was outstandingly accurate, the filling procedure led to a semiconducting overlayer on top of P(VDF-TrFE), which is known to strongly limit the retention of the stored information [36].

Alternatively, P(VDF-TrFE) can be structured with nano-imprint lithography. This technique is very promising, as the resulting nanodomains of the copolymer showed a significantly decreased coercive field, when analyzed with piezo-force microscopy [54]. The memory diodes [55] however also suffered from retention issues, as a semiconducting overlayer was formed on top of the imprinted P(VDF-TrFE) upon backfilling. Obviously, a strategy for a backfilling procedure avoiding any overlayers is crucial for a successful technology transfer to organic ferroelectric memory diodes.

Despite the enormous effort to control the interface between the ferroelectric and the semiconducting material, the state of the art memory array is based on a random morphology [35]. The fabrication on a plastic foil additionally demonstrated the compatibility with flexible electronics. In their detailed analysis, the authors emphasize again the limitation of the random phase separated blend. Upon downscaling the area of a single memory diode in order to enhance the overall integration density, the stochastic variation of the number and size of semiconducting domains leads to an unacceptable device-to-device variability within the array [35]. This ultimate limit in the integration density can only be overcome, if the arrangement of the two polymeric materials can be controlled.

1.3   Objectives and outline of this work

Based on the state of the art review in the previous section, this work pursues the following objectives. First of all, a patterning technology should be established that enables the fabrication of well-defined interfaces between P(VDF-TrFE) and the semiconducting polymer poly(9,9-dioctylfluorene) (PFO).

Secondly, ferroelectric memory diodes comprising patterned polymer arrays as illustrated in Figure 1.2 shall be realized and carefully characterized. Importantly, an overlayer of PFO on top of P(VDF-TrFE) should be avoided to exclude retention problems for the diodes. Thirdly, a downscaling of the patterning technique should be achieved in a way that enhances the effective interface between P(VDF-TrFE) and PFO per unit area.

Finally, the experimentally obtained current-voltage characteristics shall be quantitatively described and explained. It is the ultimate goal of this work to understand the device physics of organic ferroelectric memory diodes in detail. Therefore, a universal device model shall be established.

This work is organized as follows: the theoretical background regarding semiconducting and ferroelectric polymers is given in Chapter 2. Chapter 3 describes the materials and methods used in this work. In Chapter 4, the patterning technology called solution micromolding is established and used to fabricate capacitors comprising patterned P(VDF-TrFE).

In Chapter 5, solution micromolding is carried out to fabricate patterned ferroelectric memory diodes, which are then analyzed in detail. Moreover, the period width of the polymer array (Figure 1.2) is systematically scaled down and the consequences for the comprising memory diodes are investigated.

Chapter 6 elaborates the device physics of organic ferroelectric memory diodes based on numerical simulations. The device model is first developed for patterned diodes, since the well-defined interface is ideally suited for a simulation approach. Afterwards, the model is also applied to random phase separated blends to verify the universality of the obtained findings.

Following the main results in Chapter 6, Chapter 7 demonstrates a completely new application for organic ferroelectric memory diodes: they can serve as thin film thermistors with positive temperature coefficient. The conclusion in chapter 8 finalizes the main part of this work.
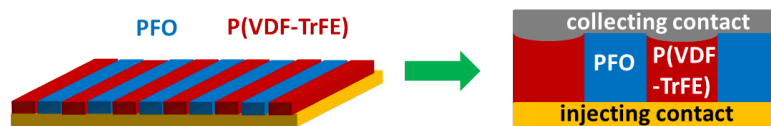
Figure 1.2: Bilinear array of P(VDF-TrFE) and PFO for a patterned memory diode.

Chapter 2

Theoretical background

This chapter provides an introduction into the theoretical background related to this work. First, the electronic structure of crystalline matter will be briefly discussed. Although organic semiconductors are typically not crystalline, the discussion on the physics of inorganic crystalline matter helps to better evaluate the differences between polymer semiconductors and for instance mono-crystalline silicon.

After elaborating the origin of the electronic structure of semiconducting polymers, the consequences for charge transport in these materials will be described. In the subsequent section, charge injection at a metal-semiconductor (Schottky) contact, which is particularly important for the physics of the memory diodes, will be discussed. The impact of the electronic structure on the Schottky barrier will be particularly emphasized. Finally, the topic of ferroelectricity and ferroelectric polymers will be shortly introduced.

2.1   Electronic structure of crystalline matter

The conductivity, Γ, determines the current density, $\vec{J}$, in a material upon the application of an electric field, $\vec{E}$, and thus $\vec{J} = \Gamma \vec{E}$ (Γ as tensor). Γ is the parameter with probably the strongest variation for different materials: between a conductor (high conductivity) and a material with low conductivity, an insulator, the conductivity can vary by 25 orders of magnitude (comparing *e.g.* Ag and quartz) [56]. The origin lies in the different electronic structure of the materials.

The electronic structure of crystalline (inorganic) matter can be approximated by solving the one-electron Schrödinger equation for a periodic potential that is defined by the cores of the crystal atoms (Bloch theorem) [57, 58]. As a result, the energy-momentum (ξ-k) relation of the electron is described.

For crystalline silicon, an excerpt of the ξ-k relation is shown in Figure 2.1a. A closer look reveals that the electronic structure is made up of bands, where electrons (or holes) can be in, and regions in between the bands, which are forbidden states for electrons (band gaps).

In Figure 2.1a, the valence band, which is the highest energetic band that is occupied at 0 K, is indicated in red. The conduction band is the next higher band in energy and it is indicated in orange. Based on the band structure, the conductivity strongly depends on how the bands are occupied with electrons. Since electrons are Fermions, they follow Fermi-Dirac statistics. Hence, the probability that an electron has a certain energy, ξ, is defined as

$$f(\xi, \xi_F) = \frac{1}{1 + \exp\left(\frac{\xi - \xi_F}{k_B T}\right)}, \tag{2.1}$$

where ξ_F is the Fermi energy, k_B is the Boltzmann constant, and T is the absolute temperature (in Kelvin). The electron density in the conduction band, $n(\xi)$, can be calculated by multiplying Equation 2.1 with the density of states (DOS), $g(\xi)$, and integrating in energy [60]:

$$n(\xi) = \int_{\xi_c}^{+\infty} g(\xi) f(\xi, \xi_F) \partial \xi. \tag{2.2}$$

The integration starts from the edge of the conduction band, ξ_C, which corresponds to the horizontal orange line in Figure 2.1a. For a three-dimensional crystalline material, the DOS is proportional to the square root of the energy, $g(\xi) \propto \sqrt{\xi - \xi_c}$ [61]. The huge difference in conductivity between insulators and conductors can be explained by the simplified picture in Figure 2.1b. In conductors (metals), different bands can overlap; the highest energetic band
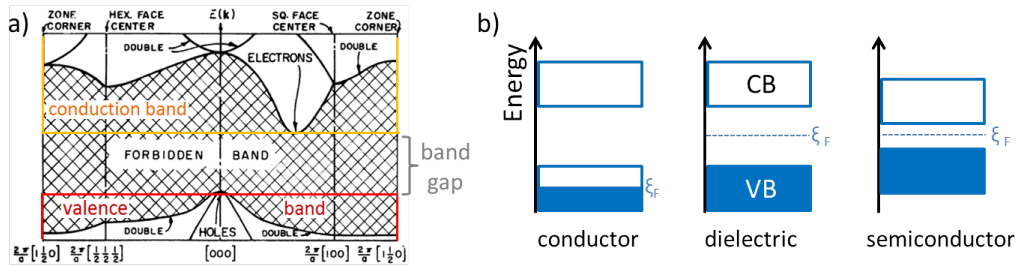
Figure 2.1: a) Energy-momentum (ξ-k) relation of crystalline silicone adapted from reference [59]. The valence band (VB) is the energetically highest band that is still occupied with electrons, while the conduction band (CB) is unoccupied at 0 K. b) Simplified electronic band structure of a conductor, a dielectric material (insulator), and a semiconductor (0 K).

that contains electrons is only partially filled. Thus, upon application of an electric field, electrons can easily move and the conductivity is high. By contrast, the valence band of insulators (or dielectric materials) is completely filled by electrons at 0 K, and consequently, $\vec{J} = 0$ [62]. Above 0 K, only a small amount of electrons can be found in the conduction band. These can move, if an electric field is applied. The same holds for the 'missing' defect-electrons or holes in the valence band. However, the conductivity Γ is defined as

$$\Gamma = q \cdot n(\xi) \cdot \mu, \tag{2.3}$$

where q is the electronic charge $(1.6 \cdot 10^{-19}\text{C})$ and μ is the mobility. Since $n(\xi)$ in the conduction band (as well as the hole density in the valence band) is very low for insulators, Γ is very low, too.

The band structure of the semiconductor appears similar to that of the insulator in Figure 2.1b, but there is one remarkable difference, the band gap, ξ_g, is significantly lower. Consequently, the electron density in the conduction band is also much higher leading to a higher Γ, which is still orders of magnitude lower with respect to conductors. It can be dramatically increased, though, by doping [1, 63], which will not be discussed further here, as the polymer semiconductors used in this work are generally not doped.

Polymers are large macromolecules, which contain a single molecular unit that is repeated many times along the backbone of the polymer. A polymeric material is made up of many of these macromolecules. While the bonds along the chain of each macromolecule are covalent, the different macromolecular chains are only linked by much weaker Van der Waals forces. Hence, polymer materials do not show a three-dimensional long-range order, although they can be crystalline over a small length scale (semi-crystalline polymers). The consequences of the disorder for the electronic structure of polymers are described in the following.

2.2 Semiconducting polymers

It is well-known that most of the commonly used polymers, such as polyethylene or polystyrene, are insulators. Their dielectric behavior is even utilized to electrically insulate conductors, *e.g.* metallic cables. But polymers can be semiconducting, if the backbone of the macromolecules is conjugated, meaning that the molecular structure contains alternating single and double bonds. The simplest case is polyacetylene, the chemical structure of which is shown in Figure 2.2a. Note that the 'only' difference between the chemical structure of polyacetylene and polyethylene is the double bond on every second carbon atom. As a consequence of the conjugation, all carbon

atoms along the backbone show sp^2-hybridization in polyacetylene, whereas the carbon atoms in polyethylene all exhibit sp^3-hybridization. The impact on the electronic structure is tremendous. The sp^2-hybridization of carbon is schematically illustrated in Figure 2.2c. In this case, the $2s$ and two of the $2p$ orbitals combine forming three degenerate sp^2 orbitals. One $2p$ orbital remains in its original state; it is used to form the double bond [64].

Ethylene (or ethene), C_2H_4, is the simplest organic molecule with a double bond. Figure 2.2b shows the ethylene molecule with its various bonds. For a covalent bond between two atoms, two atomic orbitals must overlap to form a molecular orbital. In total four sp^2 orbitals of carbon (two for each atom) overlap with the s orbitals of four hydrogen atoms: these C-H bonds are called σ bonds. The two remaining sp^2 orbitals overlap with each other yielding a σ bond between the two carbon atoms. Furthermore, the two p orbitals overlap and this results in a so-called π bond. Note that all σ bonds in ethylene lie in one plane, while the orientation of the p-orbitals is perpendicular to the plane.

The formation of covalent bonds can mathematically be described by the theory of the linear combination of atomic orbitals (LCAO). This is depicted in Figure 2.2d again for the case of ethylene. Two carbon atoms with sp^2-hybridization are shown, one on the left and one on the right; only valence electrons are considered here. The linear combination of two sp^2 atomic orbitals (one for each carbon atom) gives two possible molecular orbitals, one with lower energy, σ, and one with higher energy, σ^*.
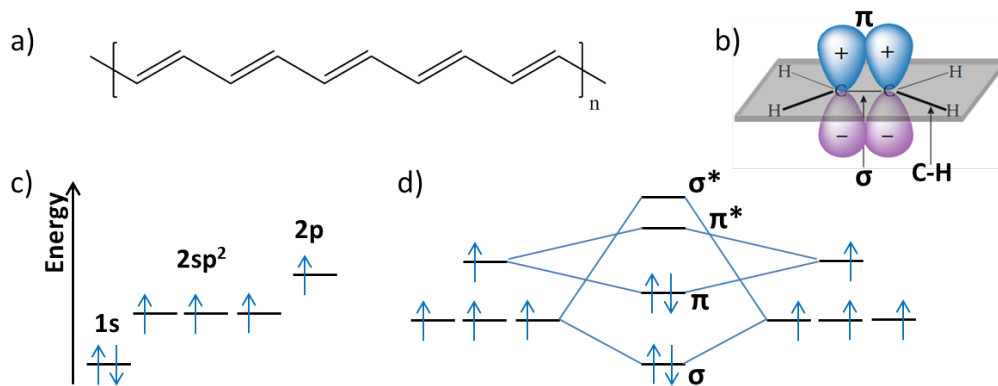
Figure 2.2: a) Chemical structure of polyacetylene. b) Formation of covalent bonds in ethylene. The picture was adapted from reference [64]. c) Schematic illustration of the sp^2-hybridization in carbon. The $1s$ orbital is filled and here only shown for completeness of the electronic configuration. Upon hybridization, the $2s$ orbital and two of the $2p$ orbitals (which are originally higher in energy) combine. As a result, three degenerate sp^2 hybrid orbitals are formed. The third p orbital remains in its original state. d) Schematic illustration of the formation of the double bond in ethylene based on the electronic configuration of the valence electrons. Molecular orbitals result from LCAO.

Similarly, the linear combination of the two *p* orbitals renders two molecular orbitals, π and π^*. For a stable bond, only the lower energetic molecular orbitals are filled, σ and π (bonding molecular orbitals), while the so-called antibonding molecular orbitals, σ^* and π^*, remain unfilled (cf. Figure 2.2d). The π orbital is called highest occupied molecular orbital (HOMO), while the π^* orbital is called lowest unoccupied molecular orbital (LUMO).

As mentioned above, a polymer semiconductor does not only have one double bond, but exhibits alternating double and single bonds (conjugation). Assuming that all carbon-carbon bonds are equal along the backbone of polyacetylene, the LCAO approach does not only consider two carbon atoms like in ethylene, but all carbon atoms in one macromolecule. The consequences for the electronic structure are indicated in Figure 2.3a. The more carbon atoms contribute to the system of π-electrons, the smaller the energetic distance between HOMO (π) and LUMO (π^*) gets [68]. Moreover, the density of energetic states increases. In an ideal case, the contribution of all carbon atoms of a macromolecule would lead to the formation of a valence and conduction band (instead of discrete HOMO and LUMO levels) and the energy gap would be very small or even zero: the polymer would be a metal-like conductor.

However, this would require a perfectly stretched macromolecule, where every carbon-carbon bond exhibits exactly the same length. The latter is not the case in semiconducting polymers due to the Peierls distortion, which always leads to a non-zero energy gap [69, 70]. More importantly, the macromolecules within a polymeric material are never stretched out completely, but suffer from twists and kinks in the chain. Hence, the system of conjugated π-electrons is limited to chain segments (conjugation length).
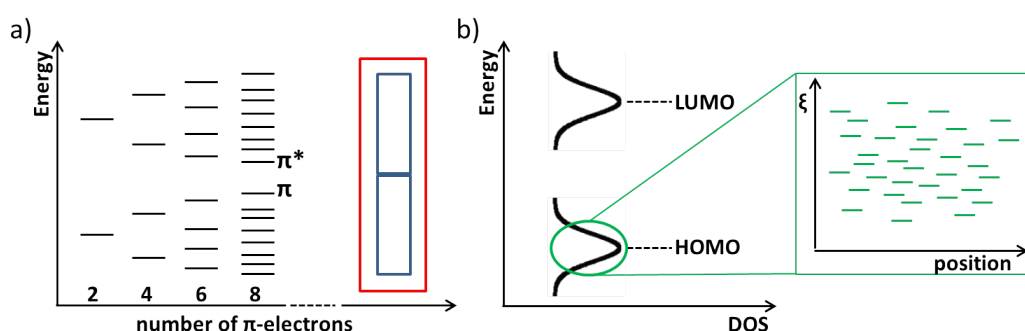
Figure 2.3: a) Energetic states as a function of the number of π-electrons in the conjugated system. Theoretically, for an infinite number of electrons, the formation of a valence band (corresponding to HOMO) and a conduction band (LUMO) would be expected (marked in red). b) Since the conjugation is limited to a small number of carbon atoms within a chain, a polymer semiconductor is characterized by discrete energetic states. The density of states (DOS) is typically described by a Gaussian [65–67].

Moreover, different macromolecules are only attached to each other by van der Waals forces rendering typically a rather weak electronic coupling between single polymeric chains. This is completely different to the case of mono-crystalline silicon, which shows strong 3D coupling between the covalently bound atoms of the crystal resulting in energetically broad (valence and conduction) bands. By contrast, the band width even in a highly ordered organic semiconductors is narrow.

In the typical case of a disordered polymer semiconductors, the electronic structure is characterized by discrete localized energetic states as schematically illustrated in Figure 2.3b. The DOS can be described by Gaussian functions, which read [65–67]

$$g(\xi) = \frac{N_t}{\sqrt{2\pi}\sigma} \exp\left(-\frac{(\xi - \xi_{HOMO})^2}{2\sigma^2}\right), \qquad (2.4)$$

where N_t is the density of sites in the semiconductor and σ is the width of the DOS. The Gaussians are centered around the HOMO/LUMO level. Note that in this work the energy is expressed by ξ and thus, the energy of the HOMO level is ξ_{HOMO}.

The disorder is also the main reason, why the charge carrier mobility in organic semiconductors is orders of magnitude below that of crystalline silicone (about 1000 cm^2/Vs [71]). Furthermore, the transport of charges works completely different in a disordered polymer semiconductor.

2.3 Charge transport in disordered organic semiconductors

Ohm's law, which defines the current density in a material under an applied electric field, can also be written as (scalars instead of vectors)

$$J = \rho(x) \cdot \mu \cdot E(x). \qquad (2.5)$$

where the charge carrier concentration, $\rho(x)$, and the electric field, $E(x)$, depend on the position in the material, x. The charge carrier concentration includes electrons (n) and holes (p), $\rho = q \cdot (p - n)$. The mobility is here taken as a constant. In conductors, the electron density and the electric field are constant, too.

For a semiconducting polymer, the situation is more complicated due to the disorder and the low mobility. The charge transport can be investigated in diodes, where a thin film of the polymer semiconductor is sandwiched between two metal electrodes (Figure 2.4a). The electrodes are chosen such that

they form an Ohmic contact with the semiconductor, which means that there is no (or hadly any) energy barrier between the Fermi energy of the metal and either the HOMO or the LUMO level of the polymer semiconductor. This guarantees that the bulk properties of the semiconductor (bulk-limited charge transport [75]) are analyzed and not the electrode-semiconductor interface; the latter will be the subject of the next section.

In a so-called electron-only diode, the electron transport in a polymer semiconductor is characterized. Therefore, the electrodes must form Ohmic contacts with the LUMO of the polymer as shown in Figure 2.4b. On the other hand, in order to achieve a hole-only diode (Figure 2.4b, lower picture), electrode materials are selected, which form an Ohmic contact with the HOMO level of the semiconducting polymer. The characterization of single-carrier diodes allows to exclusively study the charge transport for holes or electrons.

In Figure 2.4c, the current density measured for a typical hole-only diode is graphically illustrated as a function of the applied bias in double-logarithmic scale. For low voltages, the current density is proportional to the voltage (slope of 1 in Figure 2.4c) and charge transport is Ohmic [76]. The number of injected holes from the electrode is still very low in this regime.

For higher voltages the current density no longer scales linearly with the voltage, but shows a V^2-dependence (slope of 2). The high amount of charges 'supplied' by the electrode at high bias cannot be transported through the polymer film fast enough due to the low mobility and thus, a space charge is formed close to the injecting electrode. Rewriting Ohm's law, the hole
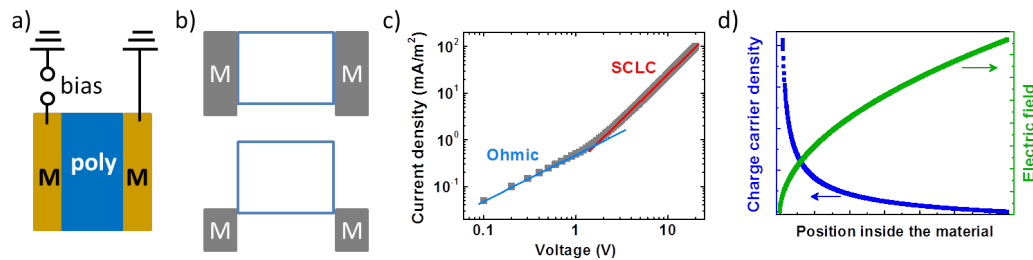
Figure 2.4: a) Device layout of a diode for charge transport characterization. The polymer is sandwiched between two metal electrodes. b) Energetic configuration of the two types of single-carrier diodes. For an electron-only diode, the metal electrodes form an Ohmic contact with the LUMO level of the polymer, which is illustrated here as one line for simplicity. In a hole-only diode (lower picture), the electrodes are selected such that their Fermi energy is close to the HOMO level of the semiconductor. c) Double-logarithmic plot of current density versus voltage showing an Ohmic and a space-charge-limited current (SCLC) regime in the hole-only diode analysis of a semiconducting polymer (curve was adapted from literature [72–74]). d) Charge carrier density (left) and electric field (right) as a function of position for the case of SCLC in a single-carrier diode.

concentration in a hole-only diode (electrons can be neglected) is

$$p(x) = \frac{J}{q\mu E(x)}. \tag{2.6}$$

Ignoring traps, the Poisson equation, which in electrodynamics [77] correlates the electric field to the charge carrier density, can be expressed as

$$\frac{\partial E(x)}{\partial x} = q\frac{p(x)}{\epsilon_r \epsilon_0}, \tag{2.7}$$

where ϵ_0 is the permittivity of vacuum, and ϵ_r is the dielectric constant of the polymer. In order to determine $p(x)$, Equations 2.6 and 2.7 have to be combined leading to

$$\frac{\partial E(x)}{\partial x} = \frac{J}{\mu\epsilon_r\epsilon_0 E(x)}. \tag{2.8}$$

Rearranging Equation 2.8 and subsequent integration yields the electric field as a function of the position for the case of space-charge-limited current (SCLC):

$$E(x) = \sqrt{\frac{2 \cdot J \cdot x}{\mu\epsilon_r\epsilon_0}}. \tag{2.9}$$

Figure 2.4d shows that $E(x) \propto \sqrt{x}$ (green curve). Here, the injecting electrode is located at $x = 0$ (on the left). Inserting Equation 2.9 into Equation 2.6 reveales that the position-dependent hole density is inversely proportional to the square root of the position: $p(x) \propto 1/\sqrt{x}$. This is shown by the blue curve in Figure 2.4d. Finally, the applied bias, V, is the integral of the electric field over the entire device thickness, l:

$$V = \int_0^l E(x)\partial x = \frac{2}{3}l\sqrt{\frac{2 \cdot J \cdot l}{\mu\epsilon_r\epsilon_0}}. \tag{2.10}$$

Solving Equation 2.10 for the current density leads to the well-known Mott-Gurney formula [78]:

$$J = \frac{9}{8}\mu\epsilon_r\epsilon_0\frac{V^2}{l^3}. \tag{2.11}$$

This explains the V^2-dependence shown in Figure 2.4c for higher voltages, when space charge effects become relevant [72, 74, 79].

In the discussion above, the mobility was assumed to be low and constant. Due to the disorder, the latter is not the case for polymer semiconductors. Instead, the mobility strongly depends on the exact shape of the Gaussian DOS (width σ), the temperature, the applied electric field, and especially

the charge carrier density. The origin lies in the nature of charge transport in disordered systems.

Figure 2.5a shows again the Gaussian distribution of energetic sites in a polymer film (DOS centered at the LUMO in this case). An applied electric field is the driving force for electrons to move across the film (here from left to right). Therefore, the electron has to hop from one discrete energetic site to the next. This is only possible, if the second site is unoccupied, and if the electronic wave functions of the two sites sufficiently overlap. The process of electron hopping from a site i to a site j is illustrated in Figure 2.5b.

In order to get from its present position r_i with the energy ξ_i to the position r_j with the energy ξ_j, the electron has to overcome the distance $\Delta r = r_j - r_i$ and the energy $\Delta \xi = \xi_j - \xi_i$. Since both energetic states are localized, hopping is a tunneling process. As it is additionally thermally activated, if the site j is higher in energy than the site i, hopping is often also referred to as 'phonon-assisted tunneling' [80], where both the energetic and the spatial distance are important.

The rate of hopping from site i to site j, expressed as ν_{ij}, can mathematically be described by the Miller-Abrahams formalism [81]:

$$\nu_{ij} = \nu_0 \exp\left(-2\alpha\Delta r\right) \cdot \exp\left(-\frac{\xi_j - \xi_i + |\xi_j - \xi_i|}{2k_B T}\right), \qquad (2.12)$$

where α is the inverse localization radius and ν_0 is the attempt-to-escape frequency, which is typically close to the phonon frequency [68]. Note that the argument of the second exponential becomes zero, if $\xi_j < \xi_i$ (downhill jump). In order to describe the charge transport across the entire film, a large number of hops has to be taken into account. This can be done in different
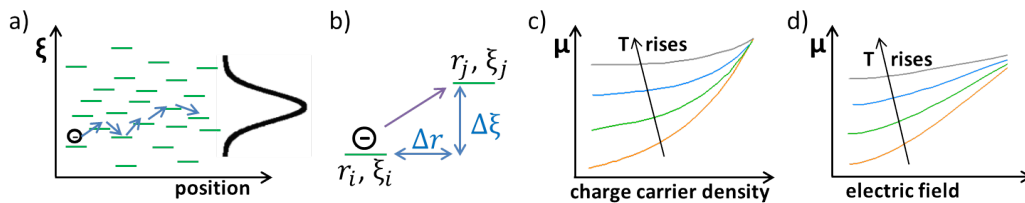
Figure 2.5: a) Sketch of an electron hopping between discrete energetic states upon the application of an electric field (tilting of states due to field is ignored). The Gaussian DOS is here centered at the LUMO level. b) Zoom into the energetic distribution focusing on two coupled sites i and j. Following the Miller-Abrahams formalism, a charge carrier must overcome the energy $\Delta\xi$ and the distance Δr to jump from site i to site j. c) Dependence of the charge carrier mobility in disordered organic semiconductors on the charge carrier density and the temperature. The curve is adapted from reference [44], where both axes are normalized and logarithmic. d) Dependence of the charge carrier mobility on the electric field for varying temperatures. The curve is also adapted from reference [44], where both axes are normalized and the plot is semi-logarithmic.

ways. One option is to use percolation theory [82–84]: each couple of sites in the DOS exhibits a microscopic conductance accounting for Equation 2.12. The goal is to find the critical (minimum) conductance, for which at least one percolation path across the film exists. Only site couples with a conductance higher than the critical conductance can contribute. Based on that, an exact numerical solution for the macroscopic conductivity and thus the mobility can be calculated. The shape of the Gaussian DOS and the occupation of the sites strongly impact on the value of the critical conductance. Since the charge carrier density, the temperature and the applied field all impact on the occupation of the Gaussian DOS (Fermi energy), the impact of these parameters on the conductivity is inherently included in this approach. The corresponding mathematical details will be given in Chapter 6, where the charge transport in the semiconducting polymer used in the memory diodes will be quantitatively described.

Alternatively, the Miller-Abrahams hopping formalism (Equation 2.12) can be integrated into the Pauli master equation, which reads [44]

$$\sum_{i \neq j} \left(f_i \left(1 - f_j\right) \nu_{ij} - f_j \left(1 - f_i\right) \nu_{ji} \right) = 0, \qquad (2.13)$$

where f_i is the probability that the site i is occupied, while $1 - f_j$ is the probability that the site j is unoccupied. The sum in Equation 2.13 only equals zero in equilibrium. In this case, the probabilities in Equation 2.13 follow Fermi-Dirac statistics. If an electric field is applied, the system is no longer in equilibrium and an additional contribution $\exp\left(-e \cdot E \cdot \Delta r\right)$ occurs in Equation 2.12. The mobility can be determined by numerically solving the master equation on a 3D cubic lattice [44]. The electronic structure of the polymer is explicitly taken into account, since the site energies are randomly picked from the Gaussian DOS. Regarding the spatial disorder, the hopping distance is usually in the range of the inter-site distance of the lattice, a, as the inverse localization length is in the order of $\alpha = 10/a$ [43]. The approach presented above is often referred to as extended Gaussian disorder model, since it is based on the Gaussian disorder model originally proposed by Bässler [85].

Both, the percolation and the master equation approach, provide an exact solution for the mobility. It can be shown that both solutions lead to an equivalent description for the mobility [86]. In order to make charge transport models more efficient, the exact mobility solution can be approximated with an analytical expression that includes the impact of the temperature, the electric field, the charge carrier density, the width of the density of states, σ, and the inter-site distance, a, in the polymer film [44, 86]:

$$\mu(p, T, E) \approx \mu(p, T) \cdot h(T, E), \qquad (2.14)$$

where the impact of hole density and temperature is expressed as

$$\mu(p,T) = \frac{a^2 q \nu_0}{\sigma} c_1 \exp\left(-c_2 \frac{\sigma^2}{(k_B T)^2}\right) \exp\left\{\frac{1}{2}\left[\left(\frac{\sigma}{k_B T}\right)^2 - \frac{\sigma}{k_B T}\right]\left(2pa^3\right)^\delta\right\}.$$
(2.15)

Here, $c_1 = 1.8 \cdot 10^{-9}$ and $c_2 = 0.42$. Moreover, the exponent δ reads

$$\delta = 2\frac{\ln\left[\left(\frac{\sigma}{k_B T}\right)^2 - \frac{\sigma}{k_B T}\right] - \ln(\ln 4)}{\left(\frac{\sigma}{k_B T}\right)^2}.$$
(2.16)

The influence of the electric field (combined with the temperature) on the mobility is described as

$$h(T,E) = \exp\left\{0.44\left[\left(\frac{\sigma}{k_B T}\right)^{3/2} - 2.2\right]\left[\sqrt{1 + 0.8\left(\frac{Eea}{\sigma}\right)^2} - 1\right]\right\}.$$
(2.17)

Note that $a = N_t^{-1/3}$ with N_t being the density of transport sites. The parametrized analytical expression for the mobility is very well described in literature [44, 86, 87]. But it is difficult to extract the main conclusions solely from Equations 2.14 - 2.17. Therefore, Figures 2.5c and d qualitatively illustrate the impact of charge carrier density, electric field, and temperature on the mobility.

In Figure 2.5c the mobility for a disordered organic semiconductors is plotted as a function of charge carrier density for varying temperatures (electric field is constant and low). The curve trends were adapted from reference [44], where both axes are normalized and logarithmic. For low charge carrier densities, the mobility strongly depends on the temperature. Since only a small portion of the Gaussian DOS is filled with charge carriers, a site i with a charge carrier has only very few neighboring sites j that allow hopping due to wave function overlap. It is however very likely that these sites exhibit higher energies, $\xi_j > \xi_i$. The resulting (high) energy barriers for hopping explain the strong temperature dependence: $\Delta\xi$ can be overcome more easily at high temperatures leading to a higher mobility.

On the other hand, if the charge carrier density is high, then the Gaussian DOS is filled to a large extent. Due to the shape of the DOS, a site i now has a lot of neighboring sites j, where the charge carrier could jump to as far as wave function overlap is concerned [86]. This means that it is also very likely that $\Delta\xi$ is small for at least one of these sites. As a consequence, the mobility is significantly less temperature-dependent at high charge carrier concentrations and, furthermore, by orders of magnitude higher compared to the situation at low charge carrier densities [43].

The impact of charge carrier density on the occupation of the DOS is schematically illustrated for low and high charge carrier densities in Figures 2.6a and b, respectively. Since hole transport is considered here, the DOS is centered at the HOMO level. Note that holes have to take up energy (from a phonon), if they want to jump down. Therefore, an increased filling of the DOS means that the Fermi level for holes is shifted downwards. The latter is the case in Figure 2.6b. A comparison of Figures 2.6a and b also reveals, why the mobility scales exponentially with $1/T^2$ for low charge carrier densities, while it scales exponentially with $1/T$ for high charge carrier densities [89]: in the case of low charge carrier density, the hole first has to jump down to an energy level, where hopping is possible. Since the first jump and hopping itself are both thermally activated, $\ln \mu \propto 1/T^2$. By contrast, if the charge carrier density is high (Figure 2.6b), the lowest lying holes are already at an energy level, where hopping is possible. Hence, the mobility-temperature dependence is Arrhenius-like: $\ln \mu = 1/T$.

In a similar way, the electric field-dependence of the mobility can be analyzed. Figure 2.5d shows the mobility as a function of electric field for varying temperatures (charge carrier density is low). For high electric fields, the temperature-dependence of mobility is very low. The reason is a Poole-Frenkel-like effect [90]. When a high field is applied, the energetic distribution of sites is tilted. Consequently, the energy barrier for hopping between two sites significantly decreases by a value that is proportional to the square root of the electric field. It should be noted that an additional field-dependence of the mobility at high fields has already been observed in early charge transport studies on organic semiconductors [91, 92]. For low electric fields, this effect does not play a role and the mobility strongly depends on the temperature (Figure 2.5d). It is worth mentioning that carrier concentration
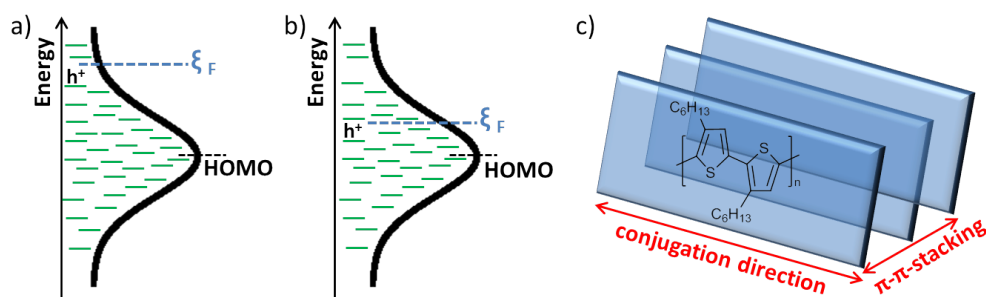
Figure 2.6: Fermi level position in a Gaussian DOS for a) low and b) high hole densities. Note that for holes downhill jumps are thermally activated. Hence, an increase of the hole-density means a downward shift of the Fermi energy level, ξ_F. c) Scheme of π-π-stacking in an organic semiconductor: a planar structure of a conjugated polymer, here poly(3-hexylthiophene), allows stacking of several macromolecular chains (blue rectangles). This can lead to enhanced intermolecular charge transfer (scheme adapted from reference [88]).

dependence of the mobility is considered to be dominant with respect to the field-dependence. The latter is especially important at low temperatures [93].

So far, the impact of the temperature, the charge carrier density and the field on the mobility have be discussed. Additionally, the inter-site distance, a, and the width of the DOS, σ, influence the charge transport (cf. Equations 2.15 and 2.17). It is obvious that a decrease of a increases the mobility, because the overlap of wave functions between neighboring sites and thus hopping is facilitated.

Regarding σ, the picture in Figure 2.6a implies that a decrease of σ leads to a higher mobility, because the smaller the width of the density of states, the less charges are needed to push the Fermi level to the transport energy level, where $\ln \mu = 1/T$ holds. A decrease of σ can be related to a higher order in the polymer film. In this context, the morphology of a semiconducting polymer has a great influence on the mobility [94]. Especially in field-effect transistors, it was shown that mobility can be orders of magnitude higher, if the polymer chains are aligned [95].

The reason is that intermolecular charge transfer, *i.e.* charge transfer between single macromolecular chains, is expected to be the current-limiting process. Alignment of the polymer chains enhances this kind of charge transfer and thus the mobility observed. This is schematically illustrated in Figure 2.6d, where a planar conjugated backbone structure of the semiconducting poly(3-hexylthiophene) is indicated as blue rectangle. Several of these structures are aligned enabling efficient intermolecular charge transfer due to this so-called π-π-stacking.

In this work, the focus will be on disordered polymers, but it should be noted that a lot of research has been dedicated in the last decades to the question, how order and mobility are related [96]. If the order is very good, even band-like transport can be found in organic semiconductors [97–99]. This especially holds for molecular crystals based on conjugated small molecules [71, 100, 101].

The discussion so far did not address the strong difference between electron and hole transport observed in organic semiconductors. Electron currents are often orders of magnitude lower [74]. The reason is trapping of electrons [102], the effect of which can be decreased to a large extent by blending the semiconductor with an insulating material [103].

Finally, it should be mentioned that, recently, charge transport models have been developed for organic semiconductors, which deliberately take into account the amorphous morphology of the polymer films [104]. The electronic structure of the polymer is then determined from the obtained morphology [104, 105] including the calculation of transfer integrals to obtain the hopping rates [106]. This approach is again finalized by solving the hopping

problem on a grid, where the sites represent the molecules in the corresponding morphology. This yields the mobility as a function of temperature, field and charge carrier density [107]. Note that instead of the Miller-Abrahams formalism, Marcus theory [108], where transfer integrals are inherently included, is typically used in this case to describe charge transfer. Importantly, a main conclusion of reference [107] is that the temperature and concentration dependence of mobility found in the extended Gaussian disorder model [44] is very similar despite the simplicity of its lattice model, which does not account for the detailed microscopic morphology of the polymer.

2.4 Charge injection at Schottky contacts

The interface between a metal and a semiconductor is called Schottky contact, when there is a significant energy barrier between the Fermi energy of the metal and the valence/conduction band of the semiconductor. Regarding organic semiconductors, a Schottky barrier for hole injection is for instance expected, when the energy barrier between the injecting electrode's Fermi level and the HOMO level of the polymer is above 500 meV.

Figure 2.7a shows a metal and a semiconductor before forming a contact. The difference between the Fermi level of the metal and the vacuum level is the work function, Φ_M, of the metal. It is the energy needed to release an electron from the metal into vacuum just above the surface of the metal [111, 112]. For the semiconductor, the energy needed to emit an electron from the HOMO level is called ionization potential (IP). The energy gained
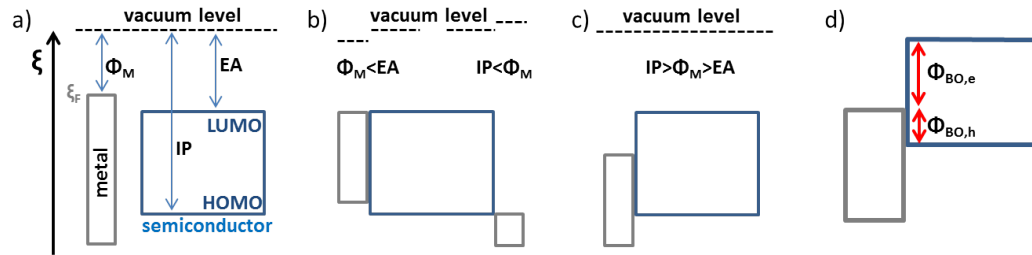
Figure 2.7: a) Energy levels of a metal and a semiconductor before the contact is formed. The work function of the metal, Φ_M, is the difference between the vacuum level and the Fermi level, ξ_F. The difference between vacuum level and the LUMO/HOMO level of the organic semiconductor is called electron affinity (EA)/ionization potential (IP). b) An Ohmic contact for electron transport is formed, when $\Phi_M < EA$ (left), and $\Phi_M > IP$ (right) yields the formation of an Ohmic contact for hole transport. In both cases, electron transfer occurs to align the Fermi level of the metal and the HOMO/LUMO [109]. c) Vacuum level alignment [110] occurs, when $EA < \Phi_M < IP$, and consequently, a Schottky contact is formed. d) The Schottky contact exhibits an energy barrier for the injection of holes ($\Phi_{B0,h} = \xi_F - \xi_{HOMO}$) and electrons ($\Phi_{B0,e} = \xi_{LUMO} - \xi_F$).

when the semiconductor takes up an electron from the vacuum level is called electron affinity (EA). Since the HOMO level is completely filled, the electron occupies the LUMO level. Note that care must be taken, when analyzing the electronic structure including HOMO, LUMO, EA and IP levels [113].

Figure 2.7b shows the energy level alignment at the metal-semiconductor contact for two different cases: on the left, $\Phi_M < EA$ holds before the contact is formed. Hence, when the two materials are brought together, electrons are transferred from the metal to the LUMO of the semiconductor until ξ_F and ξ_{LUMO} are aligned. An Ohmic contact for electrons is formed. On the right side of Figure 2.7b, $\Phi_M > IP$ holds before the contact is formed. It is thus energetically more favorable for electrons in the HOMO of the semiconductor to move to the metal electrode upon formation of the interface. Again, the electron transfer occurs until the Fermi level of the metal and the HOMO of the semiconductor are aligned leading to an Ohmic contact for hole transport. For both cases, the process at the interface is called Fermi level pinning [109].

By contrast, a situation, where the value of the work function is between the ionization potential and the electron affinity of the organic semiconductor ($IP > \Phi_M > EA$) is presented in Figure 2.7c. Here, Fermi level pinning cannot occur, because electrons can neither be transferred from the HOMO of the semiconductor to the metal nor from the metal to the LUMO of the semiconductor. Instead, the energy levels are pinned in such a way that the vacuum levels of the metal and the semiconductor align (vacuum level alignment) [110]. As a consequence, energy barriers both for electron injection ($\Phi_{BO,e}$) and hole injection ($\Phi_{BO,h}$) are formed as illustrated in Figure 2.7d.

In order to transfer charges from the metal to the semiconductor, the energy barrier needs to be overcome or passed. Two mechanisms are well-known for charge injection at a Schottky barrier: thermionic emission and field emission (barrier tunneling). The underlying physics behind these mechanisms will be discussed in the following. Moreover, the special aspects about charge injection into polymer semiconductors accounting for the disorder will be addressed and the model of van der Holst et al. [114] will be presented.

Thermionic emission is the first of the electrode-limited conduction mechanisms at Schottky contacts. Originally, it was derived to describe emission of electrons from a metal into vacuum (Richardson-Schottky equation). Later, it was adapted to metal-semiconductor contacts. The idea is that a charge carrier acquires sufficient thermal energy to overcome the barrier at the contact [115] and the injection-limited current density is expressed as [75]

$$J_{RS} = A^* T^2 \exp\left(\frac{\Phi_{B0} - \Delta\Phi}{kT}\right), \tag{2.18}$$

where A^* is the effective Richardson constant, $A^* = 4\pi q m^* k_B^2/h^3$, with m^* being the effective mass of the charge carrier and h being Planck's constant. As Equation 2.18 was originally applied to inorganic semiconductors, Φ_{B0} is the difference between the Fermi level and the valence or conduction band of the semiconductor. This energy barrier is decreased by $\Delta\Phi$, which comprises two components: an applied electric field and the image force effect. The latter is the decrease of the potential energy of an injected electron due to the Coulomb interaction with the remaining counter charge in the metal. The resulting position-dependent potential energy of an electron is sketched in Figure 2.8a. Additionally, the application of an electric field lowers the injection barrier, as presented in Figure 2.8b. The two effects lead to a position-dependent injection barrier, $\Phi_B(r)$, which reads [116]

$$\Phi_B(r) = \Phi_{B0} - \frac{q^2}{16\pi\epsilon\epsilon_0 r} - qEr, \tag{2.19}$$

where r is the distance from the electrode. The effective energy barrier, Φ_B, is the maximum energy barrier in Figure 2.8b. It can be determined by differentiating Equation 2.19, solving for r, and then inserting the resulting value. This leads to

$$\Phi_B = \Phi_{B0} - \Delta\Phi = \Phi_{B0} - \sqrt{\frac{q^3 E}{4\pi\epsilon_0\epsilon_r}}. \tag{2.20}$$

For low-mobility semiconductors, the situation is more complicated, because charges, which overcome the injection barrier, are likely to recombine with
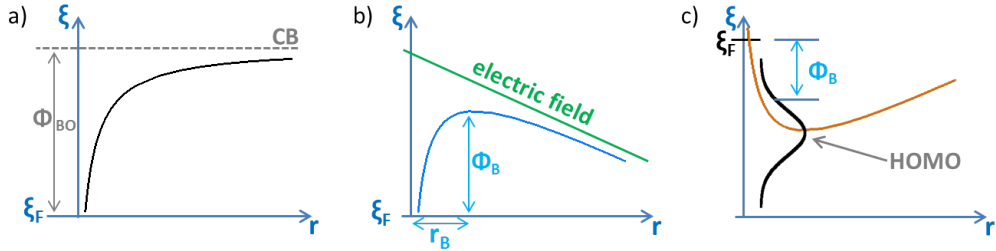
Figure 2.8: a) Position-dependent potential energy of an electron in the semiconductor close to the interface with a metal (Schottky contact). The image force effects decreases the actual barrier, Φ_{B0}, which is the difference between the metal's Fermi energy and the conduction band of the semiconductor. b) Effect of an applied electric field, which yields an effective injection barrier Φ_B (maximum position). c) Hole injection at the Schottky contact of an electrode and an organic semiconductor. Besides the image force barrier lowering and the effect of the applied electric field, the barrier is further decreased because of the Gaussian DOS. The first jump from the metal into the polymer can be into an unoccupied state of the DOS and thus the energy barrier is lower with respect to a band-like semiconductor. The curve was adapted from reference [116].

the electrode (counter charges) due to the low bulk-mobility. This process is often called back-diffusion [117] and the resulting diffusion-limited injection current at a Schottky barrier can be expressed as [118]

$$J = qN_V\mu E \exp\left(\frac{-\Phi_B}{k_B T}\right), \qquad (2.21)$$

where N_V is the effective density of states. As mentioned above, organic semi-conductors do not only exhibit low mobilities, but they are also disordered. This has an important consequence for the actual effective energy barrier of charge injection, which is lower than Φ_B (Equation 6.26). For hole injection for instance, the hole does not have to jump all the way down to the HOMO level of the semiconductor, but it can get to an unoccupied state of the Gaussian DOS. Since this state is energetically higher than the HOMO level, the energy barrier for the injection is lower. Figure 2.8c schematically illustrates the impact of the Gaussian DOS on the effective injection barrier. Note again that a hole has to take up energy to jump downwards. Since the DOS is not occupied down to the HOMO level (normal charge carrier concentration in the semiconductor), the actual barrier is decreased. A metal-semiconductor contact can still be Ohmic (for holes), if the energy barrier between Fermi level of the metal and the HOMO of the semiconductor is about 0.4 eV [119].

Barrier tunneling is another well-known electrode-limited conduction mechanism. Due to the importance of the electric field, it is often also called field emission. According to the Fowler-Nordheim model, which considers a triangular barrier, the current density across the interface (from the metal to the semiconductor) is expressed as [120]

$$J_{FN} = BE^2 \exp\left(\frac{8\pi(2m^*)^{1/2}\Phi_B^{3/2}}{3hqE}\right), \qquad (2.22)$$

where B is a constant. The importance of the electric field is obvious in Equation 2.22. The idea is that charge carriers do not overcome the barrier as in thermionic emission, but tunnel through it. Therefore, the probability of the charge carrier to pass the barrier plays an important role [121]. Since tunneling is a quantum mechanical effect, an accurate derivation of this injection process includes the electronic wave function of the charge carrier in the metal and in the semiconductor accounting for the barrier at the interface [122, 123]. The full derivation is beyond the scope of this work, but a few basic ideas shall be given in the following.

Looking at a Schottky barrier from a generalized point of view, current can flow from the metal to the semiconductor and from the semiconductor to

the metal. The overall current density is then the sum of both contributions [124]. The charge carrier flux from the semiconductor to the metal, J_{SM}, can for instance universally be described by [125, 126]

$$J_{SM} \propto q \int v_x \cdot \kappa(\xi) g(\xi) f(\xi) \partial \xi, \tag{2.23}$$

where v_x is the velocity of the charge carriers in the direction perpendicular to the interface and $\kappa(\xi)$ is the probability for the charge carrier to cross the barrier. The charge carrier density results, as usual, from the product of the DOS, $g(\xi)$, and the Fermi-Dirac distribution, $f(\xi)$. Note that Equation 2.23 can also serve as starting point for the derivation of the Richardson-Schottky equation (thermionic emission). In this case, $\kappa(\xi) = 1$ [127].

Regarding barrier tunneling, the tunnel probability is often described by the Wentzel-Kramers-Brillouin (WKB) approximation [128, 129]:

$$\kappa(r, \xi) = \exp\left(-\frac{4\pi}{h} \int_0^r \sqrt{2m^*|\Phi(r) - \xi|}\, \theta\left(\Phi(r) - \xi\right) \partial r\right), \tag{2.24}$$

where $\Phi(r)$ is the barrier potential energy and $\theta\left(\Phi(r) - \xi\right)$ is a Heaviside unity step function. Calculating the sum of both currents (from metal to semiconductor and *vice versa*), the total current density at the Schottky barrier due to tunneling, J_{tun}, can be written as [130, 131]

$$
\begin{aligned}
J_{tun} = \frac{A^* T}{k_B} \int_{-\infty}^{\infty} \kappa(r, \xi) \\
\times \left[\log\left(1 + \exp\left[\frac{\xi_F(r) - \xi}{k_B T}\right]\right) - \log\left(1 + \exp\left[\frac{\xi_F(0^-) - \xi}{k_B T}\right]\right)\right] \partial \xi,
\end{aligned}
\tag{2.25}
$$

where $\xi_F(r)$ is the position-dependent Fermi energy, r is the distance from the metal/semiconductor interface. Hence, $r = 0$ relates to the position exactly at the interface; 0^- is at the interface but inside the metal electrode, while 0^+ is at the semiconductor side of the interface. Note that Equation 2.22 results from Equation 2.25 [132], when a triangular potential well is assumed as done by Fowler and Nordheim [120].

Thermionic emission and barrier tunneling as defined in Equations 2.18 and 2.22 do not explicitly take into account that a semiconductor can also be amorphous. Organic semiconductors are disordered and therefore not characterized by bands but by discrete localized states distributed in energy according to a Gaussian function with width σ. The energetic distribution impacts on the actual effective energy barrier (Figure 2.8c), as discussed above.

Furthermore, the disorder is expected to influence on the exact charge injection mechanism in case of a Schottky barrier. The original derivations of thermionic emission and barrier tunneling are based on band-like transport in the semiconductor. These models were therefore considered inappropriate for (disordered) polymer semiconductors [115].

It was claimed that an injection model for organic semiconductors has to take into account that a carrier jumps from the metal to a localized state in the polymer [133]. After the charge carrier has reached a site in the polymer, it can recombine with the electrode or it can 'escape' into the semiconductor. The latter aspect has been mathematically included using an escape probability term [134–136].

In Section 2.3, charge transport within a polymer semiconductor was described as a sum of thermally activated hops between discrete sites. Similarly, charge injection can be considered as hopping from the metal to a localized state in the semiconductor close to the interface [137]. In this regard, the entire charge transport across the interface and the semiconductor has been treated using the Miller-Abrahams formalism [81]. The approach was developed by van der Holst and co-workers [114] and the corresponding Pauli master equation reads

$$\sum_{i \neq j, j \neq 1, m_x} \left(f_i \left(1 - f_j \right) \nu_{ij} - f_j \left(1 - f_i \right) \nu_{ji} \right) + \sum_{i \neq j, j = 1, m_x} \left(f_i \nu_{ij} - \left(1 - f_i \right) \nu_{ji} \right) = 0,$$

(2.26)

where the second sum describes the hopping from and to the electrodes, which are at the positions $i = 1$ and $i = m_x$. m_x corresponds to the size of the 3D box (lattice), across which the electric field is applied. The charge carrier density in the semiconductor at the interface is described by [114]

$$n_c = \int\limits_{-\infty}^{\infty} \frac{g^*(\xi)}{1 + \exp\left[\xi / k_B T\right]} \partial \xi,$$

(2.27)

where the DOS, $g^*(\xi)$, in this case takes into account the effective barrier at the interface, Φ_B, and reads

$$g^*(\xi) = \frac{N_t}{\sqrt{2\pi}\sigma} \exp\left(-\frac{(\xi - \Phi_B)^2}{2\sigma^2} \right).$$

(2.28)

It was shown that the injection-limited current density is well described by

$$J_{ILC} = J_0 h(E) \frac{eaE}{\sigma} \exp\left(-\frac{\Phi_B^*}{k_B T} + \left(\frac{1}{2} - c_2 \right) \cdot \frac{\sigma^2}{(k_B T)^2} \right),$$

(2.29)

where $c_2 = 0.42$ and J_0 is defined as $J_0 = \frac{e\nu_0}{a^2} \exp\left(-2\alpha a \right)$ [114]. The field-dependent functional $h(E)$ is described in Equation 2.17.

Note that although Equation 2.29 provides an excellent approach to model the charge transport in diodes comprising a Schottky contact, it has not yet been successfully applied to experimental data.

2.5   Ferroelectricity and ferroelectric polymers

As briefly discussed in Section 2.1, dielectric materials exhibit low conductivities and are thus insulating. It might therefore be surprising that they are still highly relevant in technological applications and particularly in electronics. As an example, dielectric materials with high dielectric constant, ϵ_r, are introduced between the two electrodes of a capacitor in order to enhance its capacitance, which can be written in a simplified way as

$$C = \frac{\epsilon_0 \epsilon_r A}{l}, \tag{2.30}$$

where A is the area of the device and l is the thickness of the dielectric. The capacitance describes the change of the electronic charges on the capacitor's electrodes, ∂Q, as linear response to the a change of the electric potential, $\partial \varphi$: $C = \partial Q / \partial \varphi$. A potential difference between the electrodes results in an electric field, $E = \Delta \varphi / d$, which causes the polarization of the dielectric: $\vec{P} = \chi \epsilon_o \vec{E}$. The different polarization mechanisms, such as electronic, ionic, or orientation polarization [138], are all included in the value of the susceptibility, χ. The electric displacement, $\vec{D}$, is the sum of the polarization of the vacuum and the dielectric:

$$\vec{D} = \chi \epsilon_o \vec{E} + \epsilon_o \vec{E} = (1 + \chi) \epsilon_o \vec{E} = \epsilon_0 \epsilon_r \vec{E}. \tag{2.31}$$

Both, χ and ϵ_r, are second-rank tensors. It should be noted that higher-order terms for the D-E relation exist, but these are not discussed here.

Considering standard polymers or glass, it is obvious that dielectric materials are not necessarily crystalline. Yet, structural order can impose additional features for dielectrics and enhance their functionality [139]. In general, crystals can be classified according to their symmetry [140]. 32 so-called point groups exits and 21 of these point groups are non-centrosymmetric meaning that the crystal structure does not contain an inversion centre [141]. The impact of a lack of inversion symmetry can be derived from Figure 2.9a, where a sketch of a 2D ionic crystal without inversion center is shown. In equilibrium, the charges are arranged such that there is no net dipole in the system, because the sum of all present dipoles is zero. However, upon application of a mechanical stress (Figure 2.9b), charges are shifted with respect

to each other and a net dipole moment as indicated by the green arrow rises. The coupling between the mechanical stress, S, and the resulting electric displacement, D, is called direct piezoelectric effect and it is mathematically defined as

$$D_i = d_{ikl}S_{kl}. \tag{2.32}$$

In this notation, the displacement, D_i, is a vector, which is coupled with the second-rank tensor of the mechanical stress, S_{kl}, via the piezoelectric coefficient, d_{ikl}, which is a third-rank tensor. In the remainder of this work, the tensorial treatment of physical parameters will be omitted, because it is not needed for the understanding of the concepts.

Three polar axes corresponding to the diagonals of the hexagonal structure can be seen in Figure 2.9a. Since these polarizations cancel each other out, the schematic structure is not polar from an outside perspective. Again, the symmetry is decisive for the crystal properties. In this regard, only 10 of the 21 non-centrosymmetric crystal classes mentioned above are also polar [144].

The ten polar classes all exhibit pyroelectric behavior, *i.e.* a change of polarization is induced by a change in temperature [145]. Importantly, not all of these ten polar space groups yield ferroelectric behavior, whereas every ferroelectric material is immediately also pyroelectric in nature. Figure 2.9c illustrates the interdependency between piezo-, pyro-, and ferroelectricity. Every pyroelectric is piezoelectric, but not every piezoelectric is also pyroelectric. Moreover, ferroelectric materials automatically show also pyroelectric and piezoelectric features, but not *vice versa*. The origin lies in the definition of ferroelectricity.
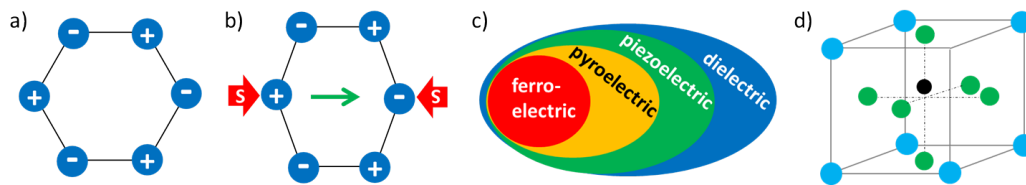
Figure 2.9: a) Scheme of a 2D piezoelectric crystal, where positive and negative charges are arranged in a hexagonal non-centro-symmetric structure. b) Upon application of uniaxial mechanical stress, S, the arrangement changes; the sum of all dipole moments in the system is no longer zero: a net polarization rises as a result of a mechanical force (direct piezoelectric effect). c) Relation between ferroelectric, piezoelectric and pyroelectric materials, which are all dielectrics. The picture was adapted from reference [142]. d) Tetragonal crystal structure of a ceramic ABO_3 compound (adapted from reference [143]). The light blue spheres correspond to A, which is twice positively charged. The green spheres correspond to twice negatively charged oxygen ions, O. The black sphere, which is above the center of the cuboid, represents the species B in the compound, which is four times positively charged.

A crystalline material is ferroelectric, when it exhibits a spontaneous polarization, which can be reversed by application of an electric field [146]. Note that pyroelectric materials do exhibit a net polarization of the crystal, but the polarization cannot always be changed by an electric field; that is why not all pyroelectric materials are also ferroelectric. An example of a unit cell of a ferroelectric crystal is presented in Figure 2.9d. This tetragonal perovskite structure can be found in ABO_3 compounds; a typical example is $BaTiO_3$.

In these compounds, eight ions of the species A sit in the corners of the cuboid and are twice positively charged (light blue spheres). Six of the twice negatively charged O-ions are located in the face centers (green spheres). Finally, the four times positively charged species B sits close to the center of the cuboid, but not in the center (black sphere). The off-center position is the reason, why the unit cell exhibits a net dipole moment and the crystal structure is polar. The material is ferroelectric, because the polarization (pointing upwards) can be reversed by an electric field pointing downwards, which is strong enough to shift the four times positively charged ion to the corresponding position slightly below the central point of the cuboid (a very instructive sketch is presented in Figure 1 of reference [147]).

In order to distinguish between the ferroelectric polarization of a crystal and the (linear) polarization, $\vec{P_{lin}}$, related to χ, the overall displacement of a ferroelectric crystal can be written as

$$\vec{D} = \chi\epsilon_o\vec{E} + \epsilon_o\vec{E} + \vec{P_s} = \vec{P_{lin}} + \epsilon_o\vec{E} + \vec{P_s}, \qquad (2.33)$$

where P_s is the spontaneous ferroelectric polarization. The two polarizations states 'up' and 'down' corresponding to the B species located above and below the center of the cuboid, respectively, are thermodynamically stable and equivalent [143]. The energy related to the switching is the product of the polarization and the applied electric field, $\Delta G = -\vec{E} \cdot \vec{P_s}$ [148].

It should be emphasized that if the ion was exactly in the center, then the unit cell would not be polar and the material would not be ferroelectric. This is typically the case at higher temperatures. Above the so-called Curie temperature, T_c, a nominally ferroelectric material becomes paraelectric, as the spontaneous polarization of the crystal vanishes.

The ferroelectric-to-paraelectric phase transition can be analyzed from a thermodynamic point of view. In order to explicitly address the impact of the polarization on the Gibbs free energy, G, the elastic Gibbs energy, $G_1 = G + E \cdot P$, is considered. The Taylor expansion of G_1 (at zero mechanical stress) yields [149]

$$G_1(T,P) = G_{10} + \frac{1}{2}a(T)P^2 + \frac{1}{4}bP^4 + \frac{1}{6}cP^6, \qquad (2.34)$$

where G_{10} is the energy for zero polarization and $a(T)$, b, and c are coefficients [150]. Only even terms appear in the Taylor expansion, as $G(T, P)$ is invariant upon polarization reversal [151]. In Equation 2.34, the full expansion was terminated after the sixth term.

The thermodynamically stable state is at the minimum of the free energy. Differentiating the free energy with respect to the polarization yields the electric field:

$$\frac{\partial G(T, P)}{\partial P} = E = a(T)P + bP^3 + cP^5. \tag{2.35}$$

Considering the G-P relation, G_0 is a stationary value and it is a minimum, if $a(T)$ is positive, because $\partial^2 G(T, P)/\partial P^2 = a(T)$ for zero polarization.

On the other hand, G_0 is a maximum, if $a(T)$ is negative. But since $G(T, P)$ must increase for very high values of P, the G-P relation must necessarily show (at least) one other stationary value for non-zero polarization. This is schematically illustrated in Figure 2.10a, which presents G-P curves for negative and positive values of $a(T)$. While the elastic Gibbs energy has two equivalent minima at non-zero polarization ($-P$ and $+P$) for $a(T) > 0$, the thermodynamically most stable state is at zero net polarization, if $a(T) < 0$ [152]. Hence, the sign of $a(T)$ determines, whether the crystal is in the ferroelectric or in the paraelectric state. The temperature dependence of the coefficient $a(T)$ is described by

$$a(T) = \frac{T - T_c}{C}, \tag{2.36}$$

where C is a constant and positive [150] (capital C to distinguish from the
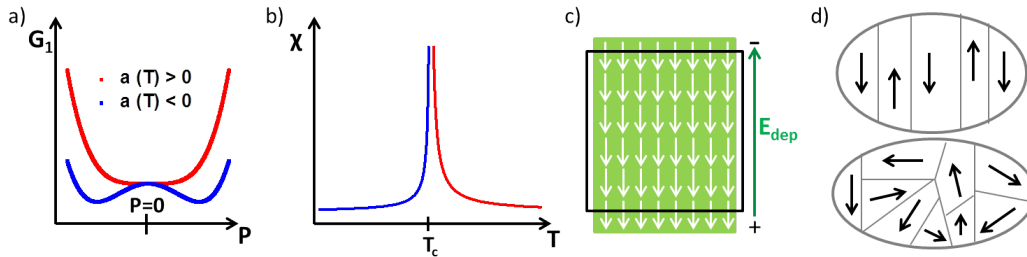
Figure 2.10: a) Relation between Gibbs elastic energy and polarization for the paraelectric state above the Curie temperature, T_c (red curve), and the ferroelectric state below T_c (blue curve). For the latter, two equivalent minima of the energy exist for non-zero ferroelectric polarization. b) Susceptibility of a ferroelectric material as a function of temperature. c) Sketch of depolarization field, $\vec{E_{dep}}$, resulting from uncompensated polarization charges at the surface of a ferroelectric material. White arrows indicate dipoles. d) Arrangement of domains in ferroelectric materials. Upper pictures shows 180° domain walls separating domains with opposite orientations (domains as black arrows). The lower picture shows an isotropic orientation of domains in a polycrystalline ferroelectric material before poling.

coefficient c). As mentioned above, T_c is the Curie temperature above which a ferroelectric behaves like a paraelectric [151]. Combining Equation 2.33 with Equations 2.35 and 2.36 yields the temperature dependence of the susceptibility, $\chi(T)$ [153]:

$$\frac{1}{\epsilon_0 \chi(T)} = \frac{\partial E}{\partial P} = \frac{\partial^2 G(T,P)}{\partial P^2} = \frac{T - T_c}{C}. \qquad (2.37)$$

This co-called Curie-Weiss law holds in the paraelectric state, when $T > T_c$ (P_s=0). In the ferroelectric state ($T < T_c$), where the crystal has a spontaneous polarization, the susceptibility follows [149, 154]

$$\chi(T) = \frac{1}{2\epsilon_0} \frac{C}{T_c - T}. \qquad (2.38)$$

Figure 2.10b schematically illustrates the temperature dependence of the susceptibility around the Curie temperature.

It is emphasized that the considerations above were made for the case of a second order phase transition. In this case, the coefficient b in Equations 2.34 and 2.35 is positive. By contrast, if $b < 0$, the phase transition is of first order [150]. Note that the coefficient c must generally be positive, because G should not approach $-\infty$ for increasing polarization.

So far, the discussion focused on one unit cell of a ferroelectric crystal. Looking at a bulk sample of a ferroelectric material, the polarization is normally not uniformly aligned. Instead, the material is made up of so-called domains, which are regions of uniform polarization. Two neighboring domains are separated by a domain wall. The driving force for domain formation is the lowering of the depolarization field energy. Considering a uniformly polarized ferroelectric material as illustrated in Figure 2.10c, the dipole moments are balanced in the bulk of the sample (black rectangle), but this is not the case at the interface. The uncompensated charges close to the interface cause a depolarization field opposing the orientation of the dipoles (white arrows). Without compensation, this field would cause depolarization. In a ferroelectric capacitor, the metal electrodes (plates) provide the counter charges to stabilize the ferroelectric polarization [30].

Figure 2.10d sketches as an example 180° domain walls (upper picture) that might be expected in a single-crystalline ferroelectric sample. In most of the cases, however, ferroelectric samples are not prepared as single-crystal but are polycrystalline. The lower picture of Figure 2.10d sketches the resulting random orientation of domains. As a consequence of the macroscopic isotropy, the ferroelectric material does not show a macroscopic polarization

in the as-prepared state. Only if the orientation of the domains is aligned by an electric field (poling [150]), the sample exhibits ferroelectric (and piezoelectric) behavior.

Ferroelectricity and piezeoelectricity are not restricted to inorganic materials. Different polymers have been shown to be ferroelectric, among them for instance nylon, cyanopolymers, and polyureas [155]. Although their ferroelectric parameters are inferior with respect to their inorganic counterparts, ferroelectric polymers received considerable attention in the last decades especially due to their excellent processability at low temperatures [158, 159].

The probably most famous and most widely used ferroelectric polymer is polyvinylidenefluoride (PVDF) together with its copolymers. The strong electronegativity of fluorine yields highly polar vinylidenedifluoride monomers with a dipole moment of 7×10^{-30} Cm (2.1 Debye) [160]. The chemical structure of PVDF is depicted in Figure 2.11a. The index n determines the number of repeating units along the backbone of the polymer. The carbon atoms are sp^3-hybridized and thus the C-F bonds and the C-H bonds can rotate with respect to each other around the carbon chain. Importantly, this rotation yields a flipping of the dipole orientation (Figure 2.11a) and is thus the mechanism for polarization reversal in PVDF.

Whether a PVDF film is ferroelectric or not depends on its crystal structure. Due the variety of chain and dipole arrangements that can be adopted, PVDF exhibits at least four well-identified polymorphs: α, β, γ, and δ [158]. The thermodynamically stable phase at ambient conditions is α. Figure 2.11b shows the projection of the monoclinic unit cell of α-PVDF along the c-axis [161], *i.e.* the direction along the carbon backbone of the polymer. Since
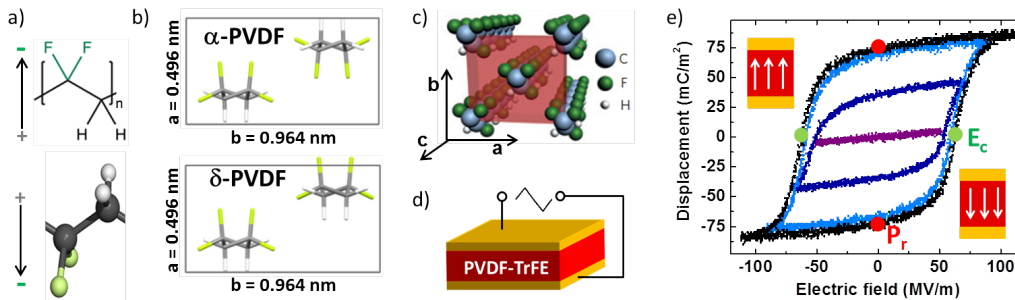
Figure 2.11: a) Chemical structure of polyvinylidene fluoride (PVDF) yielding a dipole moment that can be flipped. b) Unit cells of α-PVDF as well as of the δ-polymorph [156]. c) Three-dimensional crystal structure of P(VDF-TrFE) [157]. d) Sketch of a thin film capacitor, where P(VDF-TrFE) is stacked between two electrodes. e) The application of an alternating electric field (triangular wave form in d)) with sufficient amplitude allows the measurement of a ferroelectric hysteresis loop. The displacement at zero electric field is called remanent polarization, P_r. The field needed to reverse the polarization is called coercive field, E_c; it is extracted at zero displacement in the D-E curve.

the unit cell is centrosymmetric and the dipole moments exhibit antiparallel orientation, the α-phase is not polar and not ferroelectric [162]. By contrast, the other PVDF polymorphs (β, γ, and δ) are polar.

Since the polarization can be reversed by a sufficiently high electric field, these phases are also ferroelectric and concomitantly piezoelectric [163]. As an example, the unit cell of the δ-phase is sketched in the lower picture of Figure 2.11b [164]. Unlike in α-PVDF, the dipoles are oriented in the same direction in δ-PVDF [156].

Due to its excellent ferroelectric and piezoelectric properties, β-PVDF is the most pursued polymorph. The polarization of the unit cell, *i.e.* the overall dipole moment with respect to the volume, is about 130 mC/m^2 [163]. The main problem of this polymorph lies in the processing. Crystallization of PVDF from the melt or solution typically leads to the paraelectric α-phase. The β-phase can be obtained by biaxially stretching films, which were originally in the α-phase. However, this limits the product range to free-standing foils [156].

As the three-dimensional arrangement of polymer chains in crystalline structures is defined by van der Waals interactions, the size of fluorine and hydrogen atoms plays an important role [154]. In this context, it was demonstrated that the ferroelectric β-phase can directly be obtained from solution or from the melt, if the polymer contains monomers of trifluoroethylene (TrFE) [165, 166]. As a consequence, ferroelectric devices such as thin film capacitors [29] and ferroelectric field-effect transistors [167] based on the random copolymer of VDF and TrFE could be realized. The crystal structure of P(VDF-TrFE) is schematically illustrated in Figure 2.11c. Again, the *c*-axis corresponds to the direction along the carbon backbone of the macromolecules. The *b*-axis is parallel to the orientation of the polarization and the *a*-axis is perpendicular to *b* and *c*. The central effect of the TrFE units is that they introduce steric hindrance in the polymer causing the polar conformation of the chains to be favorable [154, 159, 160]. Another way of inducing β-phase formation is to blend PVDF with a second polymer, for instance poly(methyl metacrylate) (PMMA) [168–170].

Polarization reversal means switching of the dipolar orientation. One of the most important characteristics of a ferroelectric material in general is the hysteretic behavior of the displacement under an alternating electric field with sufficient amplitude. The latter is indicated for a P(VDF-TrFE) thin film capacitor in Figure 2.11d (triangular wave form). With the appropriate measurement setup (explained in the next chapter), a *D-E* hysteresis loop as presented in Figure 2.11e can be measured for the copolymer.

As part of the definition of a ferroelectric material, it exhibits non-zero polarization, even if the electric field is switched off. The displacement at

zero electric field is called remanent polarization, P_r. The electric field needed to switch the ferroelectric polarization is called coercive field, E_c, and it is defined as the field at zero displacement in a hysteresis loop (Figure 2.11e). For P(VDF-TrFE) a typical value for E_c is 50 MV/m [171], but it should be noted that the exact composition of the copolymer determines the ferroelectric properties [172]. A very instructive phase diagram for VDF-TrFE compositions is presented in Figure 3 of reference [171].

The remanent polarization of P(VDF-TrFE) is of the order of 70 mC/m^2 and thus a factor of five lower than for the most important inorganic ferroelectric, lead zirconium titanate (P_r of about 400 mC/m^2 [31]). One of the reasons for the big difference is that only about 50 % of a P(VDF-TrFE) film is crystalline [157]. The remaining amorphous regions cannot contribute to the ferroelectric response, as ferroelectricity in general is a collective phenomenon that requires long range order [173].

Moreover, P(VDF-TrFE) and inorganic perovskite based ferroelectrics exhibit also different behavior at the Curie-temperature. The ferroelectric-to-paraelectric phase transition is displacive for PZT, meaning that it is based on a displacive shift of the four times positively charged ion into the centre of the crystal structure. By contrast, for P(VDF-TrFE) the phase transition is of the order-disorder-type. Above the Curie temperature, the mobility of C-F bonds is so high that chain conformation becomes random and an amorphous isotropic alignment of the dipoles occurs [142, 171, 174]. Hence, the lack of ferroelectric response is then due to disorder.

The dynamics of polarization switching can mathematically be described by the Kolmogorov-Avrami-Ishibashi (KAI) model [175–177], where polarization reversal starts with the statistical formation of a large number of nucleation sites followed by homogeneous domain growth [178]. The change in polarization as a function of time, $\Delta P(t)$, is expressed as [179]

$$\frac{1}{2 \cdot P_r} \Delta P(t) = 1 - \exp\left(-\sum_i \frac{S_i}{S_0}\right), \qquad (2.39)$$

where S_0 is the area of the sample and S_i reflects the area of growing sporadic domains. The change of polarization is normalized with respect to $2P_r$. This normalized value equals 1 for complete polarization reversal. The basic assumption of the KAI model is that a domain can expand unrestrictedly after successful nucleation. Therefore,

$$S_i \propto (v \cdot t)^n, \qquad (2.40)$$

where v is a constant domain-wall velocity and t is the time. n is the Avrami index, which depends on the dimensionality of the domains. The normalized

change of polarization upon switching can then be written as a compressed exponential function:

$$\frac{1}{2 \cdot P_r} \Delta P(t) = 1 - \exp\left(-\left(\frac{t}{t_0}\right)^n\right). \tag{2.41}$$

According to the empirical Merz law [180], the switching time, t_0, is related to the activation field, E_{act}, and reads

$$t_0 = t_\infty \exp\left(\frac{E_{act}}{E}\right), \tag{2.42}$$

where t_∞ is the switching time at infinite applied field. The activation field scales inversely with the temperature: $E_{act} \propto 1/T$. Therefore, it is straightforward to conclude that polarization reversal in ferroelectric thin films is faster for large electric fields and for higher temperatures. The latter implies a decrease of the activation field.

Although Equations 2.39 - 2.42 were originally derived for inorganic ferroelectrics, they were shown to also be applicable to P(VDF-TrFE) [178, 179, 181]. This is remarkable taking into account that polarization reversal in P(VDF-TrFE) requires cooperative dipole switching across chains, which can only interact via van der Waals forces [178].

In this chapter, the basic theoretical concepts needed as background for this work have been discussed. Note that for the convenience of the reader, certain equations from this chapter will be given again later, when the theory is applied to the experimental results.

Chapter 3

Experimental

This chapter presents details on materials, device fabrication and characterization methods used in this work. The fabrication of bilinear arrays by solution micromolding is discussed in detail. Experimental methods used to investigate the resulting morphology and microstructure are addressed and explained. Subsequently, the fabrication of microstructured ferroelectric capacitors, patterned memory diodes and phase separated blend diodes is presented. The electrical characterization of the comprising capacitors and diodes with different measurement techniques is also described.

3.1   Materials

P(VDF-TrFE) is the abbreviation for the random copolymer of vinylidenefluoride and trifluoroethylene. Unless otherwise stated, it was used in the composition 65 mol% VDF and 35 mol% TrFE, which will be abbreviated in the following as 65:35. Besides, P(VDF-TrFE) with the compositions 80:20 and 50:50 were used as well. All three copolymer powders were purchased from Solvay. The values of the number- and weight-average molecular weight, M_n and M_w, were measured with gel permeation chromatography (GPC) versus polystyrene standards [182]. The values are listed in Table 3.1 together with the polydispersity (PD). Poly(vinyl alcohol) (PVA)
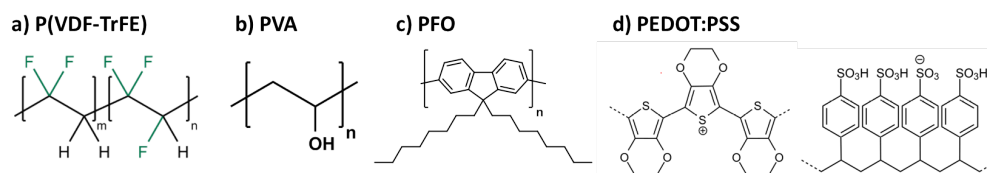
Figure 3.1: Chemical structure of a) P(VDF-TrFE), b) PVA, c) PFO and d) PEDOT (left) with PSS (right).

35

Table 3.1: Overview of polymers used in this work and their number- and weight-average molecular weight, M_n and M_w, as well as polydispersity (PD) values.

Polymer	M_w (kg/mol)	M_n (kg/mol)	PD
P(VDF-TrFE) (65:35)	365	145	2.51
P(VDF-TrFE) (80:20)	206	107	1.92
P(VDF-TrFE) (50:50)	221	77	2.84
PFO	1432	1195	1.2
PVA	27	12	2.25

was purchased from Sigma Aldrich. The semiconducting polymer poly(9,9-dioctylfluorene) (PFO) was bought from TNO/ Holst center (cf. Table 3.1). PEDOT:PSS, a waterborne latex of poly(3,4-ethylenedioxythiophene) stabilized with polystyrene sulfonic acid (Clevios P VP Al 4083) was purchased from Heraeus. The chemical structures of the functional polymers are presented in Figure 3.1. Dimethyl sulfoxide (DMSO), cyclohexanone, toluene, methyl ethyl ketone (MEK), and deionized water were used as solvents without further purification. The nonionic surfactant Zonyl®FSN-100 from DuPont could be added to solutions to enhance the wetting behavior on hydrophobic surfaces upon film processing.

It should be noted that solution concentrations will always be given in 'mg/ml' in this work. For instance, 120 mg/ml P(VDF-TrFE) in DMSO means that 120 mg of the copolymer was dissolved in 1 ml of DMSO.

Sylgard 184 silicone elastomer together with the curing agent for standard polydimethylsiloxane (PDMS) stamps was purchased from Dow Corning (USA). For the preparation of composite or so-called h-PDMS ('hard' PDMS) stamps, the following chemicals were purchased from abcr GmbH: (7-8 % vinylmethylsiloxane)-dimethylsiloxane copolymer, trimethylsiloxy terminated (CAS: 67762-94-1); platinum-divinyltetramethyldisiloxane complex in xylene (CAS: 68478-92-2); (25-35% methylhydrosiloxane) - dimethylsiloxane copolymer (CAS: 68037-59-2); 1,3,5,7-tetravinyl-1,3,5,7-tetramethylcyclo-tetrasiloxane (CAS: 2554-06-5).

3×3 cm^2 glass slides (Schott Borofloat®33) were used as substrates. They were manually cleaned with soap (Extran®MA 02, Merck Milipore), followed by ultrasonic treatment in deionized water, acetone, and 2-propanol. Afterwards, the substrates were subjected to UV/ozone treatment (UVOCS®) to remove any organic residues on the surface. For device fabrication, five 400 μm wide electrode lines could be thermally evaporated onto the glass substrates through shadow masks. Ag and Au purchased from Umicore were used as electrode materials and Cr (2 nm) served as adhesion layer.

3.2 Bilinear polymer arrays by solution micromolding and backfilling

Line gratings of functional polymers were prepared by solution micromolding, which was adapted from the well-known soft lithography technique 'micromolding in capillaries' [184–186]. These two methods will be compared in more detail in the next chapter. The process of solution micromolding and subsequent backfilling is schematically illustrated in Figure 3.2. A drop of solution of the first polymer is poured onto the cleaned substrate and a structured PDMS stamp is positioned on top. Afterwards, the substrate/stamp assembly is hot-pressed for 2 hours (hot-press from Paul-Otto Weber GmbH). For line gratings of P(VDF-TrFE), DMSO was used as solvent and typical concentrations were 150 mg/ml, the processing temperature was 140 °C. For PVA gratings, deionized water was used as solvent, concentrations were as high as 300 mg/ml and the temperature of the hot-press was 70 °C. The latter also applies to PFO, which was dissolved in toluene (5 mg/ml).
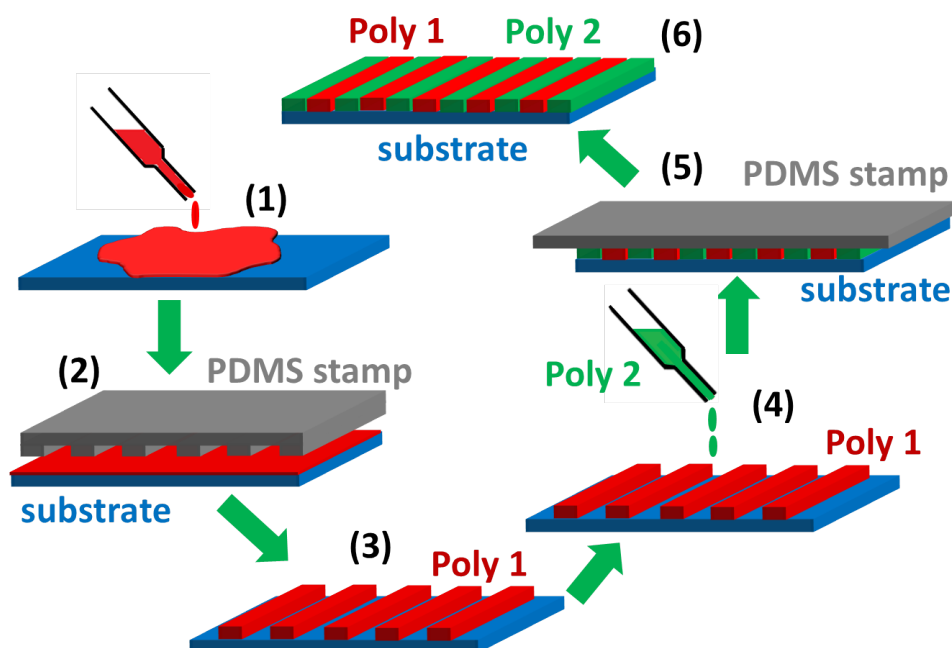
Figure 3.2: Schematic illustration of solution micromolding and backfilling [183]: the solution of a polymer is poured onto the substrate (1) and a PDMS stamp with relief structures on its surface is pressed onto the substrate surface (2) using a hot-press. After the solvent has fully evaporated, the stamp is removed and a complementary line grating of the polymer is obtained (3). The space in between the lines is then backfilled with a second polymer (4) by hot-pressing with a flat stamp (5), leading to a 'bilinear array' of two polymers (6).

In order to electrically characterize the gratings in actual devices such as capacitors, the empty space between the lines has to be backfilled. Therefore, a drop of the solution of the second polymer is poured onto the grating before hot-pressing with a flat unstructured PDMS stamp. This yields the bilinear polymer array after the solvent of the polymer (Poly 2) has evaporated.

3.3   Silicon masters and stamp preparation

Solution micromolding requires micro- and nanostructured PDMS stamps. They are typically replicated from a so-called master, *i.e.* a single-crystalline silicon wafer patterned for instance by photolithograpy. The master can repeatedly be used many times for the preparation of stamps. Different masters with anti-sticking coating were purchased from NIL Technology (Denmark) and used as received. One of the 4" silicon masters has a pitch width and height of 1.3 µm and 2 µm, respectively and a period of 4 µm. Scanning Electron Microscopy (SEM) in cross section was performed for this master and the corresponding micrograph is shown in Figure 3.3a. The second 4" silicon master exhibits a pitch width of 2 µm, a line height of 500 nm, and the period was again 4 µm. The third silicon master consists of nine fields with different structures. All structures show a line height of 500 nm and the period is about twice the pitch width, which is varying from 2 µm down to 200 nm. An optical image of this master is presented in Figure 3.3b. Stamps complementary to the master grating were prepared from PDMS.
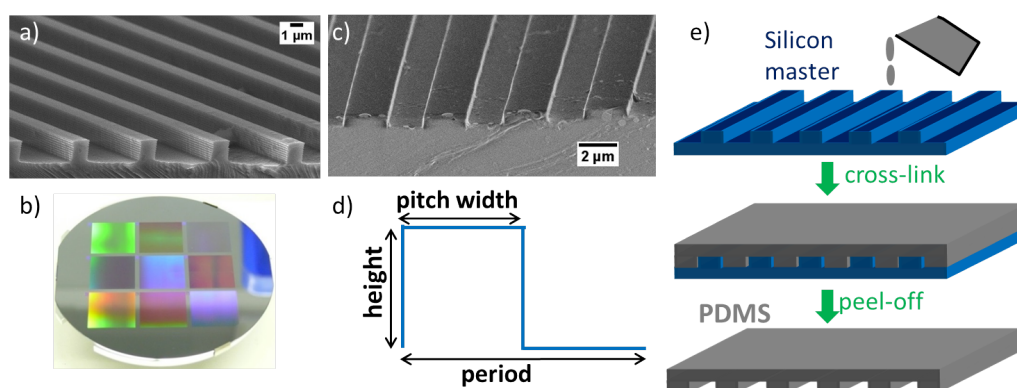
Figure 3.3: a) SEM micrograph (cross section) of a piece of the silicon master with a line height of 2 µm, a pitch width of 1.3 µm, and a period of 4 µm. b) Optical image of the silicon master with 9 different fields (area of 2x2 cm² each) with varying pitch width. c) SEM micrograph (cross section) of a PDMS stamp with a line height of 500 nm, a pitch width of 2 µm, and a period of 4 µm. d) Explanation of the terms 'pitch width', 'line height' and 'period'. e) Schematic illustration of the stamp preparation process.

Figure 3.3c shows the cross-sectional SEM micrograph of a PDMS stamp with pitch width of 2 µm, a line height of 500 nm, and a period of 4 µm. These three terms defining the structure of the stamp/master are explained in Figure 3.3d. The preparation of a stamp is schematically illustrated in Figure 3.3e. Sylgard 184 silicone elastomer was mixed with the corresponding curing agent in a ratio of 10:1 by weight. The mixture was then cast on the master (in a petri dish) followed by evacuation in a desiccator in order to detrap air bubbles. After curing for 3 hours at 60 °C (cross-linking), the PDMS stamp can be peeled off from the master.

PDMS cannot be used to prepare accurate stamps for a pitch width below 1 µm due to its high viscosity. To that end, composite or h-PDMS ('hard' PDMS) stamps were prepared following a recipe from literature [187, 188]. 6.8 g of the vinyl-precursor (CAS: 67762-94-1, cf. section 3.1) were mixed with 30 mg of the platinum catalyst (CAS: 68478-92-2) and 30 mg of the crosslinker (CAS: 2554-06-5). After stirring, 2 g of the methylhydrosiloxane precursor (CAS: 68037-59-2) were added, the mixture was stirred again and degassed. Immediately afterwards, the mixture was spin coated onto the master (1000 rounds per minute, 40 s), followed by annealing for 2 minutes at 60 °C. Subsequently, a stirred and degassed Sylgard 184 mixture was poured on top and the stamp was baked for 5 hours at 70 °C. In the composite stamp, the low viscosity mixture provides high accuracy. Since this part of the stamp is brittle after curing, 'normal' PDMS is poured on top during the processing and later serves as soft and elastic backbone of the stamp.

3.4 Thin film processing

Besides bilinear arrays, polymer thin films were also prepared in this work, for instance for reference thin film capacitors or for organic ferroelectric memory diodes comprising phase separated blend films. Two techniques were used for thin film processing: spin coating and wire-bar coating.

Spin coating was carried out with a LabSpin6 TT from Suss MicroTec. Therefore, a cleaned substrate is fixed on a chuck (vacuum). Then, the solution is applied on the substrate and homogeneously distributed by the rotation of the chuck. A typical process was the preparation of a P(VDF-TrFE) thin film with a thickness of about 500 nm. Therefore, a solution of 40 mg/ml (MEK) was used and the chuck was first rotated at 500 rounds per minute (rpm) for 10 seconds, before it was rotated for two minutes at 1500 rpm (film drying). The film thickness resulting from spin coating can be controlled by adjusting the polymer solution concentration and the rotation speed.

Wire-bar (Mayer rod) coating was performed with a K202 control coater (RK PrintCoat Instruments Ltd, UK). Since the substrate temperature can be accurately controlled, homogeneous films with low roughness can be realized [39]. This even applies to phase separated blends of PFO and P(VDF-TrFE), which tend to show a very high roughness [170]. Mayer rod-coating is a well-established process in the coating industry [169, 189] to obtain high quality films.

In this work, blend films of about 300 nm thickness were prepared by wire-bar coating. The powders of P(VDF-TrFE) and PFO were mixed in a ratio 9:1 by weight and then dissolved in cyclohexanone. A typical concentration was 45 mg of the mixture in 1 ml of the solvent. Proper dissolution occurred at 80 °C under vigorous stirring (magnetic stirrer).

A cleaned substrate (also UV/ozone treated) was put onto the heated plate (80 °C) of the wire-bar coater and fixed with two sacrificial glass slides. The idea is that the wire-bar starts its movement on top of the first adjacent glass slides, then moves over the actual substrate, and stops on top of the second adjacent glass slide after the substrate. Using these two sacrificial glass slides, the solution can be homogeneously distributed over the entire sample.

Immediately before the automated movement of the wire-bar with constant speed is started, the solution is poured in front of the rod. Due to the gap between substrate and the wires of the rod, the movement of the rod enables the distribution of the solution over the substrate. Note that the thickness of the wet film is determined by the temperature of the plate, as well as the applied speed and the dimensions of the wire, which is wound around the bar. Another advantage of wire-bar coating is that only small amounts of solution (60 µl) are sufficient to cover the substrate.

3.5   Topography and polymer analysis

The topography and the morphology of the polymer line gratings and thin films were characterized with atomic force microscopy (AFM), scanning electron microscopy (SEM), and surface profilometry. For structural characterization and phase identification, X-ray scattering and photoluminescence (PL) spectroscopy were performed. The polymer powders were analyzed by differential scanning calorimetry (DSC). All these methods will be described in the following.

Atomic force microscopy (AFM) was carried out in tapping mode using a Nanoscope Dimension 3100 (Bruker) and Si tips with Al backside coating.

The force constant of the cantilever was 26 N/m and the resonance frequency was about 270 kHz. For thin films, the scan frequency was typically 0.5 Hz, meaning that one line was scanned back and forth within two seconds. By contrast, the gratings with line heights larger than 1 μm were measured with frequencies as low as 0.1 Hz to obtain accurate topography measurements.

In an AFM measurement, the surface of a sample is scanned with a tip mounted to a cantilever. In this regard, the tip can be in contact with the surface or slightly above the surface, where it still 'feels' the forces of the sample. The latter is called non-contact mode and one special case of this is intermittent or tapping mode. The cantilever is vibrated by an actuator. The cantilever oscillates close to its resonance frequency. When in contact with the surface, the free oscillation of the cantilever is damped and thus the amplitude of the oscillation is decreased.

The measurements in this work were performed in so-called constant-amplitude operation. In order to keep the (damped) amplitude constant while scanning over the surface, the feedback loop moves the cantilever up or down by means of a piezoelectric element. The signal for the feedback is provided by a laser, which is focused onto the cantilever in such a way that the reflected beam hits a photodiode sensor. The change in the height position, which the piezoelectric element applies to the cantilever to keep the amplitude constant, serves as the desired height signal of the measurement.

The three-dimensional (3D) data were processed using the software *Gwyddion*. The pictures are shown as 2D images, where x- and y position define the probed area. The height is color-coded. Excellent reviews on the principles of AFM can be found in literature [190, 191].

Surface profilometry was performed with a Dektak XT from Bruker. In order to determine the film thickness, a thin line was scratched into the film and the height measuring lever of the profilometer was moved across the scratch, which penetrates the entire film. The film thickness is the height difference between the plateau of the film and the trench level of the scratch (substrate).

Low voltage scanning electron microscopy (LVSEM) measurements were performed using a Zeiss 1530 Gemini. The substrates with the gratings or thin films were imaged as delivered for top-view micrographs. Cross-sectional SEM micrographs could be obtained after mechanically breaking the substrates. Therefore, the samples were typically cooled down in liquid nitrogen before breaking to guarantee a neat surface of the break. The primary beam voltage was usually in the range of 100 - 800 V. Higher voltages could be applied after coating with 5 nm of sputtered Pt.

Energy dispersive X-ray (EDX) spectroscopy was used to perform element mapping of bilinear polymer arrays. EDX was carried out with a Hitachi SU8000 SEM in combination with a Bruker XFlash5010 Silicon Drift Detector. Micrographs for imaging were acquired at accelerating voltages up to 1 kV. Higher voltages could be applied after coating with 5 nm of sputtered Pt.

X-ray scattering was performed in two different configurations: specular wide angle X-ray diffraction (XRD) measurements were carried out using a Philips PW1820 diffractometer with Cu radiation. The diffractograms of P(VDF-TrFE) gratings and thin films were plotted as intensity versus the scattering angle 2θ. The spacing, d, corresponding to the distance between crystallographic planes can be calculated using Bragg's law:

$$\lambda = 2d\sin(\theta), \tag{3.1}$$

where λ is the wavelength of the incident X-ray.

Grazing incidence wide angle X-ray scattering (GIWAXS) of PFO line gratings and a reference thin film was carried out at the DELTA Synchrotron using beam line BL09 with a photon energy of 10 keV ($\lambda = 1.2398$ Å). The beam size was 0.05 mm x 0.5 mm and samples were irradiated just below the critical angle for total reflection with respect to the incoming X-ray beam (about 0.11°). The scattering intensity was detected on a 2-D image plate (MAR-345) with a pixel size of 150 µm (2300 x 2300 pixels) and the detector was placed 325 mm from the sample center. Data analysis was performed using the *Datasqueeze* software. Note that for these experiments, silicon wafers with 500 nm thermally grown oxide were used as substrates instead of glass. It is crucial for the measurement that the above mentioned angle of the incident beam is above the critical angle for the substrate. This is the case for Si/SiO_x.

Photoluminescence (PL) measurements were performed for the PFO line gratings and the reference thin film. The PFO reference thin film (on glass) was obtained by spin coating a solution of 20 mg/ml (toluene) at a rotation speed of 1000 rpm for 20 s, followed by rotation at 250 rpm for one minute. The film thickness amounted to about 190 nm. For PL measurements, the samples were exited with a wavelength of 400 nm using the frequency-doubled output from a Ti:Sapphire laser (Coherent, Libra HE 3.5 mJ, Vitesse 750 mW), which supplies 100 fs pulses with a repetition rate of 1 kHz. The laser fluence was about 1 µJ/cm^2. The PL emission spectrum was detected by a streak camera (Hamamatsu C5680). All experiments were performed at ambient temperature under a dynamic vacuum of about 10^{-4} mbar. Since

the different phases of PFO, which correspond to different structural configurations, exhibit different photoemission, PL measurements allow phase identification, when comparing the obtained spectra to reports in literature [192, 193]

Differential scanning calorimetry (DSC) measurements were performed by using a Mettler-Toledo 822/400 DSC with a modular measurement unit. The heating rate was 10 K/min (up to 473 K). Afterwards, the sample was cooled down to ambient temperature with the same negative heating rate, before it was heated up again to 473 K using a heating rate of 10 K/min. Comparing the first and the last heating cycle, conclusions about the properties of the polymer powder (typically 10 mg) can be drawn.

In DSC [194], two chambers are heated and the temperature shall increase with the same rate. One chamber contains a reference material, while the sample is in the second chamber. The heat flow needed to heat up the chambers is measured. If the tested polymer undergoes, for instance, an endothermic phase transition, then the heat flow in the chamber with the polymer is higher compared to the chamber with the reference material. In a DSC thermogram the difference of the heat flow between the two chambers is plotted versus the temperature. Melting of a semicrystalline polymer causes an endothermic negative peak in the curve, while recrystallization (upon cooling) causes a positive exothermic peak.

3.6   Device fabrication

In this section the fabrication of capacitors and diodes will be described. In all cases, the idea is that a functional layer or a bilinear array is stacked between two (perpendicular) metal lines, which serve as electrodes. The overlap of the two lines defines the device area. The processing conditions for solution micromolding and backfilling used for the device fabrication will be recalled briefly here. Further details can be found in Section 3.2.

3.6.1   Fabrication of microstructured capacitors

2 nm of Cr and 50 nm of Au were thermally evaporated on cleaned glass substrates through shadow masks at pressures below $8 \cdot 10^{-7}$ mbar and with rates of about 0.25 Å/s and 10 Å/s. The five lines (width of 400 µm) serve as Au bottom contact for the capacitors. Subsequently, P(VDF-TrFE) line gratings were prepared on the substrate by solution micromolding. PDMS stamps with pitch width of 2.7 µm and height of about 2 µm were used.

The concentration for P(VDF-TrFE) in DMSO was 150 mg/ml. The gratings were backfilled with PVA (up to 500 mg/ml in deionized water). Note that water as solvent for PVA is ideal for the backfilling procedure, because it does not dissolve P(VDF-TrFE) and it also does not swell the PDMS stamp. Device fabrication was finalized by thermal evaporation of Au top contacts again through shadow masks, which were aligned perpendicular to the original orientation of the bottom contacts. The resulting device area amounted to 0.16 mm^2.

Inverted arrays and the corresponding capacitors were fabricated as follows: A drop of a 300 mg/ml solution of PVA was placed onto the substrate comprising Au bottom electrodes and a PVA line grating was obtained by solution micromolding (two hours, 70 °C). Then, the PVA grating was backfilled with P(VDF-TrFE) using again a flat unstructured PDMS stamp at a temperature of 140 °C. Note that DMSO could not be used for backfilling, because it dissolves PVA. Instead, MEK was used and a typical concentration was 60 mg/ml. Top Au electrode evaporation finalized the processing.

For comparison, benchmark capacitors were fabricated with an unpatterned P(VDF-TrFE) thin film exhibiting a thickness of about 500 nm. The film was obtained by spin coating a 40 mg/ml solution of the copolymer (cf. Section 3.4). Afterwards, the film was annealed at 140 °C for 2 hours, because this was shown to enhance the crystallinity and thus the ferroelectric performance of P(VDF-TrFE) [157]. This is also the reason why solution micromolding as well as backfilling of P(VDF-TrFE) were always performed at 140 °C for 2 hours. For optimum comparability, Au served as bottom and top electrode also for the benchmark capacitor.

3.6.2 Fabrication of patterned memory diodes

The first approach for the patterned memory diodes was to use solution micromolding to obtain gratings of P(VDF-TrFE), which were then 'filled' by spin coating PFO on top. Ag bottom electrode lines (with Cr as adhesion layer) were first evaporated on cleaned glass substrates. Then, solution micromolding with only 60 mg/ml P(VDF-TrFE) in DMSO was carried out using in this case stamps with 2 µm pitch width, 4 µm period and 500 nm line height. The thickness of the functional layer between the electrode was deliberately chosen to be lower compared to the microstructured capacitor to allow device operation at lower voltages. A PFO solution of 20 mg/ml (toluene) was spin coated on top of the P(VDF-TrFE) grating. The diode fabrication was finished by evaporation of Ag top electrodes.

For patterned memory diodes comprising bilinear arrays without undesired overlayers, the process scheme was inverted. First, PFO line gratings

on glass substrates comprising Au electrodes were obtained by solution micromolding. The solution concentration was 5 mg/ml of PFO in toluene. Subsequently, the grating was backfilled with 120 mg/ml P(VDF-TrFE) in DMSO using a flat unstructured stamp and the hot-press at 140 °C for two hours.

The devices described in this work were not fabricated in a clean room environment but in standard ambient conditions. Hence, when using evaporated top metal electrodes, the yield of the devices was low. The yield could be significantly improved by using PEDOT:PSS as top electrode. This polymer conductor was spin coated on top of the bilinear array of PFO and P(VDF-TrFE) with a speed of 250 rpm for 10 s followed by drying at a spinning speed of 1500 rpm for 50 s. A few drops of the nonionic surfactant Zonyl were added to PEDOT:PSS prior to spin coating to prevent dewetting. Afterwards, 50 nm Au lines were thermally evaporated through a shadow mask. The Au lines served as self-aligned mask for the removal of PEDOT:PSS by reactive ion etching: oxygen plasma was applied for three minutes at a pressure of 0.1 mbar using a Flecto plasma chamber (from plasma technology, Germany). Thickness measurements before and after the treatment showed that the PEDOT:PSS top film was removed, where it was not protected by Au lines. Hence, PEDOT:PSS indeed serves as top contact of the memory diodes, but it does not cause cross-talk between single diodes, because it is completely removed in the regions between diodes.

3.6.3   Fabrication of phase separated blend diodes

Memory diodes with a phase separated blend of P(VDF-TrFE) and PFO as the active layer were in most cases fabricated by wire-bar coating. Typically, 162 mg of P(VDF-TrFE) was mixed with 18 mg of PFO and the mixture was dissolved in 4 ml cyclohexanone at 80 °C under vigorous stirring. Before use, the solution was typically filtered using a Rezist^{TM}filter unit (Whatman, Teflon) with a pore size of 1 μm. A cleaned substrate with Au bottom electrodes was put onto the heated plate (80 °C) and about 60 μl of the blend solution was coated with a rod speed of 8 cm/s. The process was performed in a closed chamber, where the humidity could be controlled. However, due to the high plate temperature, the impact of humidity is anyway negligible.

The dried film was then annealed for two hours at 140 °C in a vacuum oven to enhance the ferroelectric performance of P(VDF-TrFE). Subsequently, device fabrication was either directly finished by thermal evaporation of Au top electrodes yielding symmetric memory diodes (Au bottom and top contacts). Alternatively, PEDOT:PSS was spin coated first followed by evaporation of Au lines, which define the device area, and subsequent reactive ion etching to

locally remove PEDOT:PSS. In the second case, PEDOT:PSS serves as top contact of the memory diode. Figure 3.4a shows the image of a sample with 25 memory diodes. Here, the active layer, a phase separated blend film of PFO and P(VDF-TrFE) was indeed obtained by wire-bar coating. The alignment of bottom and top contacts is in a cross-bar array, but the single diodes were electrically disconnected from each other before the measurements to avoid effects of cross-talk.

For memory diodes with thicker films, spin coating was used for the film processing. Therefore, the substrate was fixed on the chuck and then heated with a heat gun up to 50 °C, before the solution was applied. Films were spin coated at 2000 rpm for 60 s followed by rotation at 250 rpm for 20 s. In order to achieve a variation in film thickness, the concentration of the blend solution was varied between 36 and 45 mg/ml (cyclohexanone) yielding films in the range between 300 and 500 nm.

In order to analyze the charge transport in PFO, hole-only diodes with PEDOT:PSS bottom contacts and molybdenum oxide, MoO_x, top contacts were fabricated and characterized. PEDOT:PSS was spin coated on glass slides with patterned indium-tin-oxide bottom electrodes. The ITO patterns have different size to allow fabrication of hole-only diodes with different device areas. A solution of PFO (20 mg/ml in toluene) was spin coated on top of PEDOT:PSS (1000 rpm for 10 s followed by 250 rpm for 60 s). As top contact, 10 nm MoO_x capped with 100 nm Al was evaporated through shadow masks. Only for the hole-only diodes, film processing and the subsequent measurements of the diodes were carried out in a nitrogen-filled glovebox. Note that sample cleaning was performed in a clean room to minimize any leakage current.
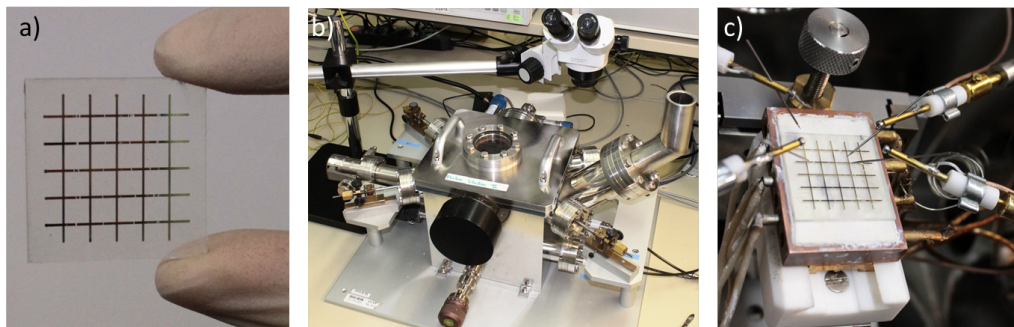
Figure 3.4: a) Image of typical sample with 25 memory diodes arranged in a cross-bar array. Note that the single diodes were always electrically disconnected from each other before the measurements by cutting the top Au lines to avoid cross-talk issues. b) Picture of the probe station. The sample is mounted on a plate, which is connected to a cryostat and heating element. c) Image of a contacted sample within the probe station.

3.7 Electrical characterization

In this section, the methods for electrical characterization will be described. Capacitors were characterized by Sawyer-Tower and shunt measurements as well as with small voltage impedance analysis. The memory diodes were characterized by current-voltage (I-V) measurements and data retention analysis. Moreover, impedance analysis was also carried out for the organic ferroelectric memory diodes. For all measurements, the samples were introduced to a probe station, which will be described first.

An optical image of the entire probe station is shown in Figure 3.4b. Samples were positioned on a plate, which can be moved in both x- and y-direction. The plate is connected to a cryostat, parts of which can be seen on the right of Figure 3.4b. Moreover, the plate itself could be heated. Hence, the temperature could be varied conveniently between 200 K (cooling with liquid nitrogen) and 400 K (Oxford Intelligent Temperature Controller ITC 4). To ensure thermal contact, a layer of heat conducting paste was applied between plate and substrate. All measurements were were performed in dynamic vacuum of 10^{-6} mbar to exclude any effects from degradation of the samples in ambient. The devices were contacted with probes as shown in Figure 3.4c.

Sawyer-Tower measurements were performed using a Tektronix AFG3022B function generator, a LeCroy waverunner LT372 oscilloscope and a Krohn-Hite 7602M wide-band amplifier. The setup is schematically illustrated in Figure 3.5a. The function generator (FG) provides a triangular waveform, which defines the frequency (typically 100 Hz or 1 kHz). The bias is then amplified and applied to the ferroelectric capacitor, which is in series with a reference capacitor. The bias applied to the circuit is measured as a function of time (triangular waveform on the left) by the first channel of the oscilloscope (*Ch 1*). The voltage drop over the reference capacitor is measured as a function of time by the second channel of the oscilloscope (*Ch 2*). The transient is shown in Figure 3.5b (blue curve). If the reference capacitance is known, the amount of charges on the reference capacitor can be calculated. This amount is equivalent to that of the ferroelectric capacitor, because both elements are in series. Therefore, the displacement can be determined by dividing the charge by the capacitor's area. The electric field is the applied voltage divided by the thickness of the ferroelectric film. Ferroelectric hysteresis curves can be shown, by plotting the displacement as a function of the applied electric.

Note that the capacitance of the reference capacitor should be orders of magnitude higher than the capacitance of the ferroelectric capacitor. Then,

the voltage measured for *Ch 2* is approximately equivalent to the voltage over the ferroelectric capacitor, because the voltage drop over the reference capacitor is very small and can be disregarded.

Shunt measurements (also called switching current measurements) are very similar to Sawyer-Tower measurements. The only difference is that the reference capacitor is replaced by a resistor. This is indicated by the red rectangle in Figure 3.5a. A reference resistor replaces the reference capacitor. As a consequence, the second channel of the oscilloscope then shows the voltage over the reference resistor as a function of time (Figure 3.5a). In this case, the charge is determined by integrating the switching current over time. Again, this charge is equivalent to the charge on the ferroelectric capacitor.

Impedance analysis was performed using a Schlumberger Si 1260 Impedance Analyzer. In this measurement, an alternating voltage ($V(t)$, sinusoidal waveform) is applied to the device and the resulting current as a function of time, $I(t)$, is measured. The ratio between voltage and current amplitude is the complex impedance, Z. The lateral shift between the two curves is called 'phase'. If the current is shifted by 90° with respect to the applied voltage, then the measured device is a very good insulator. By contrast, for a conductive material, the phase is typically zero. Assuming that the capacitor can be modeled as a perfect capacitor in parallel with a perfect resistor,
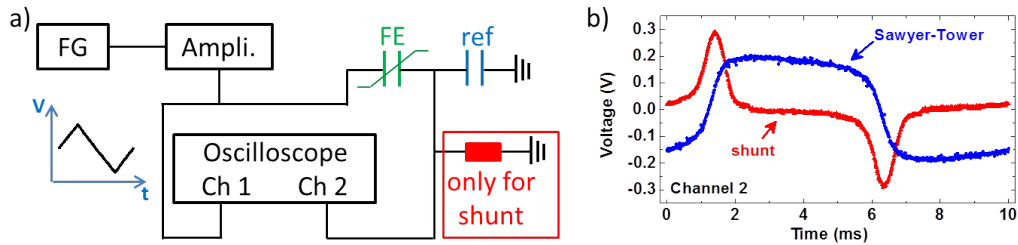
Figure 3.5: a) Schematic of the Sawyer-Tower measurement setup, which was originally reported for the first time in 1930 [195]. A triangular waveform provided by a function generator (FG) is amplified (Ampli.) and applied to the ferroelectric capacitor that shall be investigated. The ferroelectric capacitor is in series with a reference capacitor, the capacitance of which is high and known. The connected oscilloscope measures two voltage transients. Channel 1 (*Ch 1*) measures the voltage applied over the entire circuit, while Channel 2 (*Ch 2*) measures the voltage drop over the reference capacitor. Since the capacitance is known, the charge can be determined, which has to be equivalent to the charge on the ferroelectric capacitor, because both are in series. Based on that, the ferroelectric displacement can be determined. The Sawyer-Tower measurement setup can be transformed into a shunt measurement setup by simply replacing the reference capacitor by a reference resistor. b) Voltage as a function of time measured by (*Ch 2*) of the oscilloscope in case of a Sawyer-Tower (blue curve) and a shunt measurement (red curve).

the capacitance can be determined from impedance measurements as follows. The current is the time-derivative of the charge, Q, which again depends on the capacitance, C:

$$I(t) = \frac{\partial Q}{\partial t} = \frac{\partial}{\partial t} C \cdot U = C \frac{\partial U}{\partial t}. \tag{3.2}$$

Considering that $U(t) = U_0 \exp(i\omega t)$ with U_0 being the constant voltage amplitude and ω being the angular frequency, the impedance of a perfect capacitor is

$$Z(t) = \frac{U(t)}{I(t)} = \frac{U_0 \exp(i\omega t)}{C \frac{\partial U}{\partial t}} = \frac{U_0 \exp(i\omega t)}{U_0 \cdot C \cdot i \cdot \omega \exp(i\omega t)} = \frac{1}{i\omega C}. \tag{3.3}$$

The impedance of a normal ('real') capacitor is modeled by setting the perfect capacitor in parallel with a perfect resistor (resistance R) and the total impedance, Z_{tot}, reads

$$Z_{tot} = \left(\frac{1}{R} + i\omega C \right)^{-1}. \tag{3.4}$$

By measuring the impedance and the phase, the capacitance can be calculated. The dielectric constant can then be determined from the simple equation of a capacitor (Equation 2.30):

$$\epsilon_r = \frac{C \cdot l}{\epsilon_0 A}, \tag{3.5}$$

where A is the area of the plate capacitor and l is the thickness of the dielectric (the distance between the plates of the capacitor).

Current-voltage measurements were performed using a 4155B Semiconductor Parameter Analyzer from Hewlett Packard and an Agilent Easy Expert Software Package. The minimum leakage current, when both probes of the micromanipulators were in contact with the bottom and top electrode of the device, was 1 pA at a bias of 1 V.

For measurements at low temperatures, the cryostat was filled with liquid nitrogen. Using the heat control unit, the temperature was successively decreased. Measurements were only performed, when the temperature was stable for about five minutes. The same holds for measurements at higher temperatures. Note that a thermal joint paste was introduced between the sample and the plate of the probe station to guarantee optimized heat transfer.

Only the PFO hole-only diodes were analyzed with a different setup, namely a Keithley 2400 source meter controlled with LabView software.

Chapter 4

Microstructured ferroelectric thin film capacitors

In this chapter the technology is established that is later implemented into the fabrication of organic ferroelectric memory diodes. The process is called solution micromolding and it is adapted from micromolding in capillaries [184, 196]. Solution micromolding is used to prepare line gratings of the ferroelectric P(VDF-TrFE). Approaches to pattern this polymer have been reported, but the obtained microstructures and nanostructures were typically characterized only locally, for instance by piezo-force microscopy [54, 197]. By contrast, it is one key objective of this work to analyze the physics of the micropatterns in actual devices, here a thin film capacitor

Therefore, it is crucial that the micromolded grating is backfilled with a second polymer. If the empty space between the lines of P(VDF-TrFE) remained unfilled, thermal evaporation of the top electrode would lead to electric shorts. Surprisingly, backfilling procedures have hardly been investigated in literature so far. Here, bilinear arrays are realized by backfilling the obtained grating with the non-ferroelectric and insulating poly(vinyl alcohol) (PVA). Stacking the bilinear array between Au bottom and top electrodes, the P(VDF-TrFE) micropattern can be electrically characterized in the resulting capacitor.

In order to complete the study, inverted arrays are also fabricated and studied in capacitors. In this case, micromolded PVA gratings are first obtained by solution micromolding followed by backfilling with P(VDF-TrFE). All bilinear arrays exhibit topography; the polymer patterned first always protrudes. The consequences for the electric characteristics are investigated considering that the electrical equivalent circuit is a linear capacitor of PVA in parallel with a ferroelectric capacitor of P(VDF-TrFE). The key results presented in this chapter were published in *Physica Status Solidi A* [183].

4.1   Solution micromolding

Micromolding in capillaries (MIMIC) is a promising technology that allows solution-based patterning of microstructures and nanostructures [196]. It is compatible with large area solution processing on flexible substrates, and therefore, it was expected to be an ideal technique for the fabrication of microstructured devices as aimed in this work.

MIMIC was first introduced by the Whitesides group in 1995 [184]. In the beginning, it was only utilized to pattern polymers, but later it was also applied to ceramics [198]. MIMIC belongs to the group of soft lithography techniques [185]. The term 'soft' is used, because all these techniques rely on a structured elastomeric stamp, typically made from polydimethylsiloxane (PDMS) [199]. The stamp is obtained by casting the precursor components onto a reusable master followed by curing [200]. Afterwards, the stamp can be peeled off the master; the procedure is described in detail in Section 3.3.

In Figure 4.1a the process flow of MIMIC is schematically illustrated. The structured PDMS stamp is brought in conformal contact with a substrate. Then, a polymer solution is poured onto the substrate in vicinity of the open cavities of the stamp. The solution is soaked into these cavities due to capillary forces. The driving force for the capillary filling is the minimization of the total surface energy [184, 196]. The filling rate depends on different factors and follows [201]

$$\frac{dz}{dt} = \frac{R_H \left(\gamma_{SV} - \gamma_{SL} \right)}{4\eta z}, \tag{4.1}$$

where z is the length of the channel and γ_{SV} and γ_{SL} are the solid/vapor and the solid/liquid interfacial free energies, respectively. η is the viscosity and R_H is the hydraulic radius, which corresponds to the ratio between the volume and the surface area of the capillary. The filling rate increases with decreasing viscosity. However, low viscosities are often related to low solution concentrations, which may lead to incomplete filling. High concentrations and low viscosity can both be achieved, if MIMIC is carried out at elevated temperatures [202].

The solvent acts as carrier for the transport of the polymer through the channel; the solvent finally evaporates and escapes together with the trapped air either through the other opening of the cavity or by diffusion through the porous PDMS [196]. A line grating remains on the substrate after removal of the stamp.

Figure 4.1c shows a sample, where MIMIC was carried out at about 110 °C using a concentration of 25 mg P(VDF-TrFE) in 1 ml dimethyl-sulfoxide (DMSO). DMSO was chosen as solvent, as it does not swell the

PDMS stamp [203]. The solution was applied on both sides of the cavities
and small gratings were formed at both edges. The height and width of each
P(VDF-TrFE) lines were about 1.2 μm and 1.5 μm, respectively. However,
the solution transport was limited to only a few mm. Most of the area that
was in contact with the stamp does not show a grating. A variety of con-
centrations and temperatures was systematically tested, but in all cases, the
area covered with a homogeneous grating was very small. This is probably
due to the rather high surface tension of DMSO of about 43 mN/m [204],
which provides a low thermodynamic driving force for capillary filling.
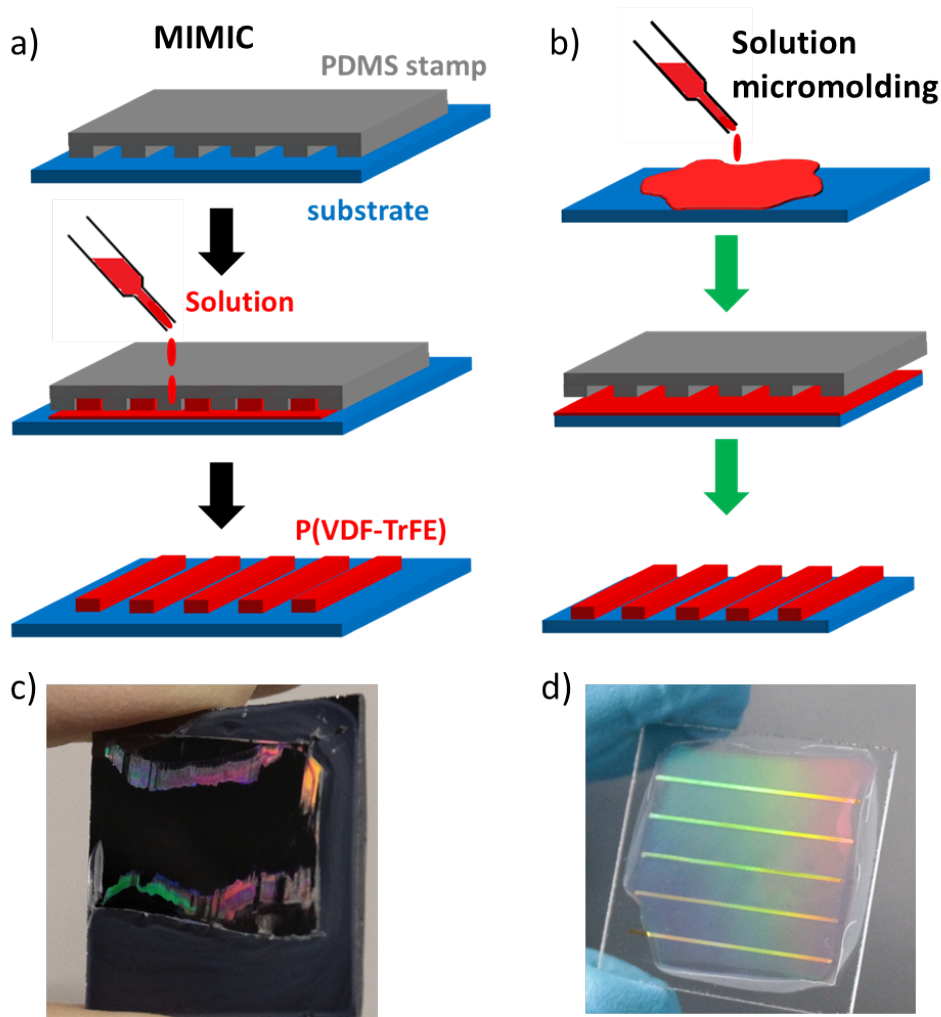
Figure 4.1: Schematic illustration of a) micromolding in capillaries (MIMIC) and b)
solution micromolding. c) Photograph of P(VDF-TrFE) grating on a Si substrate ob-
tained by MIMIC. d) Photograph of P(VDF-TrFE) grating on a glass substrate prepared
by solution micromolding. The glass substrate shows Au lines typically used as bottom
electrodes in devices (*e.g* memory diodes or thin film capacitors).

It is worth noting that problems with incomplete filling and discontinuous lines were also reported for PVDF gratings patterned by MIMIC [205]. For the successful fabrication of patterned devices larger areas need to be covered. To that end, the process of MIMIC was slightly altered in this work. The adapted technology is called solution micromolding and and it is schematically illustrated in Figure 4.1b. A drop of solution is poured onto the substrate and then, a structured PDMS stamp is pressed onto the substrate surface using a hot-press at elevated temperatures. It should be noted that the film is still wet, when the pressure is applied. Therefore, solution micromolding significantly differs from nano-imprint lithography (NIL) [206, 207], where a stamp or master is pressed into a dry film. In NIL, shear forces play an important role, while solution micromolding, like MIMIC, relies on capillary forces. The advantage of solution micromolding with respect to MIMIC is that it is not limited by solution transport, because the solution is distributed over the entire substrate surface before the stamp is applied and capillary forces come into play.
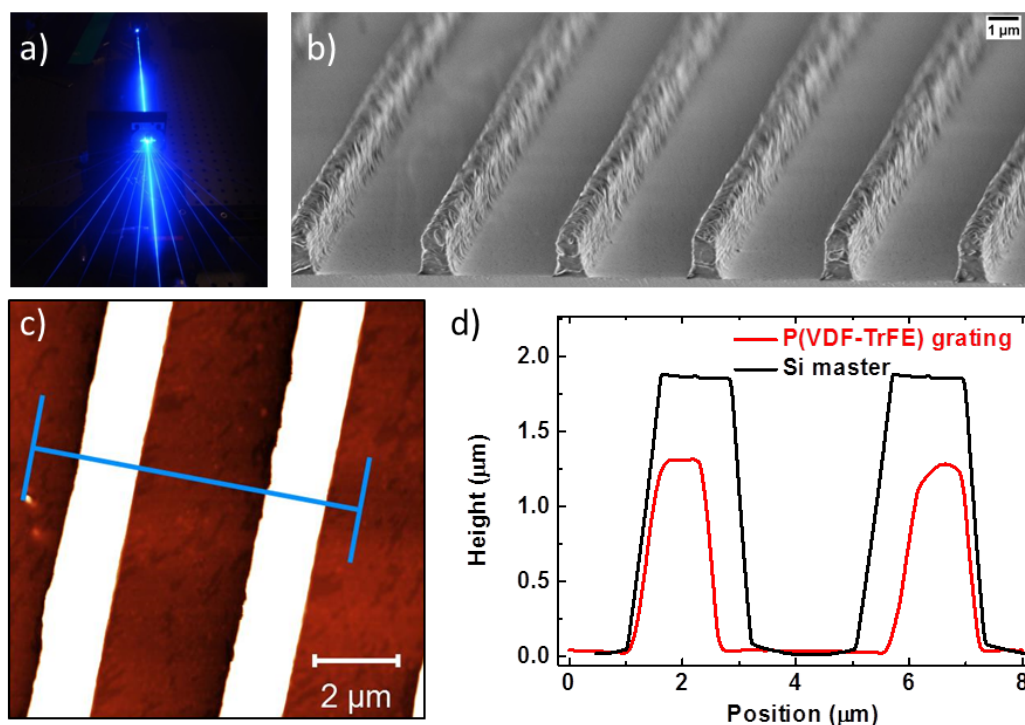
Figure 4.2: a) Laser diffraction experiment with a P(VDF-TrFE) line grating prepared by solution micromolding. The experiment was carried out at Imperial College London. b) SEM and c) AFM micrographs of a grating obtained with a concentration of 150 mg/ml P(VDF-TrFE) in DMSO. The range of the color-coded height scale in c) is 160 nm. d) Profile line extracted from c) and profile line extracted from the AFM measurement of the silicon master for comparison.

Figure 4.1d shows the photograph of a line grating of P(VDF-TrFE) obtained by solution micromolding. Note that the lines show similar height and width as the structures resulting from MIMIC (Figure 4.1c), but this time a homogeneous pattern is achieved over an area of more than 2x2 cm^2.

The topography of the gratings can be analyzed with atomic force microscopy (AFM) or scanning electron microscopy (SEM). Measurements for both techniques will be discussed in the following. Moreover, the grating is an ideal candidate for laser diffraction experiments as illustrated in Figure 4.2a.

4.2   Characterization of line gratings

A cross-sectional SEM micrograph of a micromolded P(VDF-TrFE) line grating is presented in Figure 4.2b. The pattern is highly homogeneous and periodic, although the width of the lines is lower than the empty space in between. This is due to the silicon master used for the first experiments: the pitch width was less than half the period (Figure 3.3a).

Figure 4.2c shows an AFM micrograph of the same grating and the indicated profile line (blue) is presented in Figure 4.2d together with a profile line extracted from the AFM measurement of the silicon master. The lines of the grating are about 1.25 μm high and exhibit an average width of about 1.3 μm. Hence, the features are smaller than those of the master.

Considering a solution with a concentration of 150 mg/ml, the polymer makes up for about 8 % of the solution's volume (the density of P(VDF-TrFE) is taken as 1.87 g/cm^3 [208]). Assuming that the solution completely fills the cavity of the stamp upon solution micromolding, a single line of the grating should make up for 8 vol% of the master's feature after the solvent is fully evaporated. However, a comparison of the integrals in Figure 4.2d reveals
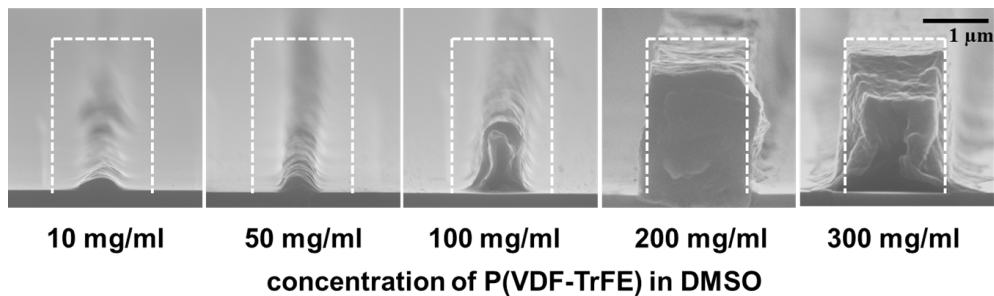
Figure 4.3: SEM micrographs of micromolded P(VDF-TrFE) lines fabricated with different concentrations of P(VDF-TrFE) in DMSO [183]. The dotted line represents the shape of the cavity in the stamp. The measurements were performed at Imperial College London. The scale bar is shown on the upper right.

that the cross-sectional area of the micromolded lines is about 50% of that of the master. The significantly higher fill factor can be explained by capillary forces, which also play a very important role in solution micromolding. Again, the advantage with respect to MIMIC is that even such polymer solutions can be used, which exhibit poor pattern replication in MIMIC due to a high surface tension.

The solution concentration is a key parameter of solution micromolding. Figure 4.3 shows cross-sectional SEM micrographs of the gratings obtained with various concentrations. At a high concentration of 300 mg/ml, an almost complete filling of the cavity indicated by the dotted line was obtained. However, due to the high viscosity of the solution, a thin P(VDF-TrFE) film is left in between the lines. Such a thin film might interfere with the electrical characterization of capacitors and is thus undesired.

The residual film is not present at low concentrations, however, below 100 mg/ml the filling is incomplete and replicated lines are discontinuous. The optimum concentration is around 150 mg/ml (grating in Figure 4.2b). The lines are then continuous and there is hardly any debris in between the lines. The height of the patterns is about 1.2 µm, which is the maximum thickness for convenient electrical characterization in capacitors.

Another important parameter for solution micromolding is the molecular weight. If the molecular weight is low, then higher concentrations are needed to obtain gratings with similar feature sizes. The corresponding study is presented in the Appendix.

The morphology of the gratings can be investigated with both AFM and SEM. Figure 4.4a shows an AFM micrograph of the top surface of a typical line grating. For comparison, an AFM micrograph of a reference thin
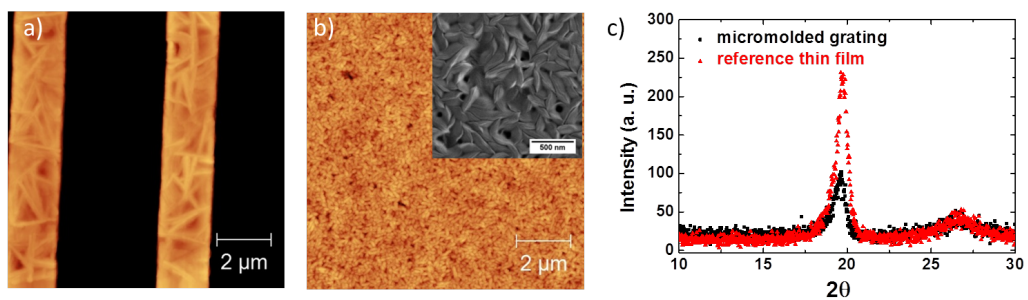
Figure 4.4: a) AFM micrograph of micromolded P(VDF-TrFE) grating obtained with a concentration of 20 wt% of the copolymer in DMSO. The range of the color-coded height scale is 160 nm focusing on the top surface of the grating. b) AFM micrograph of a thin P(VDF-TrFE) film prepared by spin coating. The film was annealed at 140 °C; the film thickness amounted to about 400 nm. The color-coded height scale is 85 nm. The inset shows an SEM micrograph of the same film [183]. The scale bar is 500 nm. c) Specular XRD measurement of the pattern and the reference thin film.

film obtained by spin coating is depicted in Figure 4.4b. It shows a typical post-annealing microstructure with small rice-like domains [157]. This is confirmed by the SEM micrograph included as inset.

By contrast, the size of the crystals in the micromolded grating (Figure 4.4b) is much larger. The origin presumably is Ostwald ripening; the coarsening originates from the presence of solvent in the cavity of the stamp at elevated temperature.

Specular XRD measurements of the micromolded grating and the reference thin film are presented in Figure 4.4c. Both spectra show a peak at 19.7° corresponding to the β-phase of P(VDF-TrFE). Hence, solution micromolding at 140 °C provides the ferroelectric phase of P(VDF-TrFE), which is a prerequisite for the fabrication of a ferroelectric capacitor.

4.3   Bilinear polymer arrays by backfilling

In order to analyze their ferroelectric properties in actual devices, the gratings have to be backfilled. Poly(vinyl alcohol) (PVA) was used as electrically insulating (non-ferroelectric) polymer. For backfilling, a drop of the PVA solution was poured onto the grating followed by hot-pressing at 70 °C with a flat unstructured PDMS stamp (schematic in Figure 3.2). Water was used as solvent, because it does not dissolve P(VDF-TrFE) and it also does not swell the elastomeric stamp.

Figure 4.5a shows a cross-sectional SEM micrograph after backfilling. The amorphous PVA densely fills the space between the semicrystalline P(VDF-TrFE) lines. It should be emphasized that there is no sign of a PVA overlayer on top of P(VDF-TrFE). On the contrary, the bilinear array of the two polymers shows topography, as the height of the backfilled PVA features is lower than that of the original P(VDF-TrFE) grating. The initial micromolded grating protrudes and the aspect ratio of the array is about 1:2. The filling increases with the concentration of the PVA solution. However, at very high concentrations the viscosity is so high that the PVA overflows the P(VDF-TrFE) gratings. A thick overlayer is formed, which needs to be avoided. As a compromise between filling and processability a concentration of 500 mg/ml PVA in water can be used.

In order to confirm that PVA is perfectly interdigitated with the P(VDF-TrFE) grating, element mapping was performed using energy-dispersive X-ray spectroscopy (EDX). Figure 4.5b shows the top view SEM micrograph of the bilinear array and the corresponding EDX image is presented in Figure 4.5c. The presence of F atoms (fluorine), which only occur in P(VDF-TrFE) and not in PVA, is indicated in blue. PVA contains oxygen atoms

(unlike P(VDF-TrFE)), which are indicated in green. PVA is confined between the P(VDF-TrFE) lines; the EDX analysis again suggests that there is no overlayer of PVA on top of P(VDF-TrFE). This is further substantiated by thickness measurements using a DEKTAK profilometer. The thickness values before and after backfilling are identical.

In order to find out, whether solution micromolding plus backfilling is generic in the creation of bilinear arrays, the process flow can be inverted. First, a line grating of PVA was obtained using solution micromolding (30 wt%, 70 °C). Subsequently, the grating was backfilled with P(VDF-TrFE) using a flat unstructured PDMS stamp (140 °C). 2-butanone was used as solvent in this case, because DMSO is also a solvent of PVA.
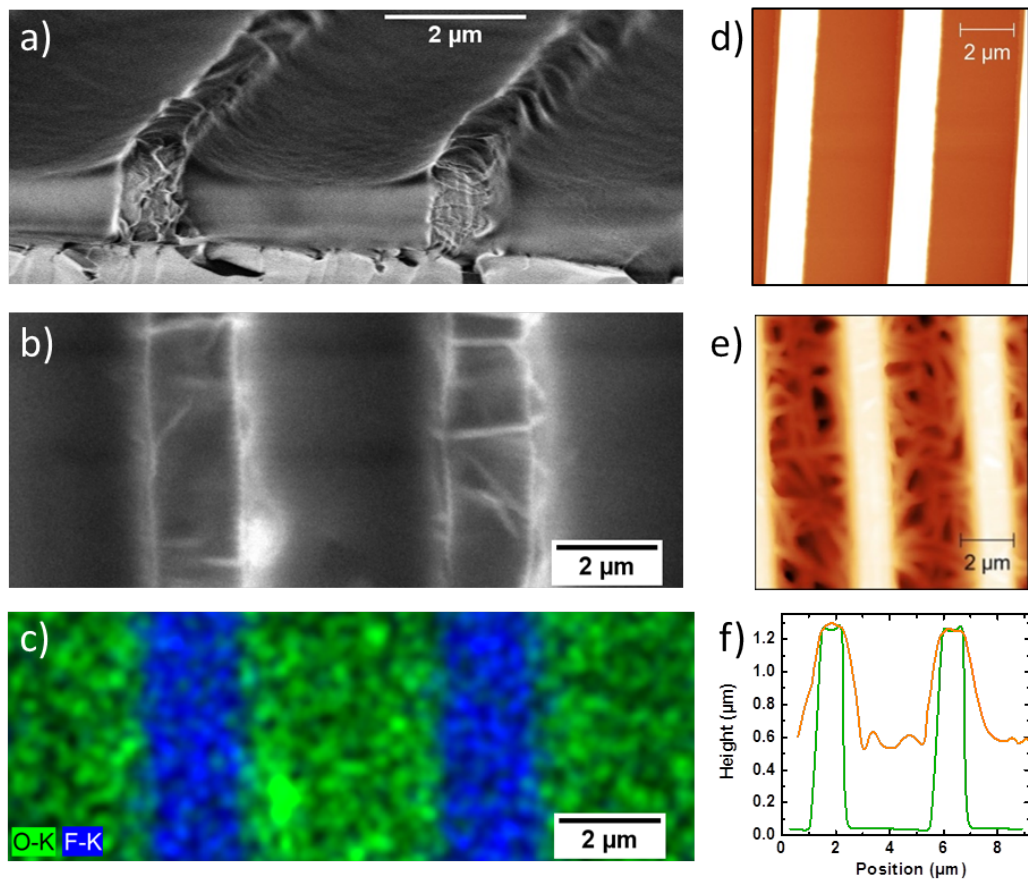
Figure 4.5: a) Cross-sectional and b) top-view SEM micrograph of bilinear array. c) Corresponding element map obtained by energy-dispersive X-ray spectroscopy. The distribution of F and O atoms is presented in blue and green, respectively. d) AFM micrograph of PVA line grating obtained by solution micromolding (color-coded range of the height scale is 100 nm). e) AFM micrograph after backfilling with P(VDF-TrFE) (height scale of 1.2 µm). f) Characteristic profile lines from AFM before (green) and after backfilling (orange). The orange line was shifted to account for profilometer measurements. [183]

The AFM micrographs of the PVA grating and the binary array after backfilling are shown in Figures 4.5d and e, respectively. The P(VDF-TrFE) lines show large crystals, similar as in Figure 4.4a. Typical line profiles are presented in Figure 4.5f. The inverted array also exhibits a non-planar topography. The height of the backfilled P(VDF-TrFE) is lower than that of the micromolded PVA; the aspect ratio is again about 1:2. For all binary arrays the initial micromolded grating protrudes in the height profile. As shown in Figures 4.5a and f, the surface of the backfilled polymer is concave, because upon backfilling the second polymer also covers the sidewalls of the previously patterned grating.

4.4 Device physics of thin film capacitors

In order to electrically characterize the bilinear arrays the patterning procedure was carried out on glass substrates comprising Au electrode lines. After solution micromolding and backfilling, Au top electrode lines were thermally evaporated. The lines are perpendicular to the bottom electrode lines yielding a cross-bar array. The device area of a single capacitor amounted to 0.16 mm^2; the capacitors were electrically disconnected from each other to avoid parasitic effects. The electric displacement D of the capacitors as a function of the applied electric field E was measured using a Sawyer-Tower setup as explained in detail in Section 3.7. A typical D-E curve for a bilinear array, where P(VDF-TrFE) protrudes (because it was patterned first), is presented in Figure 4.6a (orange curve).
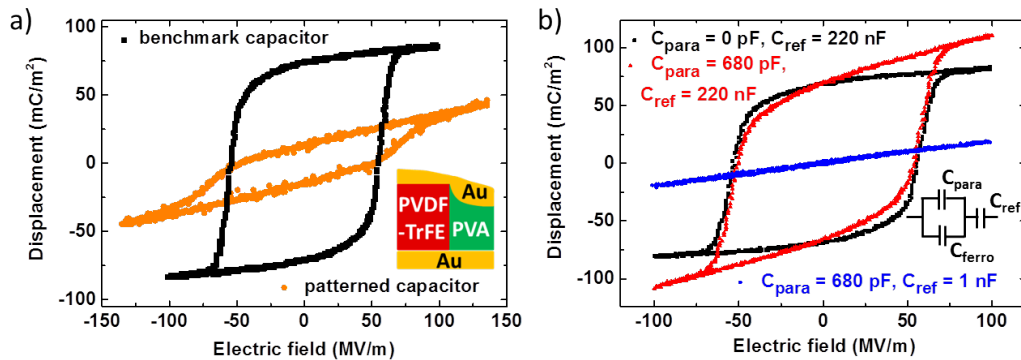
Figure 4.6: a) D-E hysteresis loops of a patterned capacitor and a benchmark thin film P(VDF-TrFE) capacitor. In the patterned capacitor a bilinear array of P(VDF-TrFE) and PVA is stacked between two electrodes. The ferroelectric copolymer protrudes, as illustrated in the inset. b) Hysteresis loops for electric circuits, where the benchmark capacitor was electrically connected in parallel with a non-ferroelectric linear capacitor and varying capacitors in series.

For comparison, the hysteresis loop of an unpatterned P(VDF-TrFE) film (black curve) is included, too. This benchmark capacitor exhibits a coercive field, E_c, of about 55 MV/m and a remanent polarization, P_r, of 72 mC/m^2 in good agreement with literature values [154].

The patterned capacitor also shows hysteresis with a very similar coercive field of about 54 MV/m confirming the ferroelectric response of P(VDF-TrFE). The remanent polarization of the patterned capacitor is about 15 mC/m^2 and thus lower compared to the benchmark. This is not surprising, since the displacement is calculated using the entire capacitor area. Taking into account that only 32.5% of the area is ferroelectric, the actual remanent polarization of P(VDF-TrFE) in the array is about 46 mC/m^2. This is still significantly below the benchmark value.

In order to exclude depolarization as the origin of the lower value of P_r, two tests were carried out. Firstly, the inner loops of the patterned capacitor were measured and compared to the saturated loop, as presented in the Appendix. The shape of the inner loops is very similar to the shape of the saturated loop implying that depolarization does not play a role. Secondly, bilayer capacitors were fabricated, where a thin film of PVA was introduced between P(VDF-TrFE) and the top electrode. The resulting bilayer capacitors did not suffer from depolarization (cf. Appendix), but showed the same value of P_r as the benchmark capacitor.

Obviously, even a thin film of PVA on top of the P(VDF-TrFE) lines would not explain the lower P_r value determined for the patterned capacitor. It is stressed again that different tools such as SEM, AFM combined with profilometry, as well as EDX were used to analyze the topography of the bilinear arrays. They all suggested that an overlayer of PVA on top of P(VDF-TrFE) can be avoided completely. Since these tools test the topography only locally, the study of the bilayer capacitors was additionally carried out to confirm that depolarization effects can probably be excluded.

The equivalent electrical circuit for the patterned capacitor is a linear capacitor of PVA in parallel with a ferroelectric P(VDF-TrFE) capacitor. In order to elucidate the origin of the lower remanent polarization in Figure 4.6a, the benchmark capacitor was connected in parallel with a non-ferroelectric (commercial) capacitor and the system of two parallel capacitors was introduced into a Sawyer-Tower setup. The circuit is schematically illustrated as inset of Figure 4.6b. The benchmark capacitor is abbreviated as C_{ferro} and the capacitor in series is abbreviated as C_{ref} (cf. scheme in Figure 3.5a).

The parallel capacitor C_{para} and the reference capacitor in series C_{ref} were systematically varied and hysteresis loops were measured for all combinations. Figure 4.6b shows the benchmark hysteresis loop (black curve, C_{para} is zero) together with two examples of the circuit. If the capacitance of the

parallel capacitor (680 pF) is higher than that of the benchmark ($C_{ferro} = 270$ pF) and, simultaneously, C_{ref} is orders of magnitude higher (220 nF), then the hysteresis loop exhibits the same values for P_r and E_c as the benchmark ferroelectric capacitor, but the slope at zero bias is higher (red curve).

However, if C_{ref} is only slightly larger than C_{para}, then the measured D-E curve is a straight line and does not show hysteresis at all (blue curve). The problem is intrinsic to the Sawyer-Tower setup, which relies on the charge measurement from the linear reference capacitor C_{ref}. A voltage, V, is applied over the electrical circuit and the voltage drop over the reference capacitor, V_{ref}, is measured. Knowing C_{ref}, the density of surface charges, Q_{ref}, at the reference capacitor can be calculated as

$$Q_{ref} = C_{ref} \cdot V_{ref}. \tag{4.2}$$

If C_{ref} is sufficiently large, then the voltage drop over this series capacitor is small and the ferroelectric capacitor is fully polarized. Moreover, since the two capacitors are in series, Q_{ref} at zero bias is equivalent to the remanent polarization of the ferroelectric capacitor, P_r. The ferroelectric polarization is normally determined this way.

However, if C_{ref} is comparable to C_{ferro}, then the ferroelectric properties cannot be properly determined [209]. Considering the equivalent circuit illustrated in Figure 4.6b, electroneutrality requires that

$$Q_{ref} = Q_{para} + P_r + C_{ferro} \cdot V_{ferro}. \tag{4.3}$$

Since the voltage drop at the ferroelectric and the parallel capacitor is equal,

$$Q_{para} = C_{para} \cdot V_{ferro}. \tag{4.4}$$

The applied voltage V is the sum of the voltages of the different elements,

$$V = V_{ref} + V_{ferro}. \tag{4.5}$$

Combining Equations 4.2 - 4.5 at $V = 0$ leads to

$$Q_{ref} = \frac{C_{ref} \cdot P_r}{C_{ref} + C_{ferro} + C_{para}}. \tag{4.6}$$

Equation 4.6 reveals that the measured Q_{ref} only corresponds to P_r, if the capacitance values of the ferroelectric and the parallel capacitor are significantly lower than C_{ref}, as it is the case for the red curve in Figure 4.6b. On the other hand, P_r vanishes in the measurement, if $C_{para} + C_{ferro} \approx C_{ref}$ (blue curve).

For the study of the equivalent circuit model, both, C_{para} and C_{ref} were systematically varied and hysteresis measurements were performed for each case. The extracted values of Q_{ref} at zero bias normalized with respect to P_r = 70 mC/m² are plotted versus the ratio of C_{para} and C_{ferro} in Figure 4.7a (symbols). The fully drawn lines are calculated according to Equation 4.6 and a good agreement between experiment and theory is obtained.

As long as C_{para}/C_{ferro} is small, Q_{ref} is indeed equivalent to P_r. Above a certain threshold value, Q_{ref} drops gradually to zero. The threshold value of C_{para}/C_{ferro} increases for higher values of C_{ref}. Hence, Figure 4.7a demonstrates that, depending on the device layout and value of C_{ref}, the apparent polarization, as measured with a Sawyer-Tower circuit, can significantly deviate from the actual remanent polarization. If the polarization of the ferroelectric is not fully compensated due to suppression of charges inside the circuit [209], then $Q_r < P_r$.

This can be avoided completely by performing shunt measurements, where the reference capacitor in the Sawyer-Tower setup is replaced by a resistor and the switching current is calculated from the voltage drop over the shunt resistance. The scheme of the circuit is shown as inset of Figure 4.7b. Detailed explanations were also given in Section 3.7. The hysteresis loop can be obtained by integrating the measured switching current. The green stars in Figure 4.7a represent the extracted values for Q_r from the shunt measurements. Artefacts of the conventional Sawyer-Tower configuration are eliminated, as the remanent polarization is constant and no longer depends on the ratio of C_{para}/C_{ferro}.
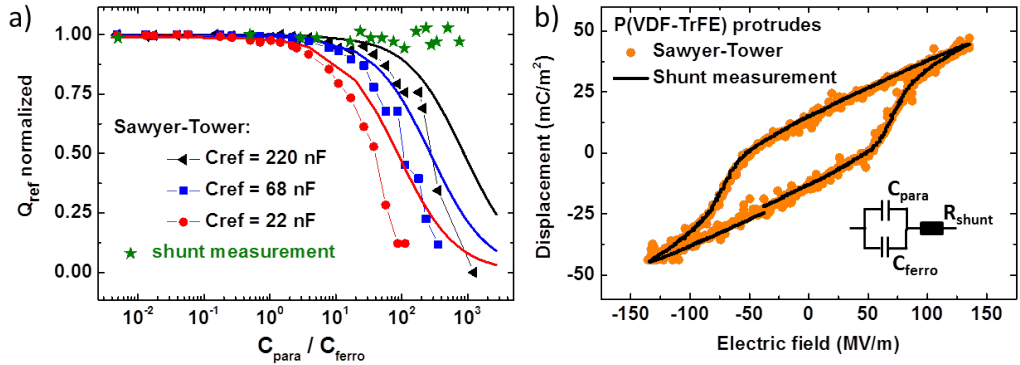
Figure 4.7: a) Normalized surface charge density of a ferroelectric capacitor, which is in parallel with a linear non-ferroelectric capacitor, as a function of the capacitance ratios [183]. The experimentally extracted values are shown as symbols and the theoretical calculations are presented as straight lines. The resistance of the reference resistor in the shunt measurement (green stars) amounted to 1 kOhm. b) Hysteresis loops of the patterned capacitor from shunt and Sawyer-Tower measurements. The inset schematically illustrates the circuit for shunt measurements, where C_{para} was systematically varied.

Figure 4.7b shows the hysteresis loops of the patterned capacitor obtained by shunt measurements and the Sawyer-Tower setup. Both curves lie on top of each other, which proves that the lower remanent polarization is not due to a measurement artefact.

In order to explain the experimentally observed lower P_r for the patterned capacitor, where P(VDF-TrFE) protrudes, the electric field distribution was calculated using a numerical device simulator. A two-dimensional (2D) grid was used, which accounts for the topography of the bilinear array, as shown in Figure 4.8a. The dielectric constants of PVA and P(VDF-TrFE) are here taken as 3 and 14, respectively. The potential on the electrodes is fixed. The electric field is then calculated using Poisson's equation. For simplicity, the ferroelectric dipoles in the P(VDF-TrFE) layer are neglected. Hence, the simulated field distribution is realistic only at low electric fields (below E_c). Figure 4.8a shows the calculated color-coded electric field distribution as well as the field lines (black). The electric field over the P(VDF-TrFE) lines is inhomogeneous due to the topography. It is high in the center and low at the edges. The large region of reduced electric field in the P(VDF-TrFE) at the interface with the PVA slab can be interpreted as a reduction in the effective device area. This might explain the measured lower remanent polarization.

The problem can be solved by using the inverted bilinear array. The inset of Figure 4.8b illustrates the corresponding capacitor layout, where PVA protrudes, because it was patterned first. The measured *D-E* hysteresis loop of the corresponding capacitor is shown as blue curve in Figure 4.8b. The original curve was multiplied by a factor of 4/2.7 to account only for the ferroelectric area. This leads to a small overestimation of the slope, but it allows
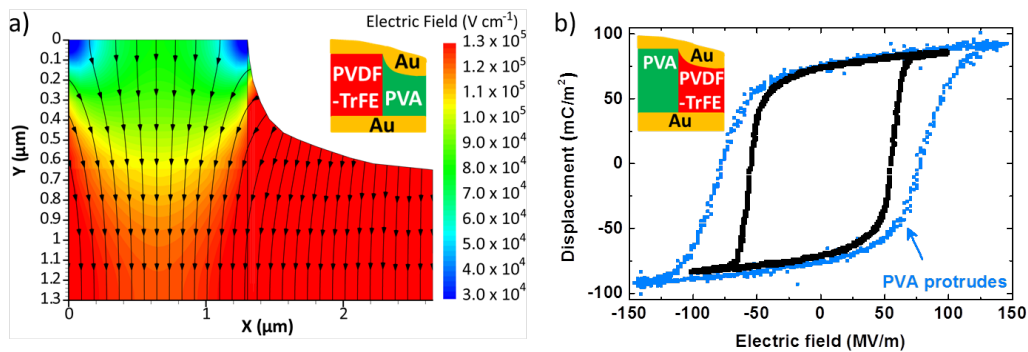
Figure 4.8: a) Electric field distribution in the bilinear array. The bottom and top contact are at a fixed potential. The electric field is color-coded and field lines are shown as black arrows. The inset illustrates the device layout: the left slab is P(VDF-TrFE) ($\epsilon = 14$) and the right slab is PVA ($\epsilon = 3$). b) *D-E* hysteresis loop of a patterned ferroelectric capacitor, where PVA protrudes in the bilinear array. The inset shows the device layout and the curve of the benchmark capacitor (black curve) is included for comparison [183].

better comparison with the benchmark capacitor (black curve). The values of P_r of the patterned and the benchmark capacitor are equivalent. The coercive field is higher for the patterned capacitor, probably because the electric field was calculated considering the minimum thickness of P(VDF-TrFE) in the concave profile. Using the inverted array, a capacitor comprising micropatterned P(VDF-TrFE) with excellent ferroelectric characteristics could be obtained.

4.5   Summary of Chapter 4

In this chapter, line gratings of the ferroelectric polymer P(VDF-TrFE) were obtained by solution micromolding using a microstructured elastomeric PDMS stamp. In order to fabricate capacitors the gratings were backfilled with the electrically insulating polymer PVA, which was chosen because it dissolves in deionized water, a solvent that is orthogonal to P(VDF-TrFE). Inverted arrays by micromolding PVA and backfilling with P(VDF-TrFE) were fabricated as well.

Capacitors were finished in cross-bar geometry and electrically analyzed in detail. The equivalent electrical circuit is a linear capacitor of PVA in parallel with the ferroelectric capacitor of P(VDF-TrFE). The consequences for conventional Sawyer-Tower measurements were analyzed and experimentally verified. The determined polarization can significantly deviate from the expected remanent polarization. This can be avoided completely in shunt measurements, where a reference resistor is used instead of a reference capacitor. The hysteresis loops of the bilinear arrays extracted from the switching current always yield the actual remanent polarization.

The arrays exhibit topography as the height of the backfilled polymer is always lower than that of the initially micromolded grating. In capacitors made from binary arrays, where P(VDF-TrFE) protrudes, the remanent polarization is reduced. Numerical simulations of the electric field distribution suggest that the origin is a decrease in the effective electrode area. On the other hand, in binary arrays, where PVA protrudes, the ferroelectric hysteresis loops are similar to those of unpatterned, benchmark capacitors. This implies that solution micromolding is a versatile technology to study confinement by scaling down the lateral dimensions of the grating. The latter will be a subject of the next chapter.

Chapter 5

Nanostructured organic ferroelectric memory diodes

Organic ferroelectric memory diodes consist of a blend thin film of P(VDF-TrFE) and a semiconducting polymer sandwiched between two electrodes. Typically, the thin film is obtained by spin coating or wirebar-coating the blend solution. After deposition the two polymers phase-separate due to their pronounced incompatibility [49]. This leads to a film morphology, where single domains of the semiconductor with a broad size distribution are randomly distributed in the matrix of the ferroelectric polymer.

The random distribution is undesired for various reasons: Firstly, the interface between two polymers is decisive for the memory effect and thus the device performance. In a random network, the interfaces can hardly be controlled/tuned. Secondly, if the concept of a single diode is transferred to a cross-bar memory array, which is the ultimate goal, the random phase separated blend exhibits a strong On-state current variation for the single diodes, particularly upon increasing the integration density [35].

In this chapter, solution micromolding is utilized to obtain bilinear arrays of P(VDF-TrFE) and the semiconducting polymer poly(9,9-dioctylfluorene) (PFO). This allows fabrication of memory diodes with well-defined interfaces between the two functional polymers in the active layer. Electrical characterization of the diodes, including data retention analysis, is carried out in detail. Moreover, the lateral dimension of the bilinear arrays, the pitch width, is scaled down systematically and the comprising memory diodes are compared. The results discussed in this chapter have been published in *Advanced Functional Materials* [210].

5.1 Solution micromolding for memory diodes

In a first approach to obtain a patterned memory diode, a P(VDF-TrFE) line grating was prepared on a glass substrate comprising Ag electrodes, followed by simply spin coating a PFO solution on top. The stamp used for solution micromolding shows a pitch width and depth of 2 µm and 500 nm, respectively. The period width is 4 µm. Figure 5.1a shows an AFM micrograph of the P(VDF-TrFE) grating (upper picture) obtained with a solution concentration of 6 wt%. The corresponding height profile is shown in Figure 5.1b. The copolymer lines are about 1.5 µm broad and 120 nm high. It should be noted that the height is deliberately lower than in the previous chapter, because thinner films allow operation at lower voltages and thus lower power consumption.

The AFM micrograph after spin coating PFO (20 mg/ml in toluene) is shown in Figure 5.1a, too (lower picture). The surface is not flat but exhibits a profile with alternating hills and valleys as shown in Figure 5.1b (blue profile line). The height difference between the top and the bottom of the profile is about 80 nm, less than the height of the original grating. The film thickness was measured before and after spin coating PFO and shows an increase of about 80 nm, in agreement with the AFM measurement. The blue profile line in Figure 5.1b was shifted accordingly. Apparently, PFO does not only fill the free space of the P(VDF-TrFE) grating, but also covers the top. It should be noted that different spin coating processes with varying solution concentrations and spin parameters were tested, which all led to a topography with protruding lines, where the P(VDF-TrFE) grating was covered with PFO. Diode fabrication was finished by thermal evaporation of Ag top contacts yielding a device area of a single diode of 0.16 mm^2.
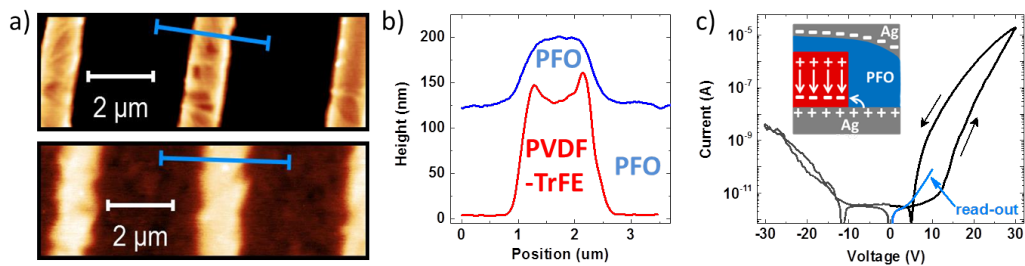
Figure 5.1: a) AFM micrographs of P(VDF-TrFE) before and after spin coating PFO solution on top. b) Characteristic profile lines extracted from the AFM micrographs. The blue line was shifted according to profilometer measurements, which provided thickness values of 135±9 nm before and 210±11 nm after spin coating PFO. c) Current-voltage (*I-V*) characteristics of the resulting memory diode with Ag bottom and top contacts. The inset illustrates the device layout. The bias was applied at the bottom contact. The top contact was grounded. The black arrows indicate the sequence of measurements.

The resulting device layout accounting for the PFO overlayer is schematically illustrated as inset of Figure 5.1c. Current-voltage (*I-V*) characteristics of the diode are presented in Figure 5.1c. For low negative bias the current is very small (below 10 pA) and increases only slightly for higher voltages. The nominal injection barrier, *i.e.* the difference between the work function of Ag (4.3 eV [38]) and the HOMO level of PFO, 5.8 eV [211], is about 1.5 eV. The Ag-PFO Schottky contact is strongly injection limited explaining the low current measured for negative bias. The situation is completely different at positive bias. The current is also very low for low bias, but starting at about 12 V, it increases by more than seven orders of magnitude. Sweeping back from 30 V to 0 V, the current stays high and is about three orders of magnitude higher at 10 V as compared to the forward sweep.

The strong non-linearity for positive bias and the high asymmetry between positive and negative bias can be explained by the device layout. At the bottom contact the interface of P(VDF-TrFE) and PFO is in contact with Ag. If the applied bias exceeds the coercive voltage, here about 10 V, P(VDF-TrFE) polarizes. The ferroelectric polarization charges are compensated by counter charges in the electrode leading to a stray electric field as illustrated by the white bent arrow in the inset of Figure 5.1c. Due to the stray field a significant amount of charges is injected from the electrode into the semiconductor despite the high injection barrier [41]. As a consequence, a high current is observed. Further details on the stray electric field and its strong impact on the device physics will be discussed in the next chapter.

Upon sweeping back, the current stays high, because sweeping back does not change the polarization of the ferroelectric. However, if the current is measured a second time at positive bias (light blue curve), it is an order of magnitude lower and it decreases further over time. The high current state is not retained, because the ferroelectric polymer depolarizes. The origin lies in the PFO overlayer, which cannot provide sufficient negative compensating charges. Hence, the ferroelectric polarization cannot be fully compensated resulting in a significant depolarization field. These findings are in agreement with a literature report, where a semiconducting layer was deliberately deposited on top of a working phase separated blend to get a model system for depolarization [36]. In that study, the retention was still good as long as the semiconducting layer thickness was below 10 nm. According to Figure 5.1c, the PFO overayer exhibits a thickness of about 80 nm and thus, the diode suffers from depolarization and poor retention performance.

A stable high current state cannot be obtained, because the Ag top electrode does not have a direct contact with P(VDF-TrFE). This is also the reason for the high asymmetry of the *I-V* curve. At the top contact there is

no stray electric field, which could yield a high charge injection, as it is the case for the bottom electrode at positive bias. Therefore, the current stays comparably low for negative bias due to the high injection energy barrier. Note that the problem of a semiconducting overlayer on top of P(VDF-TrFE) has previously also been observed in literature, where patterning approaches for organic ferroelecric memory diodes were investigated [53, 55].

In this chapter, it will be demonstrated that this issue can be solved by inverting the process sequence: first, a PFO line grating is prepared by solution micromolding. Then P(VDF-TrFE) is backfilled using the hot-press and a flat unstructured stamp. Hence, the technology developed in Chapter 4 is now used for the memory diodes. The inverted process is explained in detailed in the following section.

5.2   Bilinear arrays without overlayer

Non-polar solvents such as toluene, which are typically used to dissolve PFO, are expected to be not compatible with soft lithography and thus solution micromolding, because these solvents swell the elastomeric PDMS stamp [203]. Therefore, the solubility of PFO and PDMS was analyzed in numerous solvents. The underlying physics, namely the Hansen theory, and the details of the experiments as well as the results are presented in the Appendix.

In short, the solubility of a polymer can be described by δ_D, δ_P, and δ_H which are the dispersive, the polar and the hydrogen bonding Hansen solubility parameters, respectively. These three parameters form the axes of the three dimensional Hansen space. The position of each solvent in the Hansen space is fixed by its three components. For a polymer, the three components determine the center of a Hansen solubility sphere. In a simple approach, the radius of the solubility sphere is defined such that good solvents of the polymer lie inside the sphere and bad solvents or non-solvents outside.

The experimental study revealed that the solubility spheres of PFO and PDMS in the 3D Hansen space almost completely overlap (for details see Appendix). This means that there is no orthogonal solvent for PFO and PDMS, and swelling of the stamp during solution micromolding cannot be avoided by choice of solvent. However, the problem can still be solved by adjusting the process itself: the integrity of micromolded PFO line gratings can be maintained, if the elastomeric stamp is mechanically fixed to a rigid support before the beginning of the process. As a rigid support a stack of glass slides and unstructured pieces of PDMS was used. This stack fixes the PDMS stamp and strongly suppresses the swelling. Moreover, it equalizes the applied pressure in the hot-press upon solution micromolding.

PFO line gratings were fabricated over areas of 2x2 cm^2. A typical AFM topography image is shown in Figure 5.2a. Homogeneous lines with a height of about 300 nm are obtained with hardly any debris in between. The fill factor is 60 % presumably due to the low concentration of PFO in the solution (5 mg/ml in toluene). Higher concentrations also led to continuous lines, which were, however, very inhomogeneous in thickness.

For backfilling, a drop of P(VDF-TrFE) dissolved in DMSO (120 mg/ml) is put onto the PFO line grating followed by hot-pressing with a flat un-structured PDMS stamp (140 °C, 2 h). The AFM topography image of the resulting bilinear array is presented in Figure 5.2b. The morphology shows the characteristic needles of P(VDF-TrFE), which were also observed for micomolded gratings of the copolymer [183]. The topography profiles before and after backfilling as derived from AFM measurements are shown in Figure 5.2c. The backfilling ratio is about 85%. Using concentrations of P(VDF-TrFE) even higher than 120 mg/ml led to overfilling, which is un-desired. An overlayer of the ferroelectric copolymer would limit the current density of the diode significantly, because P(VDF-TrFE) is an insulator.

In the bilinear array the PFO lines protrude with respect to the backfilled P(VDF-TrFE) copolymer. Importantly, the two polymer lines are clearly sep-arated, as illustrated by the obvious differences in morphology in Figure 5.2b. The latter is confirmed by SEM micrographs obtained in cross section and top view, which are shown in Figure 5.3a and the inset of Figure 5.3c, re-spectively. It is emphasized that no overlayers are formed. The protruding lines of PFO and the neighboring domains of P(VDF-TrFE) are separated by a well-defined interface. To finish diode fabrication, PEDOT:PSS serving as top contact was spin coated onto the array, followed by thermal evaporation of Au lines through a shadow mask. The Au lines act as self-aligned mask for the removal of PEDOT:PSS by reactive ion etching.
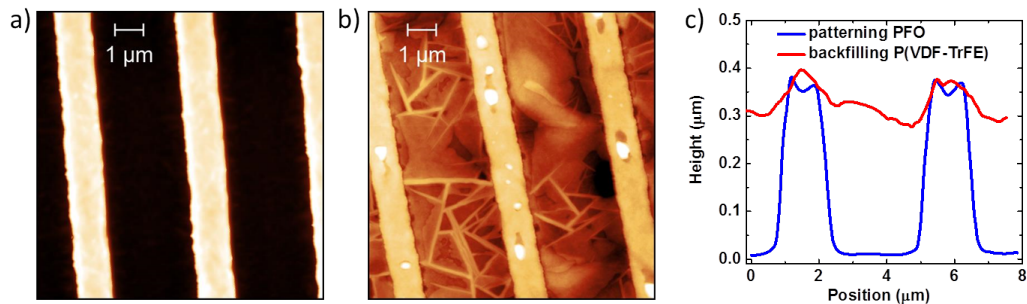
Figure 5.2: AFM topography images of a) the PFO line grating (height scale of 400 nm) and b) the bilinear array after backfilling (height scale of 200 nm). c) Line profiles before and after backfilling as extracted from AFM measurements. The red line was shifted according to the film thickness as measured with a surface profilometer. [210]

5.3   Characterization of patterned diodes

In the resulting crossbar array each cross point corresponds to a single memory diode with a device area of 0.16 mm^2. The device layout is illustrated in Figure 5.3a accounting for the topography. It should be noted that the characterization of entire memory arrays is outside the scope of this work. To that end, the single diodes were always electrically disconnected from each other before the start of the measurements to exclude cross-talk. Both Au and PEDOT:PSS form an injection limited contact with PFO. The injection barrier is estimated to be between 0.8 eV (PEDOT:PSS) and 1.3 eV (Au) [38, 211, 212]. Only the hole transport of PFO has to be considered, because the injection barriers for electrons are even higher than that for holes.
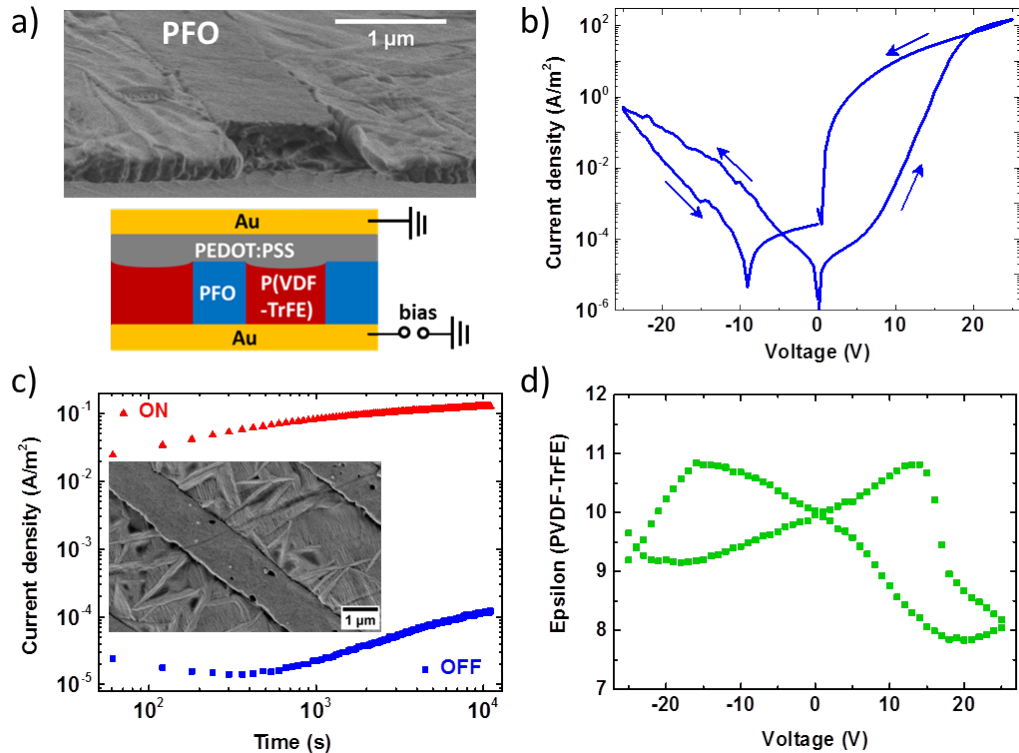
Figure 5.3: a) Top picture: SEM cross section of bilinear array of PFO and P(VDF-TrFE). Bottom picture: Schematic device layout. The bilinear array is sandwiched between Au and PEDOT:PSS electrodes. b) Current density-voltage characteristics for the comprising memory diode. The blue arrows indicate the sequence of the measurement. c) Data retention obtained by programming the diode to either the high current density On-state or the low current density Off-state and monitoring the current over time at a bias of +2.5 V. The inset shows the top view SEM micrograph of the bilinear array. The two functional polymers are clearly separated from each other. d) Dielectric constant of P(VDF-TrFE) extracted from impedance measurements as a function of applied bias. The ferroelectric copolymer switches for both bias polarities. [210]

Futhermore, electron transport is typically strongly trapped in PFO and hole transport is dominant [213]. In all measurements, bias was applied to the bottom contact. Typical current density-voltage (J-V) characteristics are shown in Figure 5.3b. Starting at 0 V, the bottom electrode is swept to +25 V. At low bias the current density is low, as the bottom contact is injection limited. The diode is in the Off-state. However, by increasing the positive bias, the ferroelectric P(VDF-TrFE) gets fully polarized. The resulting stray electric field between the polarization charges and the image charges in the electrode enables efficient charge injection: according to literature reports [41, 45], charge transport becomes bulk-limited. The current density increases by orders of magnitude and the diode is in the On-state. The ferroelectric polarization does not change upon sweeping back to 0 V. Hence, the diode remains in the high current density On-state. Note that the device physics will be analyzed in more detail in Chapter 6.

Data retention - a key parameter for memories - is evaluated by programming the diode once to the On- or Off-state and then monitoring the current over time at +2.5 V. Figure 5.3c shows that the retention is guaranteed for over 10^4 s and the On/Off current modulation is always larger than 10^3. This performance is excellent for organic ferroelectric memory diodes, especially considering the low read-out voltage [52, 214].

Next, the bottom electrode is swept from 0 V to -25 V and PEDOT:PSS is the hole injecting contact. A similar (or even smaller) injection barrier is anticipated. Hence, the J-V characteristics for negative bias are expected to be a mirror image of the curve for positive voltages. However, rather surprisingly, the current density is low even for high voltages and the diode remains in the Off-state. This means that the fabricated devices are not only bistable but also rectifying diodes.

In order to verify that the ferroelectric polymer switches for both bias polarities, the dielectric constant of the memory diode was extracted from impedance measurements. The impedance analysis provides the capacitance of the diode. The dielectric constant of P(VDF-TrFE) was then calculated taking into account that P(VDF-TrFE) makes up only about 65% of the device area. Figure 5.3d shows the dielectric constant as a function of applied bias. A characteristic butterfly shape is obtained [215]. The hysteresis stems from the ferroelectric polarization switching, *i.e.* dipole rotation in the presence of an electric field [32]. Since the polarization of the ferroelectric P(VDF-TrFE) switches regardless of the bias polarity, the low current density of the memory diode for negative bias is not due to lack of polarization switching. The reason for the rectifying behavior, which is actually desired for memory diodes, will be explained in Chapter 6.

5.4   Downscaling the bilinear arrays

As mentioned before, the interface of PFO and P(VDF-TrFE) is expected to be decisive for the operational mechanism of memory diodes. Therefore, the pitch width of the PFO grating was scaled down from 2 μm to 500 nm. The period was fixed at twice the pitch width and the corresponding profiles of the master/stamp are presented in Figure 5.4a. For a pitch width below 1 μm, PDMS cannot be used anymore, because the elastomer does not accurately replicate the features of the master due the high viscosity of the precursors. Instead, composite or so-called h-PDMS stamps can be prepared [187, 188]. The details of the preparation are given in Section 3.3.
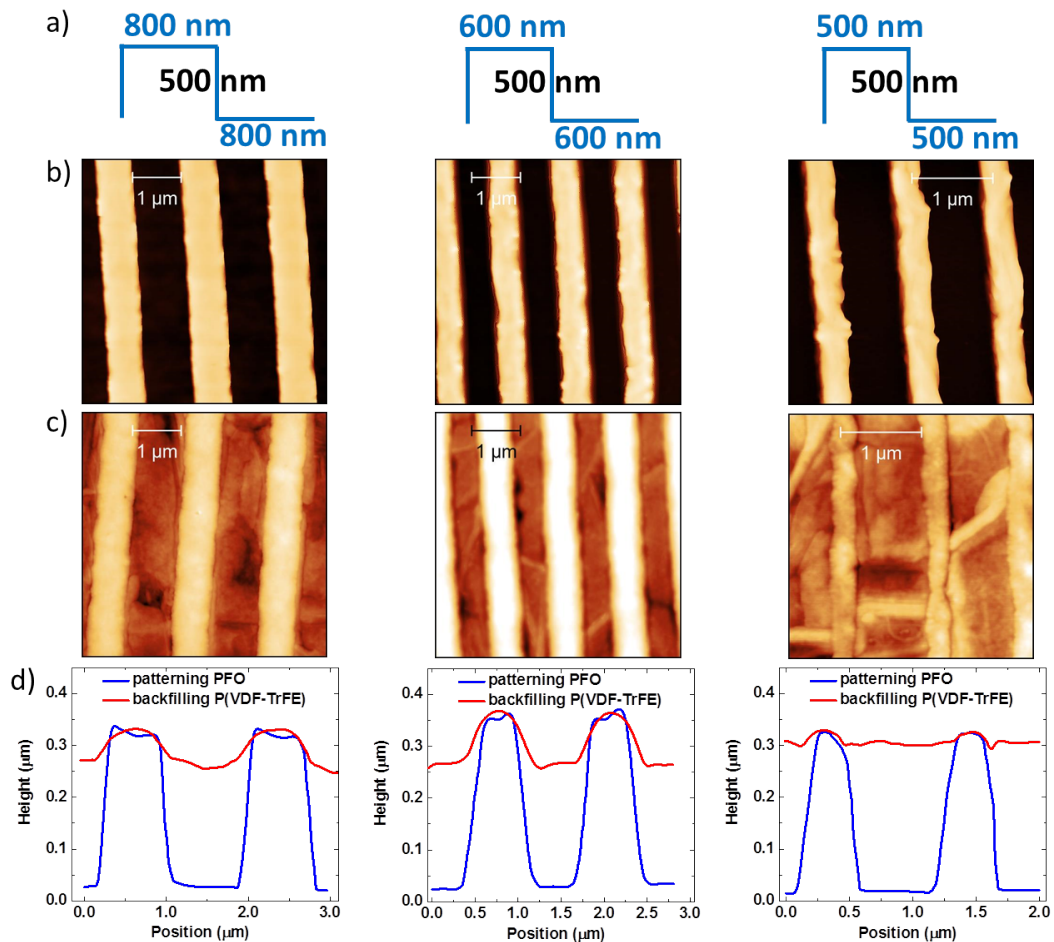
Figure 5.4: a) Schematic profiles of the silicon master and the corresponding replicated h-PDMS based stamps. b) AFM topography images of PFO line gratings obtained for pitch width of 800 nm, 600 nm, and 500 nm [210]. c) AFM topography images of bilinear arrays after backfilling with P(VDF-TrFE). d) Characteristic height profile lines as extracted from the AFM images. The red lines were shifted according to the film thickness measurements.

Figure 5.4b shows AFM micrographs of PFO line gratings obtained by solution micromolding using h-PDMS stamps with 800 nm, 600 nm and 500 nm pitch width. Even for the 500 nm grating, homogeneous lines are obtained. The height in all cases is about 300 nm yielding a fill factor of about 60%. Again, 5 mg/ml was the optimized concentration for the solution of PFO in toluene. For all feature sizes the replicated line width is smaller than the nominal pitch width probably due to the swelling of the stamp.

The PFO gratings were again backfilled with P(VDF-TrFE) using concentrations of 100-120 mg/ml (DMSO). The AFM topography images of the resulting bilinear arrays are shown in Figure 5.4c, and typical line profiles before and after backfilling are presented in Figure 5.4d. The backfilling ratio is between 80 and 95 % for all feature sizes. No overlayer of P(VDF-TrFE) is formed; in all bilinear arrays the PFO lines protrude with respect to the backfilled P(VDF-TrFE) copolymer. For feature sizes smaller than 1 μm, the results are very similar to the reference with a pitch width of 2 μm.

Memory diodes were fabricated using Au bottom and PEDOT:PSS top contacts. In all cases *J-V* characteristics comparable to Figure 5.3b were obtained, as shown in the Appendix. The diodes show bistability in the current density when the bottom Au electrode is the hole-injecting contact. In contrast, when PEDOT:PSS is the injecting contact the current density is typically lower and almost no hysteresis is observed. Figure 5.5a shows the measured On-state current density as a function of bias for diodes with pitch width ranging from 2 μm down to 500 nm. The current density increases with decreasing pitch width. In order to better compare the diodes, Figure 5.5b shows the current density extracted at +15 V as a function of reciprocal feature size. Each plotted value is the average of 8 diodes.
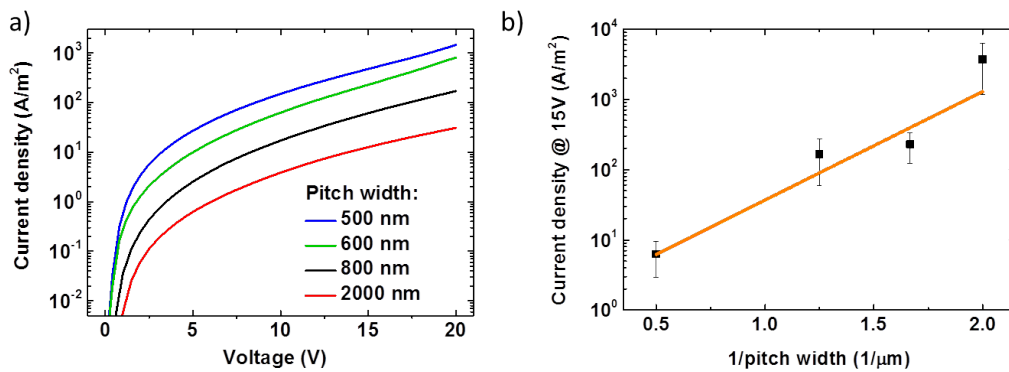
Figure 5.5: a) On-state current density of patterned memory diodes with varying pitch width as a function of the applied bias. b) On-state current density of the diodes extracted at +15 V as a function of reciprocal pitch width. The error bars present standard deviations over at least 8 diodes for each feature size. The orange line is the least squares approximation. [210]

In Figure 5.6a, the measured current densities are presented as a function of the effective interface length per unit area together with data extracted from literature [35, 45]. For the patterned memory diodes the effective interface length is the number of PFO-P(VDF-TrFE) interfaces times the length of the interfaces per unit area. For the reported memory diodes based on phase separated blends, the effective interface length is calculated by multiplying the number of semiconducting domains per unit area with the average domain circumference. The number of domains and the domain diameters were tabulated in references [45] and [35].

A large scatter in absolute values and in the functional dependence is obtained for the data reported in literature (Figure 5.6a). By contrast, the patterned diodes show a clear trend. The current density increases exponentially with increasing interface length or with decreasing pitch width as shown in Figure 5.5b. This dependence is counterintuitive. The memory diode is an interface device, where the current is injected at the interface between the ferroelectric and the semiconducting polymer [41]. Consequently, the current density is expected to increase linearly with increasing interface length (Figure 5.6a). Furthermore, it should increase linearly with the reciprocal pitch width of the bilinear arrays and not exponentially as in Figure 5.5b. The superlinear increase upon downscaling might be due to the processing. In a recent study, the organic semiconductor poly(3-hexylthiophene) (P3HT)
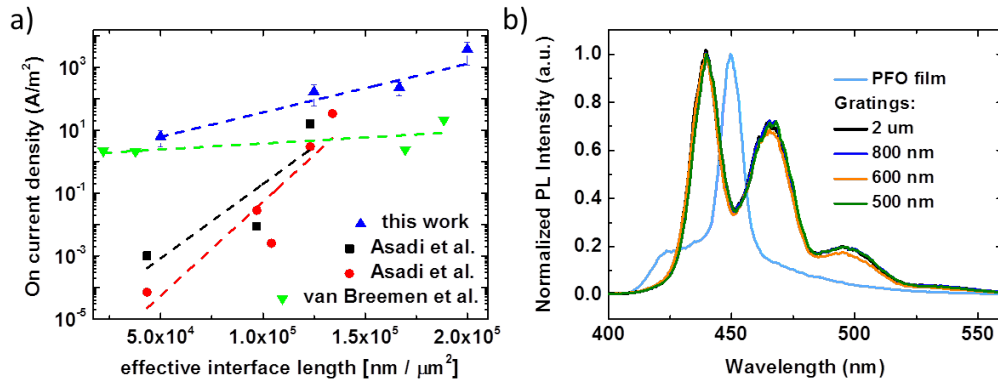
Figure 5.6: a) On-state current density of organic ferroelectric memory diodes as a function of effective interface length [210]. Comparison of the results of this work with data reported in literature. The literature data were extracted from the publications of Asadi et al. [45] and van Breemen et al. [35]. For the patterned memory diodes the effective interface length is the number of PFO-P(VDF-TrFE) interfaces times the length of the interfaces per unit area. For the memory diodes based on phase separated blends the number of semiconducting domains was multiplied by the average domain circumference. These values based on morphology analysis were tabulated in the references [35, 45]. b) Normalized photoluminescence (PL) intensity of PFO gratings with different pitch width and of a PFO reference thin film obtained by spin coating.

was structured by nano-imprint lithography (NIL) [216] yielding single circular micropatterns of P3HT. The out-of-plane mobility was increased by four orders of magnitude with respect to a smooth film. At the edge of each micropattern, the mobility was even higher compared to the center of the pillar. The enhanced mobility was related to vertical polymer chain alignment as a result of the shear forces applied in the processing.

Unlike in NIL shear forces do not play a role in solution micromolding, where pattern formation relies on capillary forces. Therefore, the processing related charge transport enhancement observed in reference [216] probably cannot explain the On-state current density increase upon downscaling in micromolded memory diodes. However, the possibility of enhanced chain alignment of PFO using solution micromolding should be considered.

A different approach to 'confine' a semiconducting polymer during processing is template wetting [217], where a solution or melt of a polymer is placed on a porous substrate with high surface energy. In order to decrease the overall energy, the polymer spreads and covers the walls of the porous structure, for instance anodized aluminum oxide [218]. Applying this technique to the semiconducting polymer poly[2-methoxy-5-(2-ethylhexyloxy)-1,4-phenylenevinylene] (MEH-PPV), Cannon and co-workers observed a significant mobility increase for the resulting nanotubes with respect to a reference thin film of MEH-PPV [219]. More importantly, the mobility increased by orders of magnitude if the nanotube diameter was scaled down from 200 nm to 100 nm.

Conductivity-enhancement upon downscaling the tube diameter was also reported for template-wetting based polypyrrole [220]. For both, MEH-PPV and polypyrrole, the improved charge carrier transport was related to enhanced ordering of the polymer chains. As explained in Section 2.3, intermolecular charge transport, *i.e.* charge transfer between different chains, is the main factor limiting the conductivity in polymer semiconductors [22]. If the molecular order is enhanced and the polymer chains are aligned during processing, as it is the case for template-wetting [220], then the overall mobility/conductivity can rise significantly [221, 222].

The question now arises, whether solution micromolding also yields an improved chain alignment of PFO and whether the effect would be enhanced upon downscaling the pitch width. The driving force for template wetting and solution micromolding is the same, the polymer (solution) spreads and covers the walls (of the porous structure or of PDMS) to decrease the total surface energy. Therefore, a similar chain ordering mechanism could be expected for solution micromolding. Moreover, PFO is known to have different conformations in thin films depending on the processing. For instance, the β-phase shows a coplanar conformation and facilitates π-π-stacking [223, 224].

Charge transport in PFO strongly depends on the phases and hence on the processing [225]. For phase identification, PFO gratings with different pitch width were investigated by photoluminescence (PL) using a laser excitation wavelength of 400 nm. Figure 5.6b shows the normalized PL spectra of a PFO reference thin film and of the micromolded PFO gratings. The spectra for the gratings with different pitch width are identical, but they differ significantly from the PL spectrum of the PFO film obtained from spin coating. The latter shows a strong peak around 450 nm and a much weaker broad peak around 426 nm. Both peaks are typical for a spin coated PFO thin film [192, 226]. It is worth mentioning that the UV-VIS absorption spectrum of the reference thin film (data not shown) shows a broad absorption maximum around 380 nm, which is again typical for an amorphous PFO film [227]. This glassy phase of PFO in the reference thin film is confirmed by X-ray scattering analysis presented in Figure 5.7, which does not show any crystalline contribution but only an amorphous phase [228]. More details on this structural analysis will be given in the next section.

The PL spectra of the gratings show two pronounced peaks at 439 nm and 466 nm and one broader and smaller peak around 498 nm. These three peaks are clearly indicative of the β-phase [193, 228]. The similarity of the PL spectra for varying feature sizes suggests that there is no effect on the phase formation upon downscaling the pitch width. In order to double-check this question, the PFO line gratings were also analyzed with X-ray scattering.

5.5   X-ray scattering analysis of PFO gratings

The signal of X-ray scattering from thin films of polymer semiconductors is typically weak because of disorder and the small number of scattering planes in a thin film [229]. Moreover, the form factors of lightweight elements is low. Therefore, high flux X-ray sources, such as Synchrotron sources, are often used to obtain reasonable scattering intensities [230].

Grazing incidence wide-angle X-ray scattering (GIWAXS) is the only scattering geometry that gives details about crystalline packing in thin films of semiconducting polymers [231]. In GIWAXS, the molecular packing is examined in both out-of-plane and in-plane direction with respect to surface [231]. Scattering is expressed as a function of the scattering angle, 2θ, or the scattering vector q, which is $q = 4\pi \sin(\theta)/\lambda$, with λ being the wavelength of the incident radiation. Following Bragg's law, the spacing between two planes, d, is then $d = 2\pi/q$. The detector is 2-dimensional (2D). For the coordinate system of the scattering vector, $q_{x,y}$ is the component along the surface.

The corresponding horizontal axis on the detector represents the equatorial plane (in-plane organization). Besides, q_z is the component normal to the surface and the corresponding vertical axis on the detector relates to the so-called meridional plane (out-of-plane organization) [232]. Any structural organization that is not purely out-of-plane or in-plane will show components of both $q_{x,y}$ and q_z. The shape, intensity and position of the diffraction peaks can be used to determine the orientation of the molecules in the investigated thin layer.

Figures 5.7a and b show the GIWAXS 2D image plates obtained for the PFO reference thin film and the PFO line grating with a pitch of 600 nm, respectively. The reference film shows a broad isotropic halo ring suggesting that PFO is completely amorphous in the spin-cast film. This is in agreement with the results from PL spectroscopy. The PFO line grating with 600 nm pitch width shows amorphous response as well, but additionally, a thin reflection ring corresponding to a d-spacing of 1.28 nm occurs. A very similar value for the d-spacing was also reported for PFO thin films containing the β-phase [193]. This appears to confirm that the micromolded PFO grating contains the β-phase. Note however that the reflection in Figure 5.7 b is still rather weak.

Figure 5.7c shows the integrated intensities as a function of the scattering vector for the reference film and the different gratings. Gratings with pitch width of 600 nm and 500 nm both show a peak related to a d-spacing of about 1.28 nm. By contrast, the reference thin film and the grating with pitch width of 800 nm lack any diffraction peaks and appear completely amorphous. This is surprising, because the PL spectroscopy suggested that all gratings contain the β-phase. These seemingly contradictory findings can possibly be explained as follows. All gratings show β-phase response in the PL spectroscopy, because a certain ordering occurs upon solution micromolding compared to the spin coated reference thin film.
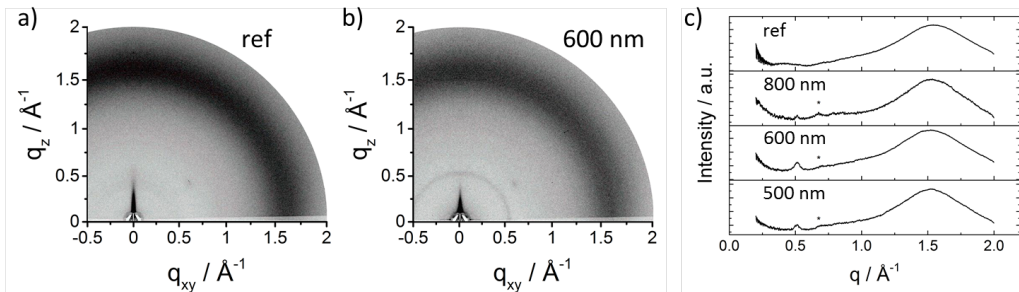
Figure 5.7: 2D detector image plates of the GIWAXS measurements of a) the reference thin film and b) the PFO grating with a pitch width of 600 nm. c) Integrated intensity as a function of the scattering vector q for the reference film and different gratings.

However, the ordering is very limited. Hence, structural investigation by GIWAXS provides only amorphous response for the grating with 800 nm pitch width just like for the reference film. Gratings with 500 or 600 nm pitch width exhibit a broad amorphous halo in GIWAXS, too. But the presence of crystalline reflections in the spectra indicates a better ordering with respect to the pattern with 800 nm pitch width.

In conclusion, gratings are better ordered than the thin film, because they contain β-phase according to PL spectroscopy. Upon downscaling the pitch width, the ordering further improves, since only gratings with 600 nm and 500 nm pitch width show a crystalline response in GIWAXS, which is however still significantly less pronounced than the response of a well-ordered β-phase thin film. The trend for the structural analysis upon downscaling gives a hint, why the On-state current density in memory diodes shows a superlinear increase as a function of the inverse pitch width. The enhanced order for lower pitch width might result in better charge transport and thus higher currents. Nevertheless, a more thorough and combined characterization of devices and gratings is needed to better understand the effect of downscaling.

5.6   Summary of Chapter 5

Ferroelectric memory diodes were fabricated from bilinear arrays of the organic semiconductor poly(9,9-dioctylfluorene) (PFO) and the ferroelectric polymer P(VDF-TrFE). First, PFO gratings with a pitch width of 2 μm were fabricated using solution micromolding. The gratings were backfilled with P(VDF-TrFE) by hot-pressing with a flat unstructured PDMS stamp yielding a bilinear array without overlayer. Arrays were sandwiched between Au bottom and PEDOT:PSS top contacts and the comprising memory diodes showed bistable electrical transport with current modulation over three decades that was retained for more than 10^4 s. Interestingly, the patterned diodes were not only bistable but also rectifying.

The feature size, *i.e.* the pitch width of the bilinear array, was varied from 2 μm down to 500 nm and memory diodes were fabricated also for the downscaled arrays. The observed superlinear increase of On-state current density as a function of reciprocal feature size is very promising. It might be due to confinement, meaning that the microstructure of micromolded PFO gets more ordered upon downscaling. A potentially resulting decrease in the width of the density of states in the valence-like band could lead to an increase of mobility upon downscaling. However, the performed structural analysis did not provide a clear conclusion on this topic.

Chapter 6

Device physics of organic ferroelectric memory diodes

Despite their technological success the physics of organic ferroelectric memory diodes is not yet fully understood. It is well-known that the ferroelectric polarization of P(VDF-TrFE) modulates the charge injection over the metal-semiconductor Schottky barrier, but the exact mechanism is not clear. Previously, it was proposed based on numerical simulations that the polarization charges in P(VDF-TrFE) and the resulting compensating image charges in the electrode provide a stray electric field, which lowers the injection barrier and facilitates thermionic emission [41]. In these simulations, the ferroelectric polarization was artificially taken into account by fixed charges located at 1.5 nm distance from the electrode [41, 42]. Hence, the calculated current modulation could only be rationalized as a function of the injection barrier. Complete current-voltage (I-V) curves could not be modeled, because the field-dependence of the ferroelectric polarization was completely disregarded. Moreover, a constant mobility was used for the semiconductor without considering the charge carrier density dependence.

In this chapter, two-dimensional (2D) numerical simulations will be performed, which deliberately take into account the 2D polarization of P(VDF-TrFE), the charge transport in the organic semiconductor and the charge injection at the metal-semiconductor interface. As a consequence, entire I-V characteristics of organic ferroelectric memory diodes can be quantitatively described for the first time. More importantly, the simulations give detailed insight into the device physics.

The calculations were carried out using a numerical device simulator, which is briefly introduced in the next section. The key results of this chapter have been published in *Nature Communications* [233].

79

6.1   Numerical simulations

The numerical device simulator allows to model multidimensional devices and circuits. By implementing the parameters of the different materials and the detailed device geometry, a thorough quantitative description of the device physics based on numerical calculations is possible.

In this context, a real device, *e.g.* a transistor, is transferred into a virtual device and the physical properties are discretized onto a grid (also called mesh) of nodes, where the grid can be regular, but also non-uniform. As a consequence, properties that are continuous in the real semiconductor, such as a charge carrier concentration profile, are defined only on the grid points. The space in between can be obtained by interpolation. Metals (electrodes) are defined as fixed voltage boundary condition in the device simulator.

Typically, the device geometry is described first, followed by the definition of the mesh and the interconnection between the single grid points. Then, the parameters for the single components of the device are defined. In a field-effect transistor for instance, the gate material and the semiconducting channel exhibit different properties, which are considered in this step.

Subsequently, the physical equations are established. In the case of the organic ferroelectric memory diode, the coupled drift-diffusion, continuity and Poisson equation have to be solved by the numerical simulator on the grid. In the simulator, these partial differential equations are converted into finite difference equations and self-consistently solved in an iterative way, *i.e.* an error is calculated for each iteration and the simulation keeps running until the error is below a certain value, which means that convergence is achieved.

The simulation usually starts by only solving the Poisson equation for an applied bias in equilibrium (zero current) and considering the pre-defined charge carrier distribution as starting point. Then, in the next step, the continuity and drift-diffusion equations are included and the three equations are solved together making use of the solutions for the Poisson equation obtained in the first step.

It should be noted that the grid has to be very dense in regions, where physical effects occur on a very small scale. Hence, in order to save calculation time, the grid is adapted with respect to the typical length scale of the physical effect. After the solution converges for a certain voltage, the procedure is repeated for a slightly higher bias. Based on that, entire *I-V* characteristics can be quantitatively described. For each bias step, the solution of the previous step is taken as initial guess.

6.2   Model of 2D ferroelectric polarization

Various components are required for the numerical simulations including an electric field-dependent polarization model for P(VDF-TrFE), a model describing the charge transport physics of the semiconducting PFO, and a model for charge injection at the Au-PFO Schottky contact. These components will be introduced one-by-one in the following.

In the past, different models have been proposed to quantitatively describe ferroelectric D-E hysteresis loops [234–243]. The Preisach model, for instance, was originally derived for magnetic materials [244] and then adapted to ferroelectrics [234, 235]. It suggests that a ferroelectric material consists of so-called hysterons [236]. These hysteretic units show a bidimensional distribution of coercive fields, which can be described by a Preisach function [234, 236]. Integrating the distribution function can finally lead to the equation for the hysteresis loop [235].

Other models [242] were based on dipole switching and thus go back to the so-called Kolmogorov-Avrami-Ishibashi (KAI) model [175–177] for nucleation and growth of domains upon polarization reversal. The change of polarization as a function of time, $\Delta P(t)$, under an applied electric field, E, can be expressed as [179]

$$\frac{1}{2 \cdot P_r} \Delta P(t) = 1 - \exp\left(-\left(\frac{t}{t_0}\right)^n\right). \tag{6.1}$$

Here, the polarization is normalized with respect to $2P_r$. This normalized value is equal to one for complete polarization reversal. n is the Avrami index and it depends on the dimensionality of the domains. According to the empirical Merz law [180], the switching time, t_0, is related to the activation field, E_{act}, and reads

$$t_0 = t_\infty \exp\left(\frac{E_{act}}{E}\right), \tag{6.2}$$

where t_∞ is the switching time at infinite applied field.

In electric circuits with several components and in devices with complicated geometry such as FETs, a dipole switching model can be inappropriate, particularly if non-ideal conditions shall be taken into account. To that end, Miller and co-workers [237] introduced an empirical model for the D-E relation, which requires only four physical material parameters to quantitatively describe a ferroelectric hysteresis loop: P_r, E_c, the dielectric constant, ϵ_{FE}, and the saturation polarization, P_{sat}, which describes the polarization at maximum electric field. As shown in Section 2.5, the electric displacement,

$\vec{D}$, is the sum of the linear dielectric response and the spontaneous ferroelectric polarization due to dipole switching, $\vec{P}_s$:

$$\vec{D} = \epsilon_0\vec{E} + \epsilon_0\chi_{FE}\vec{E} + \vec{P}_s = \epsilon_0\epsilon_{FE}\vec{E} + \vec{P}_s. \tag{6.3}$$

Here, χ_{FE} is the linear susceptibility of the ferroelectric polymer. Following Miller's approach, the ferroelectric response is then expressed using a *tanh* functional:

$$P_s(E) = P_{sat} \cdot \tanh\left(\frac{E - E_c}{\iota}\right), \tag{6.4}$$

where ι depends on the ferroelectric material parameters and reads

$$\iota = 2 \cdot E_c \cdot \left(\ln\left(\frac{1 + \frac{P_r}{P_{sat}}}{1 - \frac{P_r}{P_{sat}}}\right)\right)^{-1}. \tag{6.5}$$

The *hyperbolic tangent* was chosen, because it is mathematically convenient and it is consistent with experimental data [237]. Equations 6.4 and 6.5 were successfully implemented to model semiconductor devices comprising inorganic ferroelectrics [238–241, 243]. Later, the model was also utilized to quantitatively describe device physics of capacitors and FETs based on P(VDF-TrFE) [157, 245].

Figure 6.1a shows the measured *D-E* hysteresis loop of the benchmark P(VDF-TrFE) capacitor (black symbols) together with the calculated curve based on Equations 6.3 - 6.5 (red line). A very good agreement between the model and the experiment is obtained, if $\epsilon_{FE} = 14$, $P_r = 72.5$ mC/m^2,
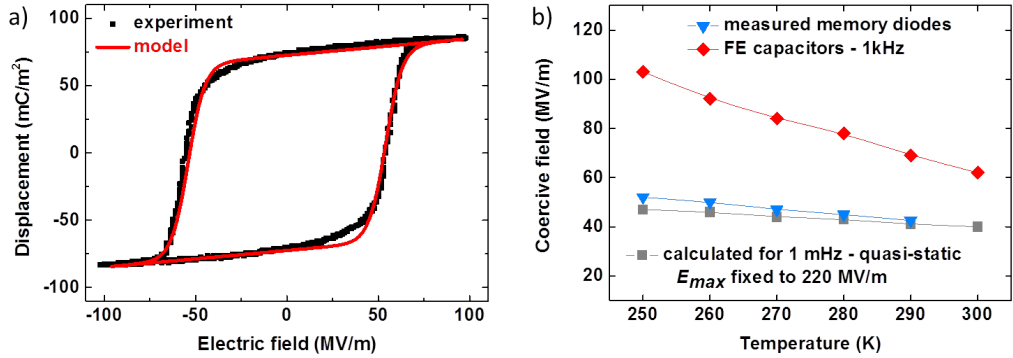
Figure 6.1: a) Experimental *D-E* hysteresis loop and calculated curve (red line) using the model of Miller et al. [157, 237]. Here, the following parameters were used for the modeling: $\epsilon_{FE} = \chi_{FE}+1 = 14$, $P_r = 72.5$ mC/m^2, $P_{sat} = 72.501$ mC/m^2, $E_c = 54$ MV/m. b) Coercive field extracted from a ferroelectric capacitor and from analyzed memory diodes as a function of temperature [233]. Additionally, the calculated coercive field at 1 mHz is shown. The calculations were performed based on the ferroelectric switching model presented in reference [179]. The maximum electric field was $E_{max} = 220$ MV/m.

$E_c = 54$ MV/m. These are typical values as reported in literature [154]. The saturated polarization is only slightly higher than P_r. The reason is that the *P-E* loop of P(VDF-TrFE) is almost rectangular; back-switching of dipoles upon removing the electric field plays only a minor role. Therefore, the slope of the *D-E* curve at zero bias is dominated by the linear response of P(VDF-TrFE).

The model of Miller has been implemented into the device simulator in a computationally efficient way [241]. Even unsaturated hysteresis loops can be modeled [243]. It is therefore ideal for the modeling of organic ferroelectric memory diodes, if one crucial aspect is taken into account: The ferroelectric capacitor (Figure 6.1a) was measured at a frequency of 1 kHz, which is typical for a Sawyer-Tower setup. By contrast, the *I-V* curve of an organic ferroelectric memory diode is measured quasi-statically.

Figure 6.1b shows the coercive field as a function of temperature extracted from *D-E* measurements of a capacitor at 1 kHz. Moreover, the coercive field values determined from memory diode measurements, which can be considered as quasi-static, are included, too. As expected, the values of E_c are much higher if measured at 1 kHz. For both frequencies, E_c decreases with increasing temperature as polarization reversal is thermally activated.

In order to obtain the quasi-static values of E_c from the capacitor measurement at 1 kHz, hysteresis loops can be iteratively calculated from polarization switching transients, if Equation 6.1 is adapted [179], which leads to

$$P(t + \Delta t) = P(t) + (P_s - P(t)) \cdot \left(1 - exp\left(\frac{t}{t_0}\right)^n\right). \qquad (6.6)$$

Assuming a triangular wave form for the electric field as a function of time, the numerical calculation of polarization as a function of time can be converted into a *P-E* relation. From the reconstructed hysteresis loops at a frequency of 1 mHz, the quasi-static coercive field is extracted and plotted as a function of temperature in Figure 6.1b (grey squares). The obtained values are in very good agreement with E_c extracted from memory diodes (details on the memory diodes will be provided later). This suggests that the numerically extracted values of E_c at 1 mHz can be used as parameters for P(VDF-TrFE), when modeling the organic ferroelectric memory diodes.

It is worth mentioning that the considerations on dipole switching, used for the determination of E_c, allow to include the physics of polarization reversal into the originally solely empirical *D-E* model of Miller and co-workers.

6.3   Modeling semiconductor charge transport

Besides the 2D ferroelectric polarization, the charge transport in PFO is a very important component for the memory diode model. In order to determine the hole transport parameters of the PFO batch used here, hole-only diodes were fabricated with PEDOT:PSS bottom and MoO_x top contacts. The device layout is shown in Figure 6.2b. The PFO film thickness and the device area amounted to 210 nm and 8 mm^2, respectively. MoO_x was chosen because it forms an Ohmic contact with PFO [213] due to its work function of about 6.8 eV [246]. As a consequence, the bulk-limited charge transport in a hole-only diode and thus the PFO transport physics can be analyzed, while effects of the metal-semiconductor contact can be excluded.

The measured I-V characteristics of the hole-only diode at temperatures ranging between 235 K and 295 K are presented in Figure 6.2a (symbols). The current for negative bias is not considered here, because PEDOT:PSS forms a Schottky contact with PFO. For positive bias (MoO_x is hole-injecting) the current increases for increasing voltage and for higher temperatures due to thermal activation. The charge transport model used to quantitatively describe the I-V curves (lines in Figure 6.2a) will be elaborated in the following. As described in Section 2.3, polymer semiconductors are typically disordered. This also applies to PFO; the spin-cast thin film analyzed with XRD in Section 5.5 did not show any crystalline response.
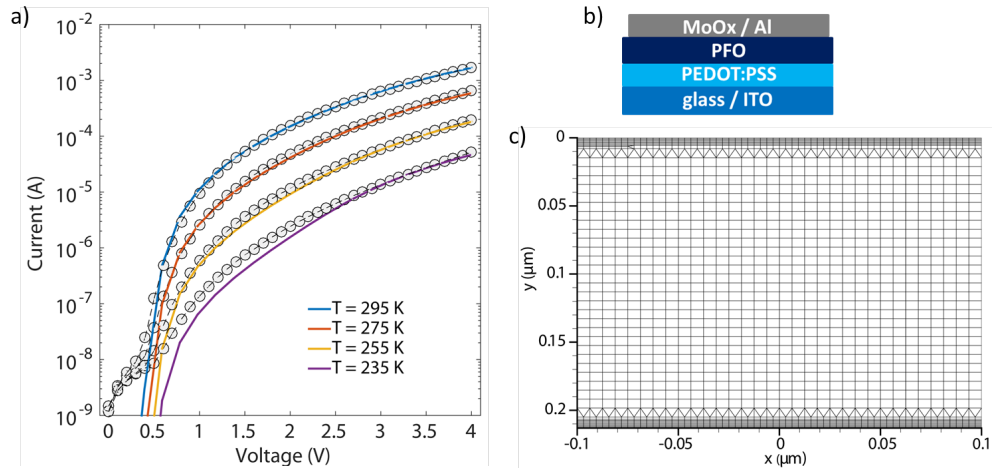
Figure 6.2: a) Measured (symbols) and calculated (lines) I-V characteristics of the hole-only diode for temperatures ranging between 235 K and 295 K [233]. Only positive bias (MoO_x is hole-injecting) is considered here, because MoO_x is known to form an Ohmic contact with PFO [213]). b) Schematic device layout of the hole-only diode. c) 2D grid used for the numerical simulation of the hole-only diode. The electrodes (anode and cathode) are shown as thin lines, they do not require discretization. The grid is more dense close to the metal-semiconductor contacts to guarantee convergence of the simulation.

Disordered semiconductors are characterized by localized states. The energetic distribution of states (DOS), $g(\xi)$, can be described by a Gaussian function centered at the HOMO (or LUMO) level, which reads [85, 87, 247]

$$g(\xi) = \frac{N_t}{\sqrt{2\pi}\sigma} \exp\left(-\frac{(\xi - \xi_{HOMO})^2}{2\sigma^2}\right). \tag{6.7}$$

Here, N_t is the total number of states and σ is the energetic width of the DOS, which is higher for more disordered systems. ξ_{HOMO} is the energy level of the HOMO (for more details, cf. Section 2.3).

Charge transport occurs via thermally activated hopping [80, 248]. The conductance, G_{ij}, between two sites depends on the occupation and can be expressed as

$$G_{ij} = f_i(\xi_i, \xi_F)\left(1 - f_j(\xi_j, \xi_F)\right) \cdot \nu_{ij}, \tag{6.8}$$

where ξ_F is the Fermi energy. The site with index i is called 'donor', while the 'acceptor' is indexed by j. Thus, ξ_i and ξ_j are the energy levels of the donor and acceptor sites, respectively; $f_i(\xi_i, \xi_F)$ is the occupation probability of the donor. Only if the donor is occupied and the acceptor j is unoccupied, hopping from i to j is possible. In equilibrium the occupation probability of the localized states follows Fermi-Dirac statistics:

$$f(\xi, \xi_F) = \frac{1}{1 + \exp\left(\frac{\xi - \xi_F}{k_B T}\right)}, \tag{6.9}$$

where k_B is the Boltzmann constant and T is the absolute temperature. In Equation 6.8 the hopping rate between the donor and acceptor, ν_{ij}, can be described by the Miller-Abrahams model [81]:

$$\nu_{ij} = \nu_0 \exp\left(-2\alpha r_{ij}\right) \cdot \exp\left(-\frac{\xi_j - \xi_i}{k_B T} \cdot \theta\left(\xi_j - \xi_i\right)\right), \tag{6.10}$$

where ν_0 is the attempt-to-escape frequency, r_{ij} is the distance between donor and acceptor, and α is the inverse localization radius. Typically, $\alpha \approx 10/a$ with a being the inter-site distance in a semiconducting polymer (between 1 and 2 nm) [85]. The Heaviside function $\theta\left(\xi_j - \xi_i\right)$ makes sure that the argument of the second exponential becomes 0, if $\xi_i > \xi_j$.

Equation 6.10 reveals that thermally activated tunneling between two localized states depends on the energy of and the distance between the states. Combining Equations 6.8 - 6.10, the conductance between two sites can be rewritten as

$$G_{ij} = G_0 \exp\left(s_{ij}\right), \tag{6.11}$$

where $G_0 = q^2\nu_0/k_B T$ [86, 249, 250] (with q being the elementary charge) and s_{ij} reads [83, 84]

$$s_{ij} = 2\alpha r_{ij} + \frac{|\xi_j - \xi_i| + |\xi_j - \xi_F| + |\xi_i - \xi_F|}{2k_B T}. \tag{6.12}$$

Combining the microscopic conductance of each couple of sites in the disordered semiconductor, the macroscopic conductivity of the semiconductor can be determined using percolation theory [83, 84]. Therefore, in the model of Vissenberg and Matters [82], the critical percolation conductance between two sites, G_c, is described by $G_c \propto \exp{(-s_c)}$, where s_c is the critical percolation exponent. Any donor-acceptor couple with $G_{ij} < G_c$ cannot contribute to the macroscopic charge transport. In order to obtain the macroscopic conductivity, Γ, which is

$$\Gamma = \Gamma_{00} \exp{(-s_c)}, \tag{6.13}$$

the value for s_c has to be determined (Γ_{00} is proportional to G_0 [86]). Therefore, the onset of percolation can be calculated as follows:

$$B(G = G_c) = B_c = \frac{N_b(\xi_F, s_c)}{N_s(\xi_F, s_c)}. \tag{6.14}$$

In this percolation problem, N_b is the density of bonds, N_s is the density of sites, and $B_c = 2.8$ for an amorphous system [251]. The density of bonds is obtained by integrating in energy the product of all available donor and acceptor sites over the distance r_{ij}:

$$N_b = 4\pi \int_{\mathbb{R}^3} r_{ij}^2 g(\xi_i) g(\xi_j) \theta\left(s_c - s_{ij}\right) d\xi_j d\xi_i dr_{ij}. \tag{6.15}$$

Note that only sites, which satisfy the percolation criterion, are included. The same holds for the expression of the density of sites, which reads

$$N_s = \int_{\mathbb{R}} g(\xi) \theta\left(s_c \cdot k_B T - |\xi - \xi_F|\right) d\xi. \tag{6.16}$$

By numerically solving Equation 6.14, using the Gaussian DOS $g(\xi)$, the macroscopic conductivity Γ as a function of the Fermi energy level can be calculated. The exact numerical solution can be approximated by [252]

$$\Gamma = \Gamma_0 \exp\left(\frac{\xi_F}{k_B T}\right), \tag{6.17}$$

where Γ_0 depends on T, σ, ν_0, α, and the inter-site distance $a = N_t^{-1/3}$ (cf. Equation 30 in reference [86]). Γ is a functional for the conductivity

comparable to the mobility functional described by Equations 2.14 - 2.17. Using Γ the current density in the hole-only diode in Figure 6.2a as a function of the applied bias can be calculated by numerically solving the coupled drift-diffusion, continuity, and Poisson equation. The drift-diffusion equation reads

$$\vec{J}_p = \Gamma \nabla \varphi + q \cdot D_p \nabla p, \tag{6.18}$$

where $\vec{J}_p$ is the hole current density, φ is the electric potential and D_p is the diffusion constant. The latter can be linked to the mobility, μ, and thus to Γ by the Einstein relation [253, 254]: $D_p = \mu_p k_B T$. p is the hole density. Only hole transport (index p) is considered here for simplicity. The equations for electrons follow analogously. The continuity equation is described by

$$\frac{dp}{dt} = -\frac{1}{q} \nabla \cdot \vec{J}_p. \tag{6.19}$$

The Poisson equation relates to Gauss's law of electrodynamics and reads [77]

$$\epsilon_0 \epsilon_r \nabla \cdot \vec{E} = \rho, \tag{6.20}$$

where $\vec{E}$ is the electric field vector. The charge carrier concentration, ρ, is the sum of all positive and negative charges per volume: $\rho = q \cdot (p - n)$.

If the ferroelectric polymer is included into the modeling (for the memory diode), then the Poisson equation needs to be adapted, which leads to

$$\nabla \cdot \vec{D} = \rho, \tag{6.21}$$

where $\vec{D} = \epsilon_0 \epsilon_r \vec{E} + \vec{P}_s$. Obviously, Equation 6.20 still holds, where the grid is made up of the semiconductor ($|P_s| = 0$). The charge carrier density results from the Fermi-Dirac statistics and the DOS according to

$$p = \int_{-\infty}^{+\infty} g(\xi) f(\xi, \xi_F) d\xi. \tag{6.22}$$

In order to model the charge transport through PFO based on the mathematical framework described so far, the coupled differential Equations 6.18 - 6.20 are solved on a 2D grid, which is shown in Figure 6.2c. The two electrodes are presented as lines. Bias is applied at the bottom electrode (for the simulations, MoO_x is the bottom contact) and the top contact (PEDOT:PSS) is grounded.

The resulting calculated *I-V* curves are presented as a function of temperature in Figure 6.2a (lines). The following material parameters were used: inter-site distance $a = N_t^{-1/3} = 1.5$ nm, $\alpha = 10/a$, $\sigma = 0.16$ eV, $\epsilon_{PFO} = 3$,

$\nu_0 = 10^{13}$ s^{-1}, and $\Gamma_0 = 2$ x 10^{-5} S/cm. These are typical values for a disordered semiconductor like PFO [106]. An excellent agreement between the experiment and the model is obtained for all temperatures. Hence, the model can be used to describe the charge transport of PFO within the organic ferroelectric memory diodes.

6.4   Charge injection at a Schottky contact

The last component for the numerical simulations is charge injection at the Au-PFO Schottky contact. In Section 2.4, it was discussed that the two well-known charge injection mechanisms, thermionic emission and barrier tunneling were derived for band like semiconductors. As such, the Richardson-Schottky equation as well as the Fowler-Nordheim equation cannot be used in their original form to describe charge injection into a disordered organic semiconductor like PFO.

   Therefore, the charge injection concept for organic semiconductors proposed by van der Holst and co-workers [114] was discussed in Section 2.4, too. It considers charge injection as a hopping process from the electrode to a discrete state of the semiconductor (and *vice versa*) accounting for the actual effective energy barrier. This leads to a total injection-limited current density, J_{ILC}, which can be written (for hole-injection) as (cf. Equation 2.29 and Section 2.4)

$$J_{ILC} = qp_0\mu(p_0, E)E = qN_t \exp\left(-\frac{\Phi_B}{k_B T} + \frac{1}{2}\frac{\sigma^2}{(k_B T)^2}\right)\mu(0, E)E, \quad (6.23)$$

where $\mu(0, E)$ expresses the field-dependence of the mobility comparable to Equation 2.17. Interestingly, Equation 6.23 is similar to the description of drift-diffusion current density in a single carrier diode (hole-only or electron-only with Ohmic contacts) based on the mobility functional described in Equations 2.14 - 2.17. This is not surprising, as both models include hopping according to the Miller-Abrahams formalism.

   The key consequence of the Schottky energy barrier for the overall current density is that it limits the charge carrier density in the semiconductor directly at its interface with the electrode. This charge carrier density, p_0, is strongly related to the effective energy barrier, Φ_B, and it can be written as [86]

$$p_0 = N_t \exp\left(-\frac{\Phi_B}{k_B T} + \frac{\sigma^2}{2(k_B T)^2}\right). \quad (6.24)$$

As described in Section 2.4, the effective injection barrier is significantly lower than the the nominal barrier, Φ_{B0}, which is defined as $\Phi_{B0} = \xi_{HOMO} - \Phi_{Au}$

and equals 1.3 eV in the case of the Au-PFO contact [38]. Two effects decrease the nominal barrier: image force barrier lowering and the disorder of the polymer.

Taking into account the width of the DOS, σ, the initial barrier Φ_B^* for charge injection is smaller than the nominal barrier, because the hop from the metal to the semiconductor can be into an unoccupied state of the DOS [114, 119, 137]. It has been demonstrated that, if $T < T_0 = \sigma^2/k_B\Phi_B^*$, then the initial barrier can be approximated as $\Phi_B^* = \Phi_{B0} - \Delta\Phi_G$, where $\Delta\Phi_G$ is a constant [255]. The aforementioned inequality is satisfied for the measurements in this work, as $T_0 \approx 370$ K, which is significantly above the experimental conditions. The value of $\Delta\Phi_G$ can be extracted from Equation 6.24, which can be rewritten as

$$p_0 = \int\limits_{-\infty}^{+\infty} g(\xi)f(\xi, \xi_{HOMO} - \Phi_{B0})d\xi \approx N_t \exp\left(\frac{-1}{k_BT} \times \left[\Phi_{B0} - \frac{\sigma^2}{2k_BT}\right]\right).$$
(6.25)

Therefore, $\Delta\Phi_G = \sigma^2/(2k_BT) \approx 0.5$ eV ($\sigma = 0.16$ eV) and the initial Schottky barrier (at 295 K) is $\Phi_B^* = 0.8$ eV. Moreover, image force barrier lowering further decreases the energy barrier such that the effective Schottky barrier, Φ_B, is described by

$$\Phi_B = \Phi_B^* - \sqrt{\frac{q^3E}{4\pi\epsilon_0\epsilon_r}}.$$
(6.26)

Note that electron injection can be disregarded completely in the organic ferroelectric memory diodes considered here, because the injection barrier is almost 2 eV.

The numerical device simulator indeed includes the drift-diffusion model [256] and explicitly takes into account the charge carrier density at the interface as well as the effective barrier due to the disorder and image force barrier lowering. Moreover, the model also includes the other two well-known charge injection mechanisms, namely barrier tunneling and thermionic emissions.

These mechanisms might not have played an important role in the charge injection model of Schottky diodes [114]. However, the situation might be completely different in an organic ferroelectric memory diode, where the polarization of P(VDF-TrFE) is crucial. To that end, all potential charge injection mechanism are included in the device simulation, in order not to miss an important contribution to the operational mechanism.

Thermionic emission is expressed as

$$J_p = \frac{A^*T^2}{N_t}(p - p_0),$$
(6.27)

where A^* is the effective Richardson constant, $A^* = \frac{4\pi q m_p^* k_B^2}{h^3}$, m_p^* is the hole effective mass and h is Planck's constant (m_p^* is here taken equal to the free electron rest mass, $m_0 = 9.11 \times 10^{-31}$ kg). Most importantly, the hole density is included also in Equation 6.27.

Barrier tunneling describes the tunneling rate over the 2D energy barrier at the metal-semiconductor contact. The hole current density flowing from the metal to the semiconductor is expressed by [131]

$$
\begin{aligned}
J_{tun} = \frac{A^*T}{k_B} \int\limits_{-\infty}^{\infty} \kappa_p(r,\xi) \\
\times \left[\log\left(1 + \exp\left[\frac{\xi_F(r) - \xi}{k_B T}\right]\right) - \log\left(1 + \exp\left[\frac{\xi_F(0^-) - \xi}{k_B T}\right]\right) \right] \partial\xi,
\end{aligned}
\tag{6.28}
$$

Here, $\xi_F(r)$ is the position-dependent Fermi energy. r is the distance from the metal/semiconductor interface ($r = 0$ is at the interface and 0^- is at the interface but inside the metal electrode). κ_p is the tunneling probability based on the Wentzel-Kramers-Brillouin (WKB) approximation, which reads

$$
\kappa(r,\xi) = \exp\left(-\frac{4\pi}{h} \int\limits_0^r \sqrt{2m_p^* |\xi_{HOMO}(r) - \xi|} \theta\left(\xi_{HOMO}(r) - \xi\right) \partial r\right), \tag{6.29}
$$

where $\xi_{HOMO}(r)$ is the barrier potential energy in the HOMO level of the organic semiconductor. The Heaviside function, $\theta\left(\xi_{HOMO}(r) - \xi\right)$, makes sure that only barrier tunneling is considered in Equation 6.29. Compared to Equation 2.24 in Section 2.4, the energetic structure of the organic semiconductor is explicitly included in Equation 6.29.

It is worth noting that barrier tunneling was successfully implemented into a device physics model of an organic field-effect transistor [257, 258]. Considering that hopping is phonon-assisted tunneling, it is not surprising that barrier tunneling works as charge injection mechanism also for polymers.

So far, the details on the different components, namely charge transport of PFO, ferroelectric response of P(VDF-TrFE), and charge injection at the Au-PFO Schottky contact have been addressed. In the next section, these different aspects are brought together to model the patterned ferroelectric memory diode. The fabrication and characterization of this device was discussed in detail in Chapter 5.

6.5 Modeling the patterned memory diode

The bilinear array of the patterned memory diode exhibits topography; PFO protrudes with respect to the backfilled P(VDF-TrFE). This is illustrated in Figure 6.3a, which shows the geometry as extracted from AFM analysis. In order to realize an optimized device physics model, the 2D grid used for the numerical simulation follows this geometry in detail (the grid is presented in the Appendix). Due to the symmetry of the patterned diode, the entire bilinear array can be modeled using Figure 6.3a. The contributions from all the other repeating lines as well as the length of each line (third dimension perpendicular to the device layout) are simply included by a multiplication factor, which is called 'area factor' accounting for the whole device area. It is further pointed out that the P(VDF-TrFE) lines are only partly included, because P(VDF-TrFE) is insulating, and thus the calculation of the current can be made more efficient using a less broad P(VDF-TrFE) slab.
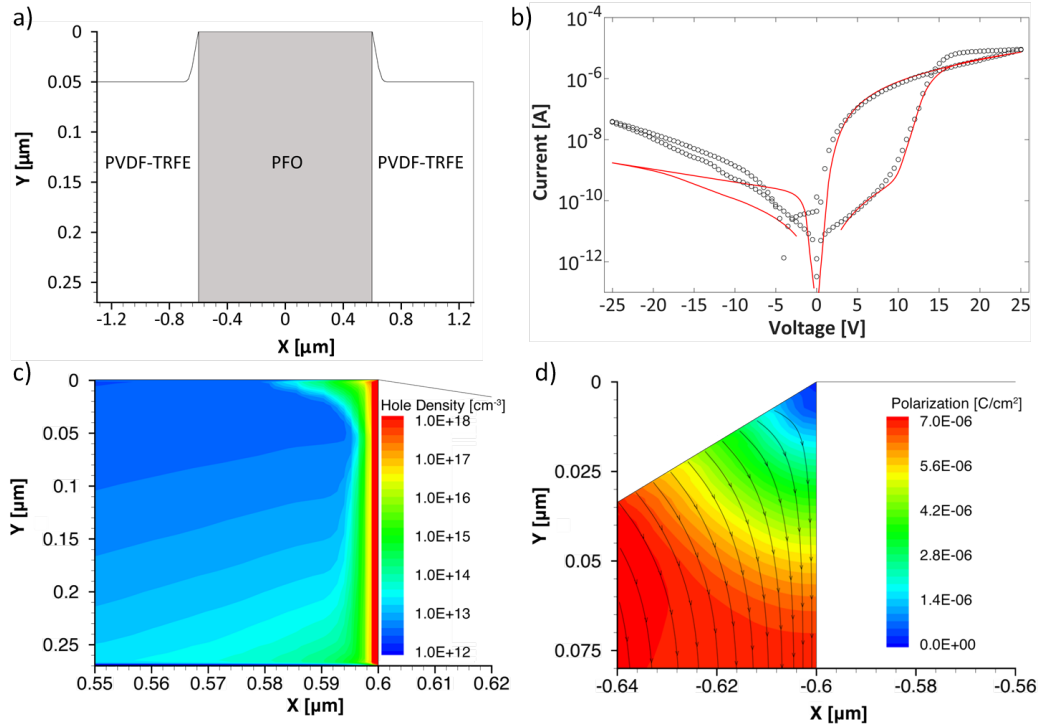
Figure 6.3: a) Cross-sectional device layout of the patterned memory diode. The detailed geometry as derived from morphology analysis (AFM) was used to form the 2D grid for the calculations. b) Measured (symbols) and calculated (lines) *I-V* characteristics of the patterned memory diode. For positive bias Au is the hole-injecting contact. c) Distribution of the hole-density in the PFO slab at its right interface with P(VDF-TrFE). d) Distribution of the polarization in P(VDF-TrFE) at the top PEDOT:PSS contact and at the left interface between P(VDF-TrFE) and PFO. This figure was published in [210].

The measured *I-V* characteristic of the patterned diode is presented as symbols in Figure 6.3b; it shows bistability and rectification as discussed in Section 5.3. Moreover, Figure 6.3b shows the calculated *I-V* characteristic (red line). Since the 2D polarization of the ferroelectric is explicitly taken into account, the entire *I-V* characteristic can be quantitatively described. The agreement between the experimental data and the calculations is remarkable considering that the parameters of the model are all physical parameters; they result from the characterization of a P(VDF-TrFE) capacitor and a PFO hole-only diode. Therefore, by separately characterizing the physics of the materials and including the results in the device model, which takes into account the geometry of the bilinear array, the charge transport in the patterned memory diode could be very precisely predicted.

It should be emphasized that the modeling goes far beyond pure fitting of the electrical measurements. The device simulator provides detailed information on the 2D distribution of electric field, polarization, charge density, and current in the memory diode at different bias voltages. As an example, Figure 6.3c shows the charge carrier density distribution in the PFO slab at +25 V (Au is the hole-injecting contact). The charge concentration is larger than 10^{18} cm^{-3} directly at the interface of PFO and P(VDF-TrFE). It decreases to 10^{15} cm^{-3} at 4 nm distance from the interface and it is below 10^{13} cm^{-3} in the bulk of the semiconductor.

Consequently, the current density is 5 orders of magnitude higher at the ferroelectric-semiconductor interface than in the bulk. The charge carriers are accumulated along the whole semiconductor-ferroelectric interface in Figure 6.3c and not only close to the injecting contact as suggested in a previous report [41]. The reason for the formation of a channel with high hole density is the lateral polarization component of P(VDF-TrFE); details will be given in the next section.

The analysis of the internal variables also allows to explain, why the memory diode is not switching for negative bias, when the top PEDOT:PSS electrode is the hole-injecting contact. Figure 6.3d shows the ferroelectric polarization in the left P(VDF-TrFE) slab close to the interface with PFO at -25 V. The bulk of the P(VDF-TrFE) slab is fully polarized, which explains the switching observed in the dielectric constant for both polarities in Figure 5.3d (Section 5.3).

However, the electric field in the P(VDF-TrFE) layer adjacent to the side wall of the PFO slab is negligible, too. The ferroelectric P(VDF-TrFE) is not polarized in this region, and thus, the stray field is negligible. The contact between PEDOT:PSS and PFO stays injection limited. As a consequence, the current density is low for negative bias and the memory diode is rectifying.

So far, the implemented device physics model is successful for the patterned memory diode, which is an ideal model system because of its symmetry. In order to demonstrate that the simulation approach works generically, it must allow to also model memory diodes with a random phase separated blend film. Moreover, variations in film thickness as well as temperature should be investigated. This is the subject of the following section.

6.6 Modeling memory diodes based on blends

Compared to patterned memory diodes the problem with phase separated blend films is that the distribution of PFO columns embedded in the matrix of P(VDF-TrFE) is random and the size of the domains can vary to a large extent, as demonstrated by the AFM micrograph of the blend film (thickness of 265 nm) in Figure 6.4a.

For the simulations, a device layout is needed, based on which the 2D grid can be designed. The utilized layout is schematically illustrated in Figure 6.4b. The PFO slab representing all PFO columns is introduced between two P(VDF-TrFE) slabs, which represent the entire matrix. This choice for the device layout is possible, because Figure 6.3c has shown that the interface between P(VDF-TrFE) is crucial. Therefore, all PFO columns can be represented by one slab of average width, if the area factor takes into account the entire PFO/P(VDF-TrFE) interface length on the device area.

In order to determine the average PFO domain diameter and the interface length, a thorough morphology analysis was performed: AFM micrographs were measured at six different positions of the blend film and the diameter
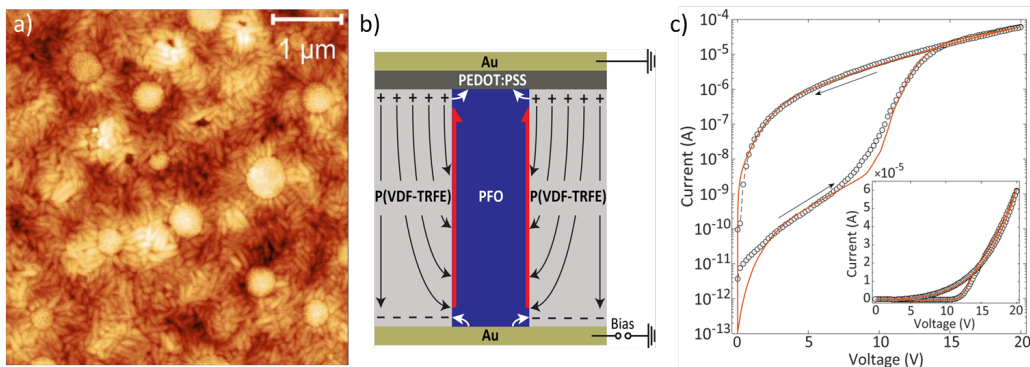
Figure 6.4: a) Typical AFM micrograph of a phase-separated blend film, where columns of PFO are embedded in the P(VDF-TrFE) matrix. The range of the color-coded height scale is 70 nm. b) Cross-sectional device layout of the comprising memory diode. c) Measured (symbols) and calculated (lines) *I-V* characteristics of the memory diode at ambient temperature. The inset shows the curve in linear scale. [233]

Table 6.1: Parameters for the numerical simulation of the memory diode.

Param.	Φ_{Au}	Φ_{PEDOT}	σ	Γ_0	ϵ_r (PFO)
Values	4.5 eV	5.0 eV	0.16 eV	$2 \times 10^5 S/cm$	3
Param.	a	E_c	P_r	P_{sat}	ϵ_r (PVDF)
Values	1.5 nm	42 MV/m	70 mC/m^2	70.001 mC/m^2	14

values were determined for all PFO domains. Based on that, the average PFO domain size and the area factor can be calculated and implemented into Figure 6.4b. The results of the analysis are presented in the Appendix together with the grid used for the numerical simulations. Unlike for the patterned diode, the phase separated blend does not show pronounced topography. Hence, the electrode lines for the Au bottom and the PEDOT:PSS top contact are flat in Figure 6.4b (for fabrication details cf. Section 3.6.3).

Figure 6.4c shows the measured *I-V* characteristic of the memory diode in a semilogarithmic scale. The inset shows the same curve on a linear scale (symbols). The arrows indicate the measurement sequence. Only positive bias (Au is the hole-injecting contact) is considered here. Curves including negative bias are presented in the Appendix together with further explanation on the role of PEDOT:PSS as top contact.

Sweeping the diode from 0 V to +20 V the current density is low for low bias as the Au-PFO contact is injection limited. The diode is in the Off-state. When the bias exceeds the coercive voltage, here around 10 V, the ferroelectric P(VDF-TrFE) gets fully polarized and the current increases by orders of magnitude. Since the ferroelectric polarization does not change upon sweeping back to 0 V, the diode remains in the On-state. In order to switch off the diode, the ferroelectric polarization has to be reversed by applying a negative voltage larger than the coercive voltage.

The *I-V* characteristic of the diode comprising a phase separated blend is very similar to the one of the patterned memory diode (Figure 5.3). Hence, it is not surprising that the calculated *I-V* characteristic in Figure 6.4c (orange line) is in excellent agreement with the experimental data. The parameters used for the calculation are listed in Table 6.1. It is emphasized again that the parameters were determined by experiments, as described in detail in Sections 6.2 and 6.3; they are not fitting parameters.

The measured *I-V* curve in Figure 6.4c is very reproducible. Repeating the positive sweep (after having poled P(VDF-TrFE) in the opposite direction with a negative bias sweep) always led to a very similar curve. It should be noted, however, that the very first measurement of the diode exhibited a

significantly lower Off-current for low positive bias, which excludes leakage as the origin of the Off-state current. Therefore, an unintentional doping density of $N_A = 10^{17}$ cm^{-3} was included into the calculation to account for the higher Off-state current with respect to the pristine diode. Further details on this topic are discussed in the Appendix.

It is well-established that the driving force for resistive switching is the modulation of the Schottky barrier by the ferroelectric polarization [41].
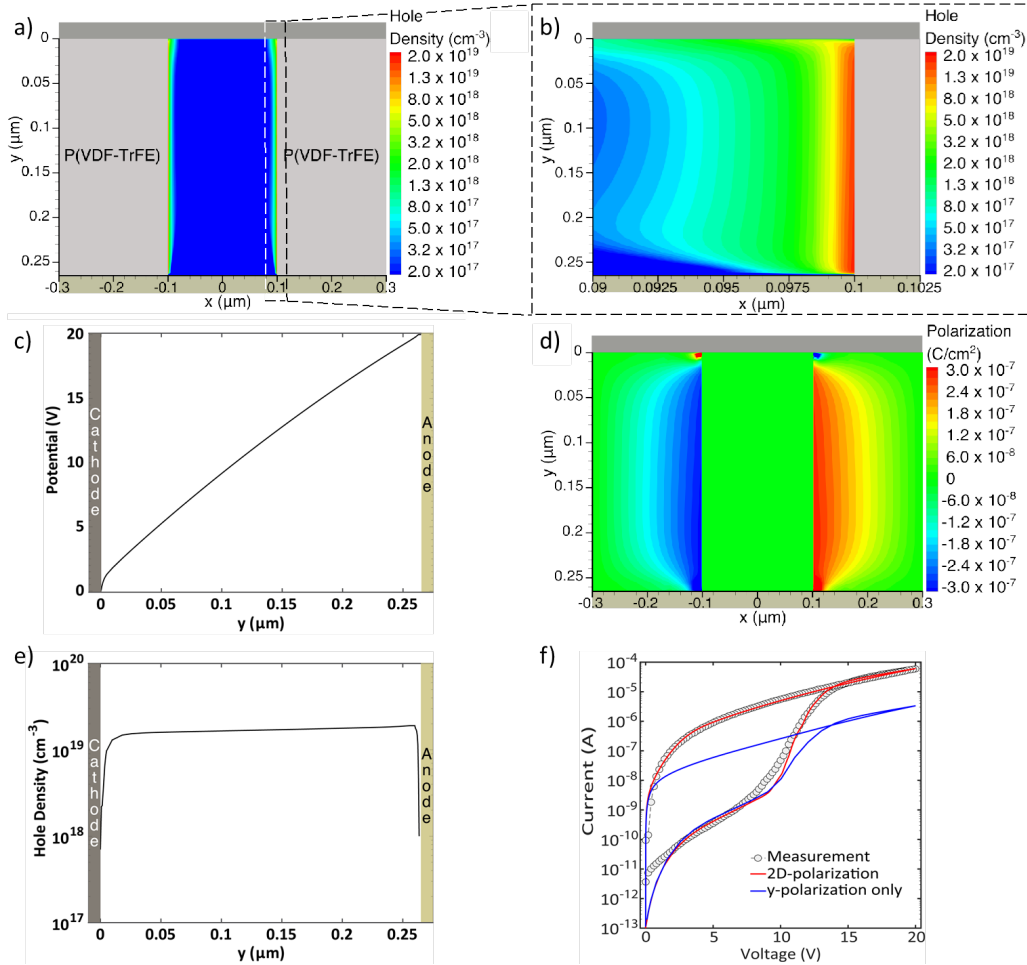
Figure 6.5: a) Hole density distribution in the PFO pillar at $V = 20$ V. b) Zoom of the hole density distribution at the right PFO/P(VDF-TrFE) interface. c) Potential along the PFO/P(VDF-TrFE) interface (cut line at $x = 0.099$ µm), V = 20 V. The anode corresponds to the injecting contact (Au), while the cathode corresponds to the collecting contact (PEDOT:PSS). d) x-component of the polarization vector at V = 20 V. e) Hole density along the PFO/P(VDF-TrFE) interface (cut line at $x = 0.099$ µm), V = 20 V. f) Measured (symbols) I-V characteristics of the memory diode presented together with the numerically calculated lines accounting for the 2D polarization ($P_x + P_y$, red line) or only for the y-component of the ferroelectric polarization, P_y (blue line). [233]

However, the underlying device physics has not been fully understood. Using the numerical simulations performed here, a large variety of parameters can be presented at different voltages, for instance, the distribution of the hole concentration or the 2D orientation of the polarization. This allows to understand the operational mechanism in detail.

Figure 6.5a shows the hole density distribution in the PFO slab when biased at +20 V. The injected charge carriers are confined at the ferroelectric-semiconductor interfaces along the whole thickness of the diode. Two separated 'channels' are formed. Figure 6.5b is a zoom of Figure 6.5a at the right PFO/P(VDF-TrFE) interface. The charge concentration at the interface is 2×10^{19} cm^{-3}, it is lower than 10^{18} cm^{-3} at a distance of 2.5 nm from the interface, and it drops to 10^{15} cm^{-3} in the center of the PFO pillar (not shown in Figure 6.5b). It is worth to note that in the center of the PFO pillar the large energy barrier at the injecting contact depletes the semiconductor over the whole diode thickness. Therefore, the charge carrier density is even lower than $N_A = 10^{17}$ cm^{-3}.

The charge carrier density in the accumulation layer is four orders of magnitude higher than in the bulk. The origin of the 'confinement' is the lateral x-component of the polarization vector in the P(VDF-TrFE) slab. Based on the diode geometry, it is expected that the polarization is oriented along the transverse y-direction. Hence, the formation of the x-polarization component is counterintuitive and it can be explained as follows: if P(VDF-TrFE) is fully polarized, a large stray electric field rises between the polarization charges of the ferroelectric polymer and the compensating image charges in the electrode. This is indicated by the white curved arrows at the bottom contact in Figure 6.4b. The stray field enables an efficient charge injection at the bottom corner of the semiconductor-ferroelectric interface.

The injected carriers set the local potential in the semiconductor equal to the bottom contact potential (Figure 6.5b, $x = 265$ nm), the electric field lines bend, and a lateral x-component of the electric field ($\vec{E}_x$) rises. Consequently, the electric field lines are no longer parallel to the interface, but exhibit a non-zero lateral component. When $\vec{E}_x$ is larger than the coercive field, a polarization component $\vec{P}_x$ occurs and the lateral displacement, $\vec{D}_x$, is enhanced. $\vec{D}_x$ is compensated by charge carriers, which further accumulate at the PFO/P(VDF-TrFE) interface. An accumulated channel along the whole interface from the bottom to the top contact is formed.

Figure 6.5d shows the x-polarization distribution in the P(VDF-TrFE) slabs. The x-polarization is about 0.3 mC/cm^2. Although this value is one order of magnitude lower than the y-polarization, it is high enough to maintain the charge accumulation. When the external applied voltage is decreased,

the x-polarization is retained by the ferroelectric polymer and, hence, the accumulated channel at the interface is preserved. This is demonstrated in the Appendix, where the hole-density and the potential distribution in the PFO slab are presented for a bias of $+5$ V. The charge carrier concentration in the channel is of course a bit smaller with respect to a bias of $+20$ V, but it is still as high as 5×10^{18} cm^{-3} directly at the interface of PFO and P(VDF-TrFE).

The x-polarization in Figure 6.5d is perfectly symmetric around the center of the PFO pillar, meaning that the negative polarization vectors at the left interface are mirrored by the positive polarization vectors at the right interface. The x-polarization is maximum (minimum) at right (left) side of the injecting bottom contact due to the stray field. The reverse situation holds at the collecting top contact, because the stray field points in the opposite direction. Therefore, close to the extracting contact, the charge carriers are pushed away from the interface. This results in a pinch-off of the accumulated channel.

As a confirmation, Figure 6.5e shows the density of holes, p, along the PFO/P(VDF-TrFE) interface between the two electrodes. The injecting bottom contact (Au) is located at $y = 265$ nm, while the extracting top contact is located at $y = 0$ nm. The injecting contact shows a 2.5 nm depletion region due to the width of the energy barrier at the contact. After the depletion region, the hole density is very high and almost constant along the whole PFO/P(VDF-TrFE) interface, before it drops at the top contact due to the oppositely oriented stray field.

In Figure 6.5f the measured *I-V* characteristic is presented together with calculated curves accounting for both x- and y-component of the polarization (red line) or accounting only for the y-component (blue line). If the non-linear ferroelectric x-polarization is not considered, the calculated current in the On-state is about two orders of magnitude lower than the measured current. Only if the full 2D polarization is implemented into the calculations, the modeling and the experiment match (red line). This substantiates the crucial role of the x-polarization of P(VDF-TrFE) on the device physics.

In previous work, the charge transport in organic ferroelectric memory diodes was suggested to be space-charge-limited, when the ferroelectric is fully polarized and the Schottky barrier can be overcome [38, 41]. Based on that the hole density in Figure 6.5e should follow $p \propto y^{-1/2}$ (cf. Section 2.3). This is, however, not the case. Instead, the constant hole density profile in Figure 6.5e resembles that of a field-effect transistor operating in the saturation regime, where the drain current, I_d, follows

$$I_d \propto \frac{V^2}{L}. \qquad (6.30)$$

Here, L is the channel length of the transistor, which corresponds to the film thickness of the diode, l. The applied voltage, V, is the gate voltage, V_g, minus the threshold voltage, V_{th} [5]. The operational mechanism of a field-effect transistor is briefly summarized in the Appendix. Although Equation 6.30 provides the same mathematical I-V relation as given by the Mott-Gurney law [79] (space-charge-limited current, Equation 2.11), where

$$I \propto \frac{V^2}{l^3}, \tag{6.31}$$

the underlying physics is completely different. In order to demonstrate that the memory diode works like a vertical transistor in saturation at pinch-off, memory diodes with varying thickness were fabricated. Figure 6.6a shows the On-state current as a function of voltage for devices with varying thickness of the phase separated blend. As expected, the current increases for decreasing thickness.

In order to more thoroughly investigate the relation between current and thickness, the films were analyzed with AFM. Since the morphology depends significantly on the film thickness, the effective PFO/P(VDF-TrFE) interface length had to be determined separately for each film (detailed analysis in the Appendix). Figure 6.6b shows the effective On-current extracted at 10 V versus the inverse film thickness. The effective On-current is the current in the On-state divided by the measured effective PFO/P(VDF-TrFE) interface length. Each data point belongs to measurements of at least six memory diodes. The least squares fit considering the three diodes with varying thickness has a slope of about 1. This proves that the current in the
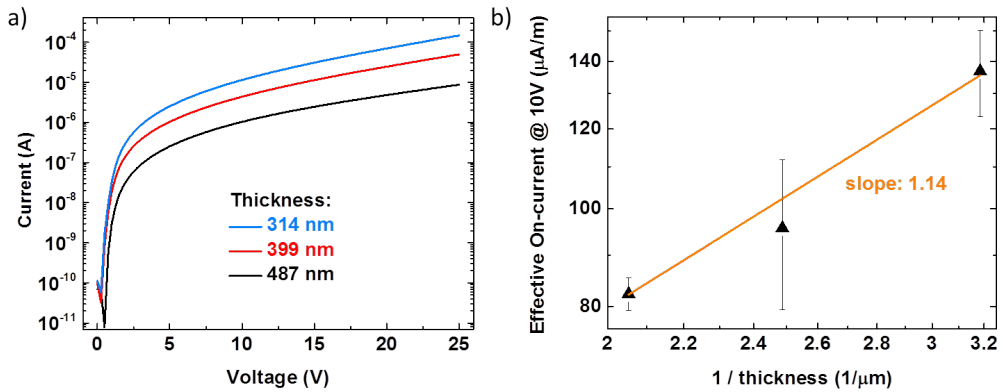
Figure 6.6: a) On-state current as function of applied bias for memory diodes with varying thickness of the P(VDF-TrFE)/PFO blend film. b) On-state current normalized by the effective interface length as a function of the reciprocal layer thickness [233]. The orange line is the linear least squares approximation, which exhibits a slope close to 1. Note that in the case of a space-charge-limited current, the slope would have to be 3, because $I \propto 1/l^3$ in SCLC.

memory diodes indeed depends inversely on the thickness. The memory diode, although being a two-terminal device, works like a transistor operating in saturation at pinch-off. The bottom contact corresponds to the source, the top contact is the drain, and the gate voltage is equivalent to the drain voltage.

It is emphasized again that in a previous theoretical work [41], the stray electric field had already been encountered as very important aspect for memory diodes. However, the subsequent conclusions, namely that current spreading in the semiconductor would occur and that the current would be space-charge-limited are in contrast to the findings of this work. This also applies to the charge injection mechanism proposed in reference [41].

6.7   Charge injection into memory diodes

As discussed above, the ferroelectric polarization makes the memory diode more complicated than a 'normal' Schottky diode. It is thus not clear in advance, which charge injection mechanism is dominant. When the ferroelectric P(VDF-TrFE) is fully polarized, the strong stray electric field between the polarization charges and the resulting image charges in the electrode allows efficient charge injection into PFO despite the high Schottky barrier. The question is, which injection mechanism benefits most from the stray field.

Figure 6.7a shows the charge carrier concentration in the PFO pillar close to the P(VDF-TrFE) slab and the injecting electrode (+20 V). The depletion width due to the contact barrier is less than 2.5 nm, which is compatible with charge injection via barrier tunneling. In the experiment, all charge injection mechanisms are present and it is difficult to find out, which of them is most important. In the numerical simulations however, one mechanism can be deliberately switched off and the impact on the calculated *I-V* characteristic can be evaluated.

Figure 6.7b shows the current calculated considering all injection mechanisms but barrier tunneling. Barrier lowering due to the image forces and the stray electric field are explicitly taken into account, but tunneling is switched off in this simulation. The resulting current (blue line) is two orders of magnitude lower than the measured current (symbols). Only if the injection by tunneling is included into the simulation (red line), the experiment and the calculation match.

It is surprising that the thermionic emission for instance can be disregarded with respect to the tunneling. Figure 6.7c shows the hole tunneling rate at the injecting contact. The hole tunneling rate is as high as 10^{26} cm^{-2}s^{-1}, efficiently providing almost all the charges transported in the

accumulated channel. The width of the energy barrier is only 2.5 nm. The ferroelectric polymer is fully polarized and barrier tunneling is due to the stray electric field and due to the accumulated channel, which causes a small depletion width. The Au-PFO contact then behaves like an ideal Ohmic contact.

Charge injection depends on the Schottky barrier height. Numerical simulations were carried out with varying energy barrier. Based on that, the On/Off current ratio at 5.3 V was calculated as a function of the injection barrier height; it is presented in Figure 6.7d. A field of $E = 2 \times 10^5$ V/cm,
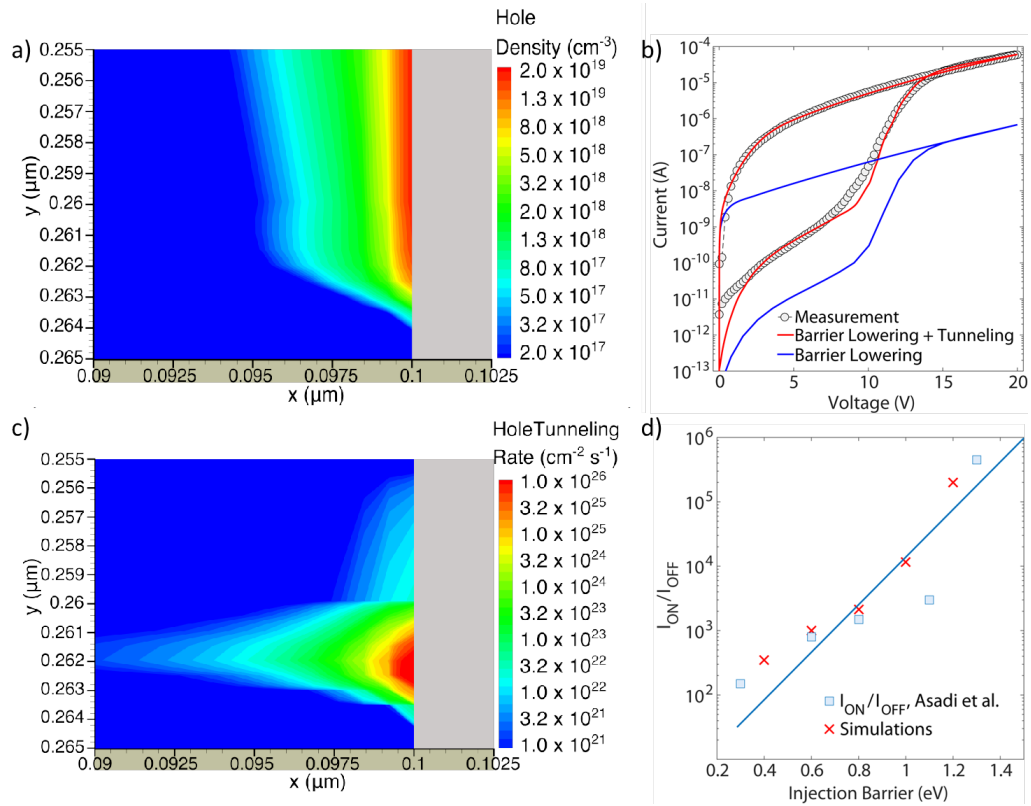
Figure 6.7: a) Hole density distribution within the PFO slab at the interface with P(VDF-TrFE) and close to the contact with Au ($V = 20$ V). b) Measured (symbols) and simulated (lines) *I-V* characteristics of the memory diode at room temperature. The blue line is calculated by switching off the barrier tunneling, and the injection is calculated accounting for only thermionic emission with image force barrier lowering. The red line considers all injection mechanisms. 'Barrier lowering' here includes all injection mechanisms apart from tunneling. c) Barrier tunneling rate within the PFO slab at the interface-contact corner, $V = 20$ V. d) On/Off current ratio as a function of injection barrier. Symbols correspond to experimental data taken from the publication of Asadi and co-workers [38], while the red crosses are the result of the simulation, and are obtained at $F_y = 2 \times 10^5$ V/cm. The line is the least squares approximation and exhibits a slope of 0.27 eV per decade of the On/Off ratio. [233]

which corresponds to 5.3 V, was chosen, so that a direct comparison with a thorough experimental study presented in reference [38] is possible. The On/Off current ratio is shown on a semi-logarithmic scale and a linear relation is obtained for the simulated data with a slope of 0.27 eV per decade of the On/Off ratio. This agrees very well with the experimentally extracted value of 0.25 eV/decade in reference [38] and again confirms the validity of the numerical simulations.

6.8 Temperature-dependent analysis

For a device physics model to be successful, it must allow to quantitatively describe the *I-V* characteristics not only at ambient conditions, but also at a variety of temperatures. Figure 6.8a presents the measured and the numerically calculated *I-V* characteristics of the memory diode in the temperature range between 250 K and 300 K. An excellent agreement between simulations and experiments is obtained proving the generality of the modeling.

Interestingly, the temperature dependence of the On-state current is very weak. Upon decreasing the temperature by 50 K the maximum current (at 20 V) decreases only by a factor of 3 and the On-state current at 3 V decreases by only one order of magnitude suggesting a low activation energy for hopping, E_A. The relation between the current and the activation energy
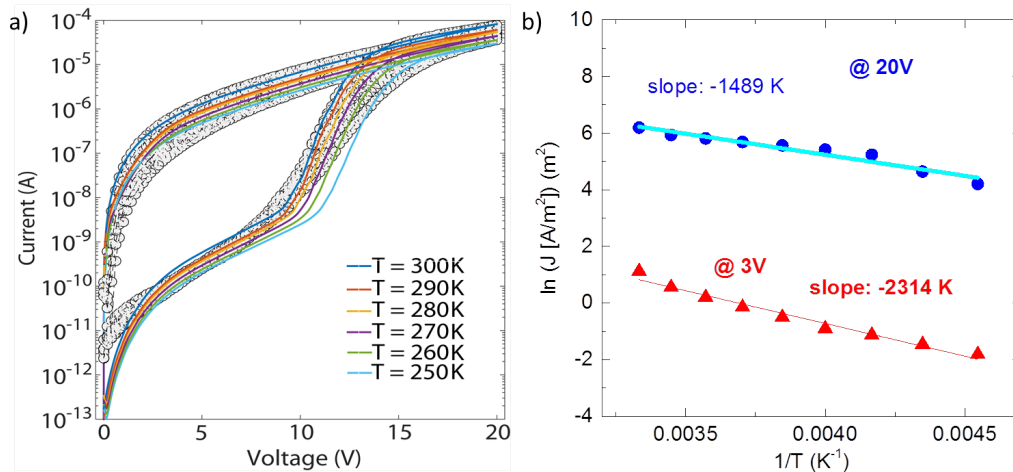
Figure 6.8: a) Measured (symbols) and simulated (lines) *I-V* characteristics of the thin film memory diode for temperatures varying between 250 K and 300 K [233]. b) Natural logarithm of the On-state current density as a function of the inverse temperature for an applied bias of 3 V and 20 V. From the slope of the least squares approximation, the activation energy can be determined by multiplying with the Boltzmann constant, k_B.

is typically expressed as

$$I \propto \exp\left(\frac{E_A}{k_B T}\right). \tag{6.32}$$

Therefore, in Figure 6.8a, the natural logarithm of the On-state current extracted at 3 V and at 20 V is plotted versus the inverse temperature. A linear relation is obtained as shown by the fitted lines, which represent the least squares approximation. The activation energy follows from multiplying the slope of the fit lines with the Boltzmann constant. This yields an activation energy of 130 meV at 20 V and 200 meV at 3 V.

For comparison, the activation energy of hole-only diodes is typically much larger, between 200 and 600 meV [85, 89]. The reason for the low temperature dependence is the very high charge accumulation at the PFO/P(VDF-TrFE) interface [43]. The low energetic states of the Gaussian DOS are all filled and the hopping is easier, because the energy barrier for nearest neighboring hopping is more likely to be lower, if the Fermi energy is higher.

6.9   Evaluating the integration density

Organic ferroelectric memory diodes are interface devices. Although this statement has been made earlier, the proof has only been provided in the previous sections. Figure 6.5 demonstrated that a hole accumulation channel is formed along the entire PFO/P(VDF-TrFE), while current spreading in the semiconductor was suggested earlier [41]. Based on the previous findings, a minimum feature size of 50 nm was suggested. In Figures 6.5 however, the width of the accumulated hole channel is only 2.5 nm implying that the limit for downscaling is significantly below 50 nm. Hence, the maximum integration density for organic ferroelectric memory diodes should be significantly above the value of 10 Mbit/cm^2 proposed earlier [41].

Figure 6.9a shows the charge carrier density in a PFO slab of only 5 nm width. Although the applied bias is only 5 V, which corresponds to a typical operating voltage of the diode, two accumulated channels occur along the entire PFO/P(VDF-TrFE) interface suggesting a minimum width of the semiconducting slab of only 5 nm.

A comprehensive evaluation of the minimum domain diameter (W) requires to consider the lateral dimensions of not only the semiconductor (W_{PFO}) but also of the ferroelectric polymer ($W_{P(VDF-TrFE)}$). Therefore, as a next step, $W_{P(VDF-TrFE)}$ was systematically varied , while $W_{PFO} = 5$ nm was kept constant. In order to make a detailed comparison between the different cases possible, the device area has to remain constant. This was realized by adjusting the area factor in each case.

The resulting calculated *I-V* characteristics for different domain sizes are presented in Figure 6.9b. The Off-state current is similar in all cases. If $W_{P(VDF-TrFE)}$ is reduced from 200 nm down to 5 nm, the On-state current decreases. This is counterintuitive, since the decrease of the ferroelectric domain size increases the effective semiconducting area of the memory diode. Hence, a current increase is expected. However, the downscaling of $W_{P(VDF-TrFE)}$ leads to a strong decrease of the *x*-polarization component. This is demonstrated in Figure 6.10, where the hole density in the PFO slabs (left column) and the *x*-polarization in the P(VDF-TrFE) slabs (right column) are shown for decreasing domain width of P(VDF-TrFE). When $W_{P(VDF-TrFE)}$ is reduced from 200 nm (Figure 6.10a) down to 50 nm (Figure 6.10b), the *x*-polarization decreases leading to a decreased charge accumulation in the PFO slab.

In the case of even smaller P(VDF-TrFE) domains ($W_{P(VDF-TrFE)}$ is 10 nm and 5 nm in Figures 6.10c and d, respectively), the *x*-polarization component occurs only in a portion of the ferroelectric slab and is extremely reduced. Hence, the charge carrier density is more than an order of magnitude lower compared to the case, where $W_{P(VDF-TrFE)} = 200$ nm. However, the On-state current for the case, where $W_{P(VDF-TrFE)} = 50$ nm, is the same as for the case, where $W_{P(VDF-TrFE)} = 200$ nm. The reason is that the decrease of $W_{P(VDF-TrFE)}$ dramatically increases the relative amount of PFO in the diode and thus the effective P(VDF-TrFE)/PFO interface length. As a consequence, the reduced charge accumulation due to the lower *x*-polarization is compensated by the increase of the effective device area. Figure 6.10b shows that even for the smallest feature size of 5 nm, a bistable diode is obtained with a current modulation of more than 7 decades. These
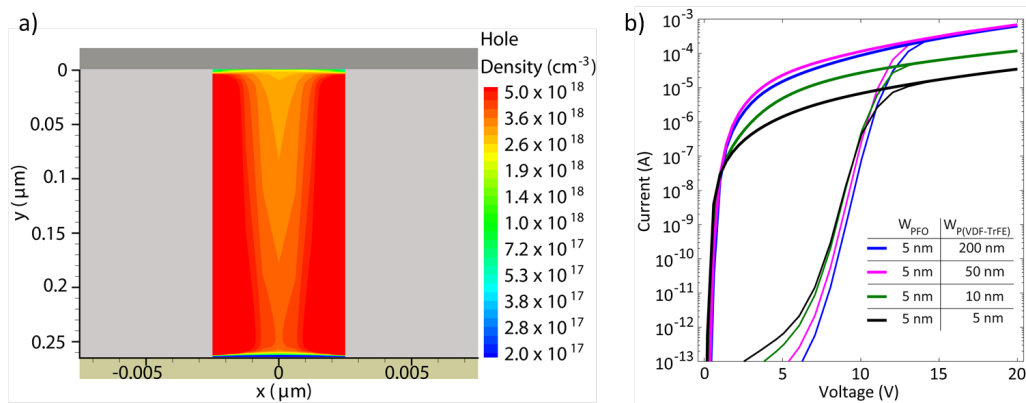
Figure 6.9: a) Hole density distribution in the PFO pillar with $W_{PFO} = 5$ nm and $W_{P(VDF-TrFE)} = 200$ nm, biased at 5 V. b) Comparison of the calculated *I-V* characteristics for varying domain sizes of P(VDF-TrFE). $W_{PFO} = 5$ nm was kept constant and the area factor was adjusted such that the device area was the same in all cases. [233]

results suggest that the maximum theoretical bit density of an array could be as high as 10^{11} bit/cm^2 considering that a single diode would have a total width of $F = 15$ nm (5 nm PFO surrounded by 5 nm P(VDF-TrFE) on both sides) and that in a cross-bar array, one diode requires a space of $4F^2$ [34].
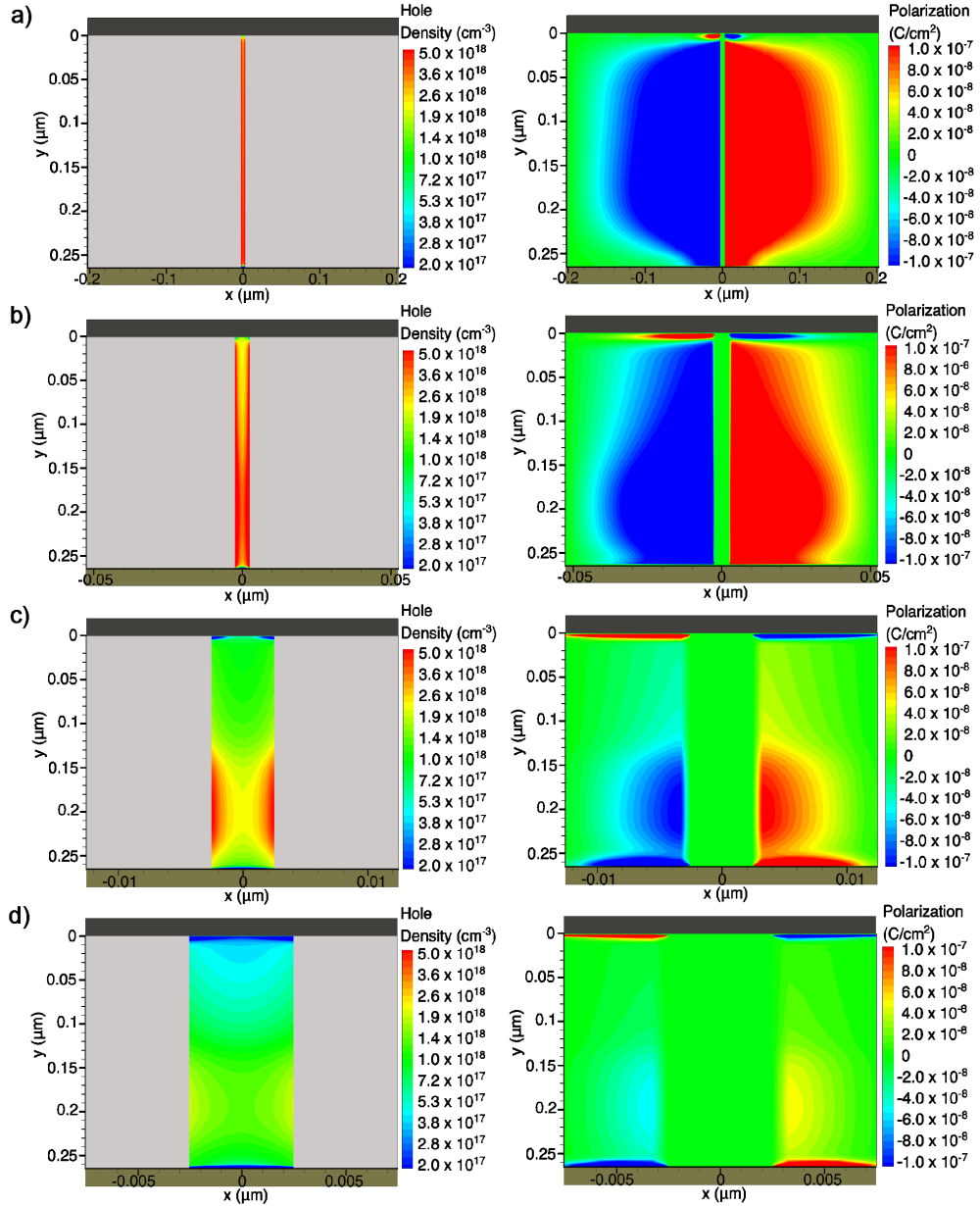
Figure 6.10: Hole density distribution in the PFO slab (left panels) and x-component of the polarization vector (right panels), at a bias of +5 V. The width of the PFO slab is $W_{PFO} = 5$ nm. The width of the P(VDF-TrFE) slab, $W_{P(VDF-TrFE)}$, is varied and it is a) 200 nm, b) 50 nm, c) 10 nm, and d) 5 nm. [233]

6.10   Summary of Chapter 6

In this chapter, the device physics of organic ferroelectric memory diodes was analyzed in detail. The three components needed for numerical simulations of the devices, were introduced one by one. First of all, the 2D ferroelectric polarization of P(VDF-TrFE) has to be taken into account. It is emphasized again that this was the most remarkable difference with respect to already published device models. The *D-E* hysteresis loops of P(VDF-TrFE) reference capacitors were measured at various temperatures and the characteristics could be excellently described using an empirical model by Miller and co-workers. Moreover, a model for polarization reversal was included to transfer the high-frequency results of the Sawyer-Tower setup to the quasi-static *I-V* measurements.

Secondly, the charge transport in PFO was characterized with hole-only diodes and the resulting *I-V* curves could be quantitatively described following a percolation model for hopping in a Gaussian DOS. The third and last component is the charge injection at the Schottky contact between Au and PFO. Here, the disorder of the polymer also plays an important role, as it impacts on the effective energy barrier and thus on the charge carrier density close to the interface. The equations for thermionic emission and barrier tunneling used in the numerical device simulator were adapted accordingly.

With these three components, complete *I-V* measurements as a function of temperature could be quantitatively described for the first time. The device simulator also allows the evaluation of the internal device variables, such as electric field and charge carrier concentration. The distribution of these parameters can be analyzed at varying voltages. The following main conclusions could be drawn: one key ingredient in the memory diode is the lateral polarization in P(VDF-TrFE), which leads to the formation of a strongly accumulated hole density along the entire interface of PFO and P(VDF-TrFE). Consequently, the current transport in the On-state is not space-charge-limited but resembles the channel current in a field-effect transistor operated in saturation at pinch-off. Experimental proof could be obtained with a detailed thickness scaling analysis, which demonstrated that the current density indeed scales linearly with the inverse film thickness.

It is worth noting that the device model worked both for the patterned memory diode as well as for phase separated blends. This is related to the fact that the input parameters were all physical and not fitting parameters. They were derived from actual devices (hole-only diodes for charge transport and capacitors for ferroelectric analysis).

The stray electric field between the polarization charges in P(VDF-TrFE) and the image charge in the Au electrode modulates the injection barrier.

Surprisingly, the charge injection is clearly dominated by barrier tunneling, while thermionic emission can be disregarded.

Chapter 7

Novel concepts for memory diodes: thin film thermistors

In the previous chapter the charge transport in organic ferroelectric memory diodes was described in detail. The polarization of the ferroelectric polymer and the charge transport through the semiconducting polymer are correlated due to the Schottky contact between the injecting electrode (Au) and the semiconducting PFO. Depending on the orientation of the ferroelectric polarization, the current through the diode is either high or low. While the two bistable states were used for memory applications in the previous chapters, this chapter describes a novel device concept: a thin-film thermistor with positive temperature coefficient (PTC).

After explaining the operational mechanism and the state of the art of PTC thermistors, the ferroelectric properties of P(VDF-TrFE) are analyzed as a function of the VDF:TrFE ratio and the temperature. P(VDF-TrFE) depolarizes at the Curie point. As a consequence, the On-state current density of a memory diode comprising PFO and P(VDF-TrFE) drops at the Curie temperature, too. Since the drop of the current density at a fixed voltage is equivalent to a strong increase of the resistance, the memory diode acts as a thin film PTC thermistor. The Curie temperature depends on the VDF:TrFE ratio, and hence, the switching temperature of the thermistor can be tuned. This novel device concept has been published in *Applied Physics Letters* [259].

7.1   What is a PTC thermistor?

A thermistor is a resistor with temperature-dependent resistance. If the resistance increases with temperature, the thermistors shows a positive temperature coefficient (PTC), and if the resistance decreases with increasing temperature, the temperature coefficient is negative (NTC). The latter is found in disordered semiconductors, where charge transport relies on thermally activated hopping between localized states.

Typical PTC materials are metals. At higher temperatures electron scattering is more pronounced leading to a lower mobility and thus a higher resistance. Technologically relevant PTC thermistors can be divided into two groups according to their operational mechanism. The first group utilizes doped single-crystalline silicon as a semiconductor. These so-called silistors exhibit a linear resistance-temperature curve with a small PTC. They are typically used as temperature sensors.

If a PTC thermistor is to be applied as self-regulating heat element or current limiter for overcurrent protection [260–262], the resistance-temperature relation needs to be non-linear. The corresponding second group of PTC thermistors is called the switching-type and comprises four material concepts [263]: ceramic composites [264–266], V_2O_3 based compounds [267, 268], polymer composites [262, 269, 270], and $BaTiO_3$ based compounds [261, 271–273]. The most prominent example for polymer composite PTCs is carbon black embedded in an insulating polyethylene matrix [274–276]. At room temperature the conductive particles just form a percolating path and the resistance is low. When the temperature increases, the large volume expansion of the semi-crystalline polymer close to its melting point breaks up the percolation path and the resistance increases dramatically.

The most commonly used switching-type PTC thermistor, however, is based on ferroelectric doped $BaTiO_3$ ceramics [263, 271, 277–279]. Undoped $BaTiO_3$ is an insulator and as such cannot be used as a PTC thermistor. Therefore, $BaTiO_3$ is n-type doped by replacing Ba with a trivalent donor such as La or by replacement of Ti with pentavalent Nb [280, 281]. The electron traps at the grain boundaries dominate the resistance and the PTC effect. Above the Curie temperature the dielectric constant decreases according to the Curie-Weiss law. This results in a linear increase of the potential barrier at the grain boundary. Since the resistance depends exponentially on the potential barrier, it increases by orders of magnitude above T_c.

The commercial switching-type PTCs are typically bulky, made as discrete components or as surface mounted devices. The manufacturing process of densely sintered, ceramic $BaTiO_3$ is very critical. The high process temperature can lead to intermixing. In addition, strain caused by the substrate

Table 7.1: Extracted ferroelectric parameters of P(VDF-TrFE) with different composition. Values are listed for the remanent polarization, P_r, the coercive field, E_c, and the Curie temperature, T_c (in Kelvin), obtained from hysteresis loops, from differential scanning calorimetry (DSC) measurements and from literature reports [172, 283, 284].

VDF:TrFE	P_c (mC/m^2)	E_c (MV/m)	T_c	T_c (DSC)	T_c (Lit.)
50:50	47	65	332	337	331
65:35	61	64	371	378	368
80:20	65	82	393	400	397

can suppress the phase transition [273]. The operational mechanism relies on the resistance modulation of grain boundaries, which cannot easily be transferred to thin films. As a consequence, thin film thermistors are elusive; in the following it will be demonstrated how the device physics of a memory diode can be utilized to realize a thin film switching-type PTC thermistor.

7.2 P(VDF-TrFE) at higher temperatures

As a first step, the ferroelectric properties of P(VDF-TrFE) at higher temperatures were characterized in capacitors with Au bottom and top electrodes. Thin films of about 300 nm were fabricated by wire-bar coating (for details see 3.6.3) and annealed at 140 °C for 2 hours in vacuum to enhance the ferroelectric properties of P(VDF-TrFE) [282]. Figure 7.1a shows the *D-E* characteristics at ambient temperature for the thin film capacitors with different compositions of VDF and TrFE. As long as the content of VDF is 50% or higher, the copolymer is ferroelectric and shows typical hysteresis curves. The values extracted for P_r and E_c are listed in Table 7.1.
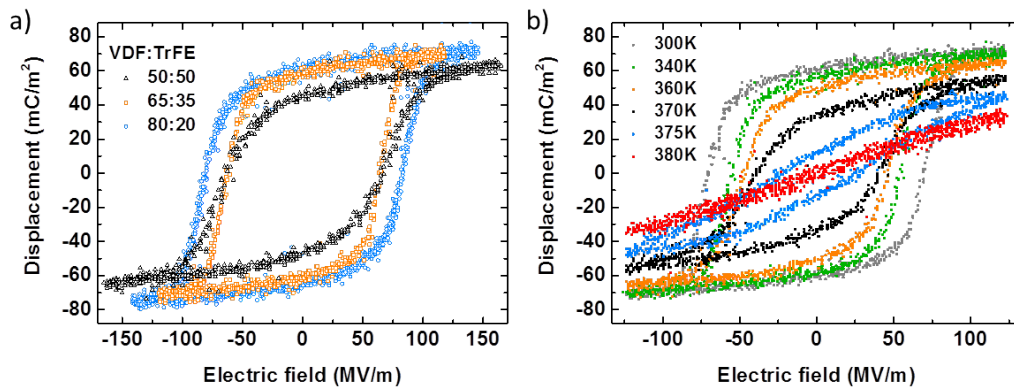
Figure 7.1: a) *D-E* loops for thin film capacitors with different composition of VDF and TrFE [259]. b) Hysteresis loops for VDF:TrFE = 65:35 for varying temperatures.

Hysteresis loops as a function of temperature for VDF:TrFE = 65:35 are presented in Figure 7.1b. Up to 360 K (orange curve) the *D-E* characteristics exhibit hysteresis and the remanent polarization is only slightly below the value at 293 K. For even higher temperatures P_r drops fast, and at 380 K the *D-E* characteristic becomes a straight line (red curve) meaning that P(VDF-TrFE) is completely depolarized and the electric response is that of a linear dielectric. The remanent polarization as a function of temperature normalized with respect to P_r at 293 K is shown in Figure 7.2a for the different copolymer compositions. The Curie temperature is arbitrarily extracted as the temperature, where P_r has decreased by 50 %, and it is listed in Table 7.1. For VDF: TrFE = 50:50 the Curie temperature is at about 332 K and for VDF: TrFE = 65:35, $T_c \approx 371$ K. Finally, $T_c \approx 393$ K for a composition of 80:20. As observed in literature the Curie temperature increases with increasing content of VDF [154].

Differential scanning calorimetry (DSC) is an excellent tool to determine the Curie temperature of ferroelectric polymers. Since the ferroelectric-to-paraelectric transition is an order-disorder transition in P(VDF-TrFE), it appears as an endothermic peak in the heating cycle of a DSC measurement (for experimental details see Section 3.5). In a typical DSC analysis a sample first undergoes a heating cycle, before it is cooled down with the same (negative) cooling rate. Subsequently, a second heating cycle is carried out, which is used for characterization, because any influences of the processing, which might impact on the measurement, are excluded due to the thermal treatment of the first cycle. Figure 7.2b shows the second heat cycles for the three copolymer compositions. The values of T_c extracted from DSC are also listed in Table 7.1. They are in good agreement with the electric characterization in capacitors and with literature reports [172, 283, 284].
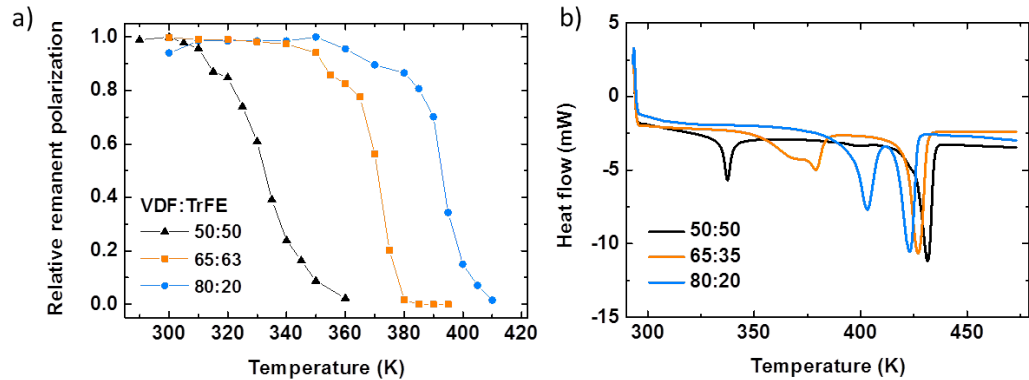
Figure 7.2: a) Remanent polarization as a function of temperature normalized by the reference value at ambient temperature for varying VDF:TrFE compositions [259]. b) Heat flow as a function of temperature from the 2nd heating cycle of DSC measurements.

7.3   Memory diodes at higher temperatures

Memory diodes with phase separated blends of P(VDF-TrFE) and PFO
were also fabricated using wire-bar coating at elevated temperatures to de-
crease the surface roughness and increase the yield [39]. With Au bot-
tom and top electrodes symmetric J-V characteristics are obtained as pre-
sented in the Appendix. The corresponding characteristics for a diode with
VDF:TrFE = 65:35 measured at 370 K, 380 K, and 390 K are presented in
Figure 7.3a. Here, only positive bias is considered. For 370 K the curve is
similar to the J-V charachteristic at 293 K with a slightly lower switch-on
voltage due to the facilitated switching at higher temperatures [179].

At 380 K, the On/Off-ratio decreases considerably, as the On-state cur-
rent density at 4 V is more than two orders of magnitude lower compared
to 370 K. P(VDF-TrFE) is close to its T_c value and is therefore partially
depolarized leading to a decreased On-state current density. At 390 K, the
J-V characteristic does not show switching at all, because P(VDF-TrFE) is
completely depolarized. The current density is low, even if a high bias was
applied beforehand. Note that at high voltages, the current density increases
significantly also for 390 K, because the high electric field forces the dipoles
of P(VDF-TrFE) to align resulting in enhanced charge injection and trans-
port. However, if the bias is removed, the dipoles move back into a random
orientation, typical for the paraelectric state. At 4 V the current density of
the diode is then equivalent to the Off-state at 293 K.

Figure 7.3b shows the extracted current density in the On-state at 4V
as a function of temperature (blue curve, left axis). The diode was first
poled in the On-state, then, the current at 4 V was monitored at increasing
temperature. Up to 370 K, the current density stays constant and is about
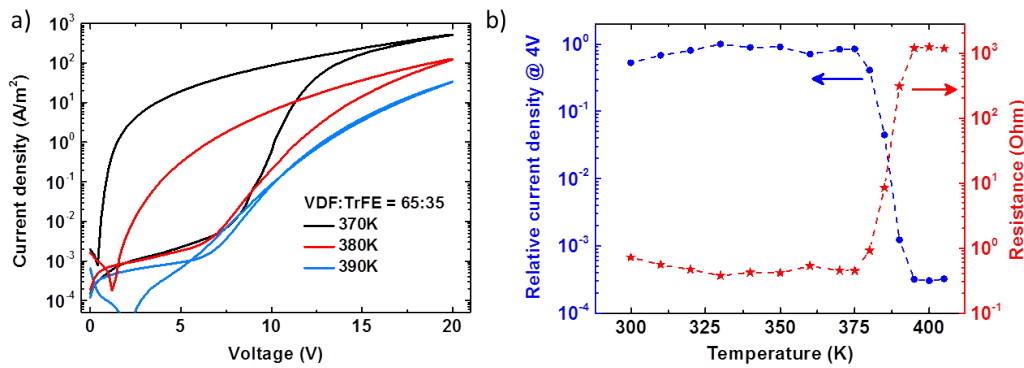
Figure 7.3: a) J-V characteristics of a blend diode for three different temperatures;
here, with VDF:TrFE = 65:35. b) Left axis: extracted current density at 4 V of the diode
presented in a) as a function of temperature. Right axis: calculated resistance at 4 V
versus the temperature showing non-linear switching-type PTC behavior.

the same as the reference value at 293 K. A significant increase of the current density is not observed, although charge transport of PFO is thermally activated suggesting improved transport for higher temperatures. The high current density in the memory diode is due to the ferroelectric polarization, as explained in detail in the previous chapter. Since the remanent polarization hardly changes between room temperature and 370 K (Figure 7.2a), the current density in the On-state at 4 V does not change much either. The effect of thermal activation on charge transport has much less impact on the current density than the charge accumulation due to the ferroelectric polarization.

Between 375 K and 395 K, the current density in Figure 7.3b decreases by more than three orders of magnitude. The onset temperature for the drop in current density of about 380 K agrees very well with T_c obtained from electric characterization of P(VDF-TrFE) thin film capacitors and the DSC measurements. This confirms that the drop of current is due to the depolarization of P(VDF-TrFE) at the ferroelectric-to-paraelectric transition. It should be emphasized that the current density extracted at a given voltage is equivalent to the inverse of the diode's resistance. The resistance of the diode at 4 V is plotted as the right axis in Figure 7.3b. The resistance increases by orders of magnitude, if the temperature exceeds T_c yielding non-linear PTC behavior. Hence, around T_c the organic ferroelectric memory diodes acts as switching-type thin film PTC thermistor.

For practical applications the PTC behavior needs to be reversible. If the diode presented in Figure 7.3b is cooled down from about 400 K back to room temperature, the current density stays low as demonstrated by the green circles in Figure 7.4a (the line is a guide to the eye). P(VDF-TrFE) remains unpolarized and thus the diode remains in the low current-high resistance state. This is undesired for a switching-type PTC thermistor, as it could only be used once for overcurrent protection.

By applying a voltage pulse larger than the coercive voltage, the diode can be reset into the high current density On-state as illustrated by the dark green arrow in Figure 7.4a. After a pulse of 20 V is applied, the current density of the diode at 4 V is enhanced by four orders of magnitude.

In order to obtain reversible PTC behavior, the conducting state has to be recovered at each temperature. This can be achieved by poling the diode before each read-out. The blue triangles in Figure 7.4a represent the current density obtained at 4 V after poling the diode with a 20 V pulse for each temperature. The curves for heating and cooling coincide meaning that the PTC behavior is indeed reversible.

The origin of the switching-type PTC behavior is the ferroelectric-to-paraelectric phase transition of P(VDF-TrFE). As demonstrated in Figure 7.2,

T_c is a function of the copolymer composition. As a next step memory diodes with PFO and VDF:TrFE = 80:20 as well as 50:50 were electrically characterized at higher temperatures. The extracted current density-temperature curves are presented together with the reference (65:35) thermistor in Figure 7.4b. The current density drops by orders of magnitude for all three devices. Again, higher content of VDF leads to a higher transition temperature of the diode/thermistor.

The PTC behavior is reversible, if a polarizing voltage pulse is applied before reading out the current at 4 V. The hysteresis in the measurements is similar to that observed in the DSC measurements (comparing 1st and 2nd heating cycle) and can be minimized by adjusting the processing conditions and the poling protocol. For instance, the smaller hysteresis for VDF:TrFE 65:35 in Figure 7.4b (orange squares) as compared to Figure 7.4a (green circles) is realized using a longer poling time.

In all three cases, the transition temperature of the thermistor coincides with the Curie temperature of P(VDF-TrFE) used in the phase separated blend confirming the operational mechanism described above. Hence, in the thin film PTC thermistor concept presented here, the transition temperature can be tuned by the P(VDF-TrFE) composition.
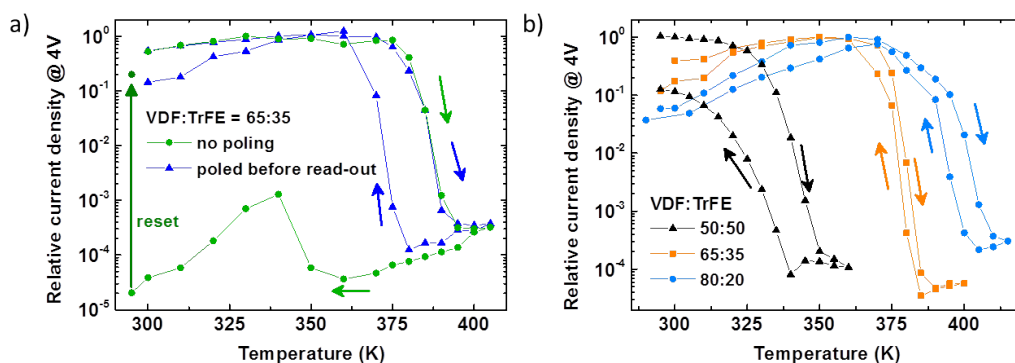
Figure 7.4: a) Extracted current density normalized with respect to the maximum current density at 4 V as a function of temperature for a memory diode with VDF:TrFE = 65:35. The green circles correspond to a typical measurement, where the diode was once (in the beginning) poled in the On-state before the current was monitored as a function of temperature. The line is again a guide to the eye. The small green arrows indicate the sequence of the measurement (first increasing, then decreasing temperature). The depolarized diode can be reset into the On-state by applying a voltage pulse with a bias larger than the coercive voltage as indicated by the dark green arrow. Reversible PTC behavior (dark blue triangles) is obtained if the diode is polarized with a voltage pulse before every read-out. b) Relative current density as a function of temperature for diodes with different P(VDF-TrFE) compositions. Before read-out at 4 V, the diodes were always poled into the On-state using a 20 V poling pulse. [259]

7.4   Summary of Chapter 7

In this chapter, a novel application for organic ferroelectric memory diodes was demonstrated. The diodes can act as thin film PTC thermistors, because the current density through the semiconductor depends on the polarization of the ferroelectric polymer. The operational mechanism of the thermistor relies on the ferroelectric-to-paraelectric transition of the ferroelectric copolymer at the Curie temperature. Upon depolarization of P(VDF-TrFE), the current density of the diode/thermistor exhibits a non-linear decrease. The decrease of the current density, which is equivalent to an increase of the resistance of the thermistor, can be made reversible as required for a PTC thermistor.

The switching temperature of the PTC thermistor can be tuned by varying the composition of VDF with respect to TrFE in the ferroelectric copolymer, because the composition itself determines the Curie temperature. While state-of-the-art PTC thermistors are typically bulky and can only be used as surface mounted devices, this chapter provides the first demonstration of a thin film concept for a PTC thermistor. This breakthrough allows combination of thin film thermistors with integrated circuits expanding the scope of applications of flexible electronics.

Chapter 8

Conclusion and Outlook

In this thesis, novel concepts for organic ferroelectric memory diodes are demonstrated. Up to date, the diodes typically consisted of a phase-separated blend of P(VDF-TrFE) and an organic semiconductor. The configuration of random semiconductor domains embedded in a P(VDF-TrFE) matrix causes several problems. For instance, the integration density is limited.

To that end, solution micromolding is established as patterning technique and utilized to prepare line gratings of one polymer, which can be backfilled with a second polymer yielding a well-defined bilinear array. At first, arrays of P(VDF-TrFE) and the non-ferroelectric insulator PVA are investigated in capacitors. The polymer, which is patterned first, always protrudes and the bilinear array exhibits topography. A decreased remanent polarization is observed, if P(VDF-TrFE) protrudes. Theoretical calculations suggest that the origin is an inhomogeneous distribution of the electric field inside the capacitor. The topography is more favorite, if PVA protrudes, and consequently, the corresponding capacitors show the same remanent polarization as benchmark capacitors, if the effective area of P(VDF-TrFE) is considered.

Reported patterning approaches for organic ferroelectric memory diodes share one problem: an overlayer of the second polymer was typically found on top of the P(VDF-TrFE) structures patterned first. This can be avoided with the process established in this work: the micromolded grating of the organic semiconductor poly(9,9-dioctylfluorene) is backfilled with P(VDF-TrFE) using the hotpress and a flat unstructured elastomeric stamp yielding a bilinear array without overlayer. Memory diodes with Au as injecting contact and the polymer conductor PEDOT:PSS as top contact show excellent memory performance. The high current density On-state and the low current density Off-state can serve as Boolean '0' and '1', the On/Off current ratio is higher than 10^3 and is retained for more than 10^4 s. The read-out voltage is as low as 2.5 V promising low power consumption. The memory diode is not

only bistable but also rectifying, meaning that it does not switch on for high negative bias. This is ideal for cross-bar memory arrays, where rectification is desired to reduce cross-talk between single devices.

The patterned memory diode is an ideal model system, because the detailed geometry of the bilinear array extracted with AFM analysis can be implemented into a numerical device simulator. Based on that, the experimentally obtained current-voltage characteristics can be quantitatively described. The two-dimensional ferroelectric polarization of P(VDF-TrFE), which was completely ignored in previous reports, serves as key ingredient. An excellent agreement between the measurements and the calculations is achieved. Importantly, the model can also be applied to random phase separated blend memory diodes measured at a range of temperatures.

It should be emphasized that the numerical device simulator does not only calculate current-voltage curves. It provides detailed information about the distribution of electric field and charge carrier density inside the diode. This enables understanding the device physics of organic ferroelectric memory diodes. If P(VDF-TrFE) is fully polarized, the stray electric field between the polarization charges and the resulting image charges in the electrode allows efficient charge injection via barrier tunneling. The entire current is then governed by a charge accumulation channel of only 2.5 nm width. This is due to the lateral polarization of P(VDF-TrFE). The diode, although being a two-terminal device, operates like a transistor in saturation at pinch-off.

Solution micromolding allows systematic variation of the pitch width of the bilinear arrays using stamps with smaller feature dimensions. Scaling the pitch width from 2 μm to 500 nm, the On-state current density of the resulting memory diodes exhibits a superlinear increase, although only a linear increase is expected. This confirms that a higher integration density can be realized by enhancing the effective interface length between the polymers.

The problem with solution micromolding is the swelling of the stamp. Alternatively, nano-imprint lithography could be used to obtain PFO nanogratings, which could then be backfilled with the technique demonstrated in this work. Since nano-imprint lithography has recently also been tested for high throughput reel-to-reel nanostructuring on flexible substrates [285], the fabrication of memory diodes with high integration density for the use in flexible electronics appears feasible in the future.

Another interesting outcome of this work is that understanding the device physics can open up novel application opportunities. In the memory diodes, the current through PFO is determined by the ferroelectric polarization of P(VDF-TrFE). The latter drops at the ferroelectric-to-paraelectric transition yielding a sudden increase of the diode's resistance. Based on that the first thin film switching-type PTC thermistor has been demonstrated.

Appendix A

Supporting Information (SI)

A.1   SI for Chapter 4

In this section, the impact of the molecular weight on the process of solution micromolding will be discussed first, before the issue of depolarization will be addressed in more detail.

Besides the solution concentration the molecular weight is another important parameter for solution micromolding. Figure A.1a shows a P(VDF-TrFE) line grating obtained with a concentration of 150 mg/ml (DMSO). The copolymer has a weight-average molecular weight of about 365 kg/mol.
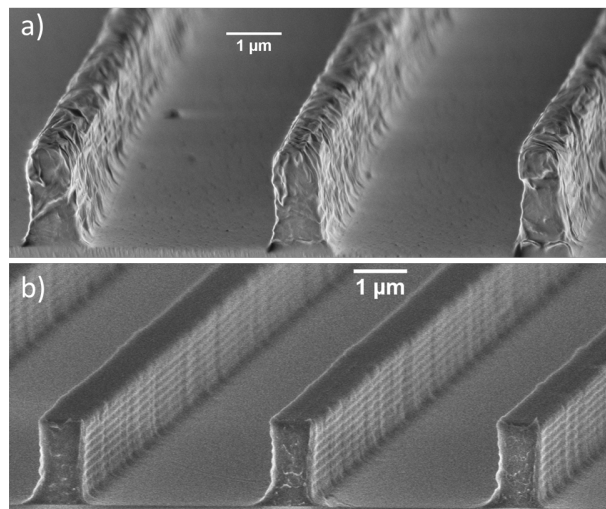
Figure A.1: (a) SEM micrograph (cross section) of P(VDF-TrFE) line grating obtained by micromolding a solution of 150 mg/ml. (b) Cross-sectional SEM micrograph of a PVA line grating. The concentration used for solution micromolding was 300 mg/ml.

By contrast, the weight-average molecular weight of PVA used in this work is only 27 kg/mol. As a consequence, a much higher concentration of 300 mg/ml was needed to obtain line gratings with similar feature dimensions. The resulting cross-sectional SEM micrograph is presented in Figure A.1b. Despite the high concentration, there is hardly any debris in between the PVA lines. The lower molecular weight allows higher solution concentrations upon micromolding.

The unsaturated hysteresis loops of ferroelectric capacitors are called inner loops. The inner loops of a patterned capacitor, where P(VDF-TrFE) protrudes, are presented in Figure A.2a. The slope of the inner loops is equivalent to the slope of the saturated loop. At low bias, the *D-E* curve of a ferroelectric capacitor is a straight line, as it only shows a linear dielectric response. From the straight, line the capacitance can be determined. If depolarization was an issue, then the slope of the saturated loop should deviate from the slope of the straight line and the slopes of the inner loops at zero bias. This is not the case, suggesting that the lower P_r value measured for the patterned capacitor is not due to depolarization.

The capacitance of the patterned devices was extracted from the hysteresis loops and also determined by small angle impedance spectroscopy. The values are listed in Table A.1 together with the calculated geometric capacitance accounting for the topography. In both cases (P(VDF-TrFE) or PVA protrudes), the capacitance measured with different techniques nicely agrees, but the experimentally determined values are lower than the theoretical ones. This might be caused by geometric effects such as an increased top electrode area due to the topography.
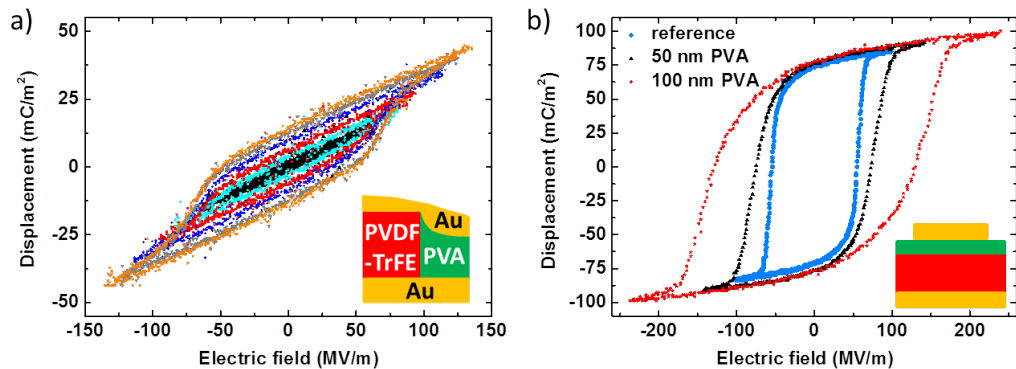
Figure A.2: (a) Inner *D-E* hysteresis loops of a patterned capacitor. P(VDF-TrFE) protrudes in the bilinear array as schematically illustrated in the inset. b) *D-E* curves of a bilayer capacitor, where a thin layer of PVA was deposited on an annealed P(VDF-TrFE) thin film. The capacitor layout with Au electrodes is again shown as inset.

Table A.1: Extracted device parameters of patterned capacitors, where either P(VDF-TrFE) protrudes or PVA protrudes. Each value is the mean average of at least 5 capacitors and the results could be reproduced in each case. The remanent polarization, P_r, is extracted from Sawyer-Tower measurements. The linear capacitance was extracted both from the slope of the hysteresis loops at zero bias and from small angle impedance measurements. The geometric capacitance as calculated from the measured topography is included for comparison.

Sample	P(VDF-TrFE) protrudes	PVA protrudes
$P_\mathbf{r}$	42.6 ± 4.4 mC/m^2	70.8 ± 8.0 mC/m^2
Cap (impedance)	16.2 ± 4.9 pF	12.8 ± 2.4 pF
Cap (hysteresis)	17.4 ± 5.6 pF	13.6 ± 1.2 pF
Cap (geometric)	5.0 pF	10.3 pF

The question was brought up, whether a very thin overlayer of PVA on top of the P(VDF-TrFE) lines could cause depolarization. It should be noted that such an overlayer would change the capacitance of the overall device. Hence, it could explain the equivalent slopes of inner and saturated loops and, simultaneously, it could cause depolarization and thus explain the lower value of P_r, if it acts as perfect insulator [286].

Therefore, bilayer capacitors were fabricated, where a thin film of PVA was deposited on a benchmark film of P(VDF-TrFE). The layout of the resulting capacitor is illustrated as inset of Figure A.2b. As always, the red bar represents P(VDF-TrFE) and the green bar (on top of it) represents PVA. The ferroelectric hysteresis loops of two typical bilayer capacitors are presented in Figure A.2b together with a benchmark *D-E* loop (black curve). The film thickness of PVA in the bilinear capacitors was varied.

In all cases, the remanent polarization is equivalent to that of the benchmark device, while the coercive field is significantly higher. The origin lies in charge injection into PVA from the electrode; hence, PVA does not serve as perfect insulator [286]. These results lead to the conclusion that even a thin overlayer of PVA on top of the bilinear array probably could not explain a lower value of P_r. It is emphasized again that the topography analysis performed for the bilinear arrays anyway did not suggest a measurable PVA overlayer. However, the topography could always be analyzed only locally and not globally. Therefore, excluding the impact of a PVA overlayer also from an electrical point of view provides additional verification.

A.2   SI for Chapter 5

A.2.1   Hansen solubility theory

According to Hansen theory [287], a solvent is likely to dissolve a polymer, if the coordinates of the solvent in the three-dimensional Hansen space lie within the solubility sphere of the polymer. In more detail, the Hildebrandt solubility parameter δ is defined as follows:

$$\delta = \sqrt{\delta_D^2 + \delta_P^2 + \delta_H^2}, \tag{A.1}$$

where δ_D, δ_P, and δ_H are the dispersive, the polar, and the hydrogen bonding Hansen solubility parameters, respectively. These three parameters form the axes of the three dimensional Hansen space (see Figure A.3). The position of each solvent in the Hansen space is fixed by its three components. For a polymer, the three components determine the center of a Hansen solubility sphere. The distance between the coordinates of the polymer and a solvent in the Hansen space is given by

$$D = \sqrt{4(\delta_{D1} - \delta_{D2})^2 + (\delta_{P1} - \delta_{P2})^2 + (\delta_{H1} - \delta_{H2})^2}. \tag{A.2}$$

Here, the indices 1 and 2 correspond to the polymer and the solvent, respectively. The radius of the Hansen solubility sphere, R, can then be experimentally determined by including all the solvents that dissolve the polymer (D < R), while excluding those that do not dissolve the polymer (D > R).
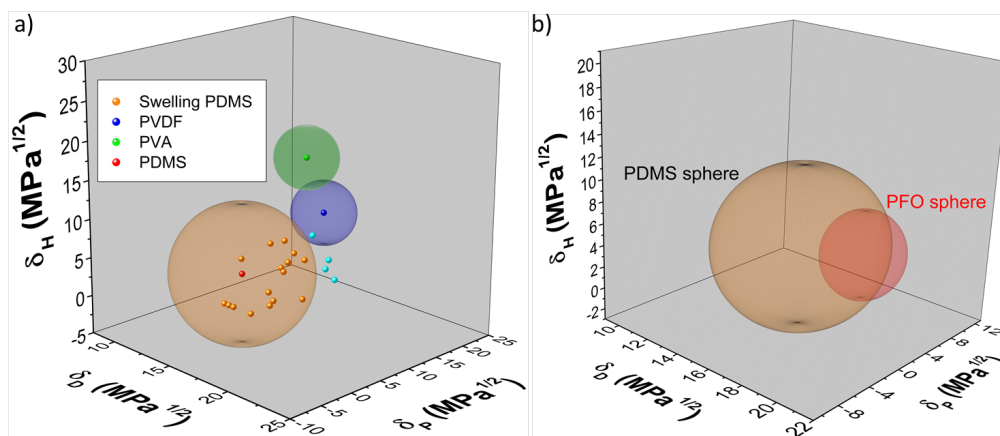
Figure A.3: a) Three dimensional Hansen space with the solubility spheres of PDMS (orange, radius of 8.9), PVDF (blue) and PVA (green). Orange dots correspond to solvents that swell PDMS, while light blue dots belong to solvents that do not swell PDMS. (b) The solubility sphere of PDMS almost completely covers the solubility sphere of PFO meaning that there is no orthogonal solvent for the two polymers. [210]

Duong et al. determined Hansen solubility parameters and the corresponding sphere for different conjugated polymers, among them also PFO [288]. They determined δ_D, δ_P, and δ_H to be 18.55 MPa$^{0.5}$, 2.8 MPa$^{0.5}$, and 4.51 MPa$^{0.5}$, respectively. Furthermore, they found a radius of 4.1 for the Hansen solubility sphere [288]. Using these parameters, the PFO sphere was drawn into the three dimensional Hansen space in Figure A.3b.

In order to compare the solubility properties of PFO and polydimethylsiloxane (PDMS), the solubility sphere of PDMS is needed. Since PDMS is an elastomer, it does not dissolve but swell. Thus, a solubility sphere of PDMS would separate solvents that swell PDMS (inside the sphere) from solvents that do not swell PDMS (outside the sphere). Up to date, a solubility sphere of PDMS has not been published. Lee et al. thoroughly investigated the swelling of PDMS by different solvents, but they only considered the Hildebrandt solubility parameter δ, but not the separate contributions [203].

To that end, the Hansen solubility/swelling sphere for PDMS was determined based on the following experiment. A drop of a certain solvent was placed on a glass substrate, then an unstructured PDMS piece was laid on top. If the stamp deforms within seconds due to swelling, then this solvent is considered 'swelling PDMS'. As a consequence, it should be inside the solubility/swelling sphere. On the other hand, if the PDMS stamp does not deform upon contact with the solvent drop, the solvent is considered 'not-swelling PDMS' and is thus outside the sphere.

Figure A.3a presents the three dimensional Hansen space, where solvents that swell PDMS are shown in orange and non-swelling solvents are indicated in light blue (these are aniline, pyridine, benzaldehyde, acetophenone). The extracted PDMS solubility sphere is shown in transparent orange. The radius is determined to be 8.9. Furthermore, the Hansen solubility spheres of polyvinylidene (PVDF, dark blue) and poly(vinyl alcohol) (PVA, green) were introduced into Figure A.3a using literature data [287]. The spheres of PVDF and PVA only slightly overlap with each other and are completely separated from the PDMS sphere. This explains, why upon solution micromolding of P(VDF-TrFE) and PVA swelling can be ignored, as the comprising solvents are orthogonal to PDMS [183] (cf. Chapter 4).

By contrast, the solubility sphere of PFO (red) in Figure A.3b is almost completely enclosed by the PDMS sphere (orange). In the small region, where the PFO sphere is not enclosed by the PDMS sphere, solvents and solvent mixtures with the corresponding coordinates were tested. However, all the tests either showed solution of PFO but simultaneously also swelling of PDMS or the tests showed lack of swelling of PDMS but also lack of dissolution of PFO. In conclusion, swelling of PDMS during solution micromolding of PFO cannot be avoided by choice of solvents or solvent mixtures.

A.2.2   Patterned diodes with varying pitch width

Memory diodes with varying pitch width of the bilinear array were successfully fabricated. Figure A.4 shows typical *J-V* characteristics for diodes with pitch of 2 µm, 800 nm, 600 nm, and 500 nm. The devices are examples from different substrates. They all show bistable memory behavior.
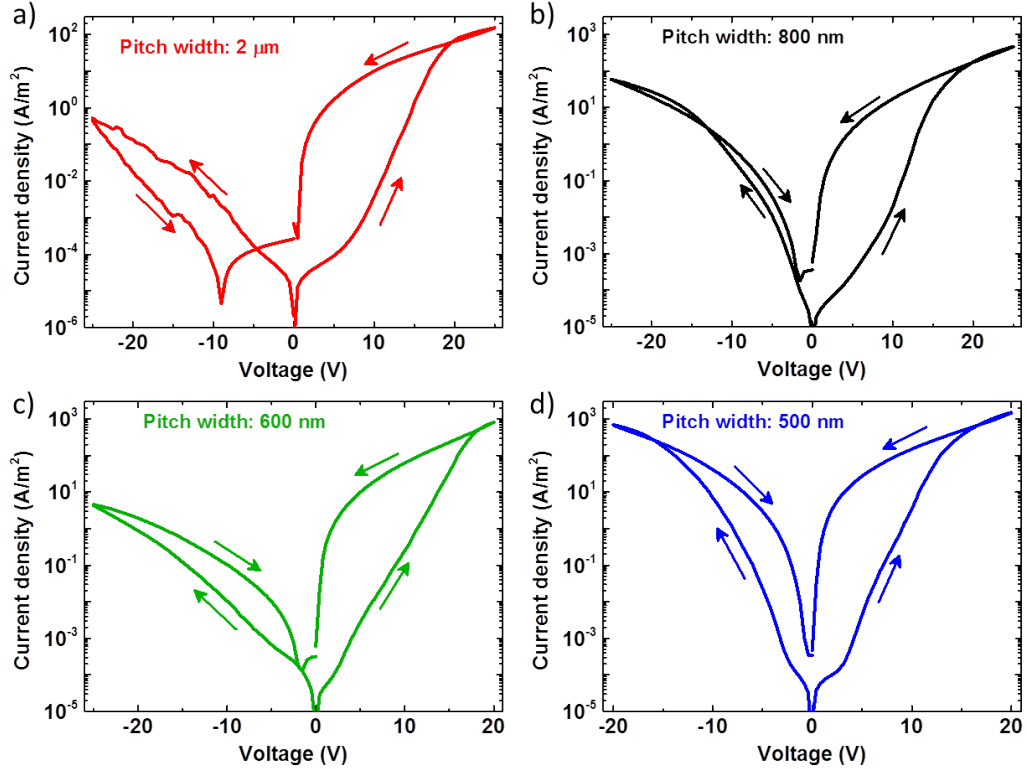
Figure A.4: *J-V* characteristics of memory diodes, where the pitch width of the utilized h-PDMS stamp was a) 2 µm, b) 800 nm, c) 600 nm, and d) 500 nm. In all cases the bias was applied at the Au bottom contact and the PEDOT top contact was grounded.

A.3   SI for Chapter 6

A.3.1   2D grids for the numerical simulations

The numerical simulations were performed on 2D grids. Figure A.5a shows the 2D grid of the patterned memory diode. The protruding PFO slab in the center is flanked by two neighboring P(VDF-TrFE) slabs on the left and on the right. The geometry was derived from AFM analysis. The electrodes are only shown as thin lines at the bottom and the top; they exactly follow the
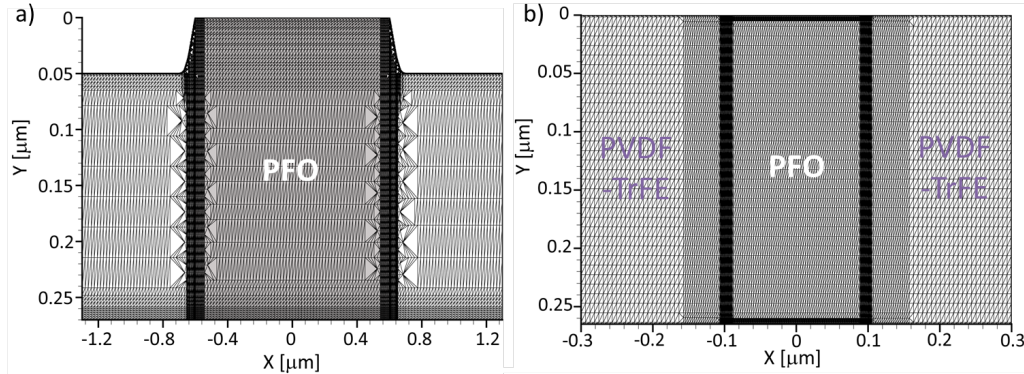
Figure A.5: 2D grids for the numerical simulations of a) the patterned diode and b) the diode comprising a phase separated blend thin film. X is the lateral dimension of the film parallel to the substrate and Y represents the axis perpendicular to the substrate (film thickness).

shape of the geometry. The latter is especially important for the patterned memory diode (Figure A.5a).

After first calculation tests showed that hole accumulation occurs in thin channels at the PFO/P(VDF-TrFE) interface, the fine structure of the grid was adjusted in such a way that the mesh size is very small at the interface. This is indicated by the black stripes in Figure A.5, where the grid is so dense that single mesh points can no longer be distinguished by eye. By contrast, the mesh is less dense in the center of the PFO slab, because this part of the semiconductor is less crucial for the simulation, and thus measurement time can be saved, if the mesh is wider.

In Figure A.5b, the 2D grid for the memory diode comprising the phase separated blend is presented. The random orientation of PFO columns in the P(VDF-TrFE) matrix made it more difficult to come up with a device layout and a grid, which really represent the blend thin film. The grid in Figure A.5b was designed based on the thorough morphology analysis described in the next Section. Again, the grid is denser at the PFO/P(VDF-TrFE) interface.

A.3.2   Morphology analysis for phase separated blend films

In order to determine the area factor for the numerical simulations, AFM measurements were carried out at 6 different positions on the phase-separated blend film (at positions with no electrodes). Figure A.6 shows the recorded AFM height micrographs, where bicontinuous PFO pillars of different diameter are embedded in a matrix of semicrystalline P(VDF-TrFE). For each

micrograph the diameters of all PFO domains were extracted showing an average value of 500 ± 100 nm on an area of 5×5 μm^2.

For the area factor, the length of the PFO/P(VDF-TrFE) interface, which corresponds to the sum circumference of the columns, has to be estimated. An average value of 16.8 μm was found for an area of 25 μm^2. For the entire device area of 0.16 mm^2, this leads to a total interface length of $10.8\times10^4\mu$m. Since the device layout has two interfaces of PFO and P(VDF-TrFE), the area factor is $5.4\times10^4\mu$m. Although the average domain diameter was determined to be about 500 nm, the slab width of the device layout was taken as 200 nm. Since the interface of P(VDF-TrFE) and PFO is crucial for the charge transport and the bulk of each column hardly contributes to the current, this simplification is reasonable. More importantly, the simplification dramatically increases the simulation efficiency.

Investigating blend memory diodes with varying thickness is vital to determine the charge transport physics of the memory diodes. Both space-charge limited current and the saturated current in a transistor show a V^2-dependence. Differentiating between the two is only possible if the thickness-dependence of the current is determined. The numerical simulations predict that the I-V characteristics of ferroelectric memory diodes are similar to
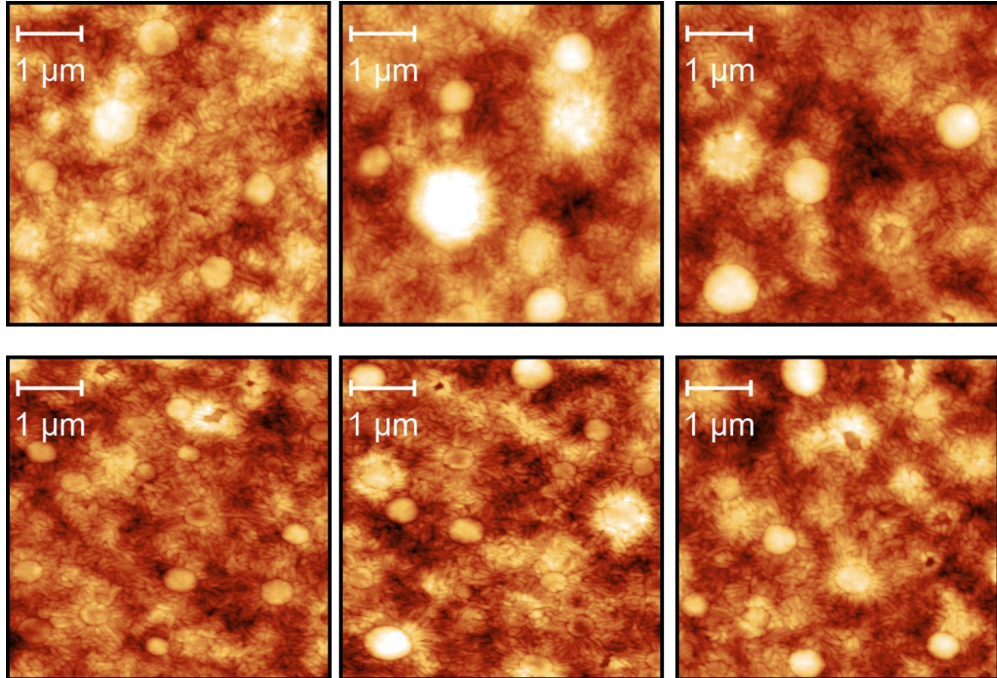
Figure A.6: AFM micrographs at six different positions of the phase separated thin film. The scale bar in each case is 1 μm. The color-coded height scale range was (from top left to bottom right) 80nm, 100 nm, 100nm, 65 nm, 60nm, 75 nm. [233]

Table A.2: Effective PFO/P(VDF-TrFE) interface length for substrates with different thickness. Six measurements were performed on different position of each substrate. The scanned area was always 25 μm^2. The circumference of the bi-continuous PFO domains was determined, and based on that, the interface length for the whole device area (0.16 mm^2) was calculated.

Substrate/Thickness	314±8 nm	399±6 nm	487±4 nm
Interface length	11.0 ± 2.0 μm	6.50 ± 0.6 μm	2.34 ± 0.7 μm

those of a field-effect transistor. Hence, the current at a given voltage is expected to be inversely proportional to the film thickness.

Figure A.7 shows AFM micrographs of blend films with thicknesses ranging between 300 and 500 nm. It is well-known that especially for thick films of phase separated blends, semiconducting domains are more likely to be not bi-continuous [49]. These domains cannot contribute to current transport. In order to be able to compare the different film thicknesses, the effective
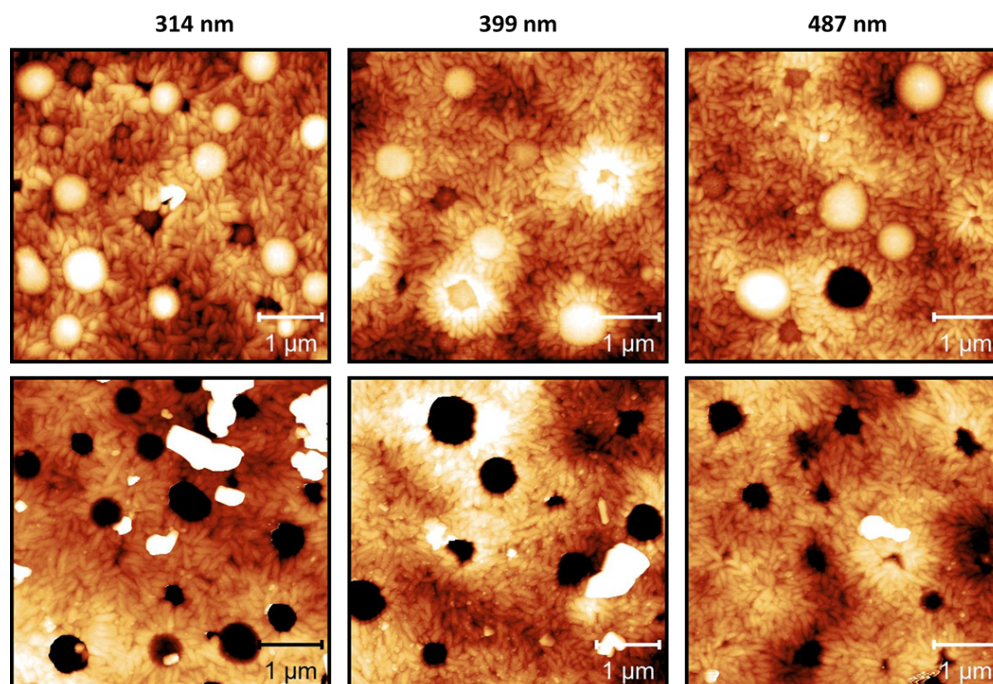
Figure A.7: The first row presents AFM height micrographs before and the second row after selective dissolution of PFO. The measured film thicknesses were 314±8 nm, 399±6 nm, and 487±4 nm. Toluene served as solvent for selective dissolution of PFO. The scale bar for each micrograph is 1 μm. The color-coded height scale range was (from top left to bottom right) 135 nm, 150 nm, 100 nm, 150 nm, 160 nm, 105 nm. [233]

PFO/P(VDF-TrFE) interface has to be determined for each film. This requires that each PFO domain is tested with respect to the question, whether it is bi-continuous or not.

To that end, the substrates with the devices for the thickness scaling analysis were immersed in toluene under vigorous stirring at elevated temperatures (after the full electrical characterization had been carried out). Since toluene is a good solvent for PFO but does not dissolve P(VDF-TrFE), PFO could be selectively dissolved from the blend film. Typical AFM micrographs after selective dissolution are presented in the bottom row of Figure A.7. Measurements were again carried out at six different positions and the diameters of the 'missing' PFO domains were determined, but only those domains were considered, which penetrated the entire film.The resulting statistics, which were used for the thickness scaling analysis, are presented in Table A.2.

A.3.3   Further details on *I-V* measurements

The numerical simulations focus on the positive bias, as only this part of the characteristics is relevant for the analysis of the device physics. For completeness, Figure A.8a shows the entire *I-V* characteristics including the negative bias. Interestingly, the diode is not only bistable but also rectifying.
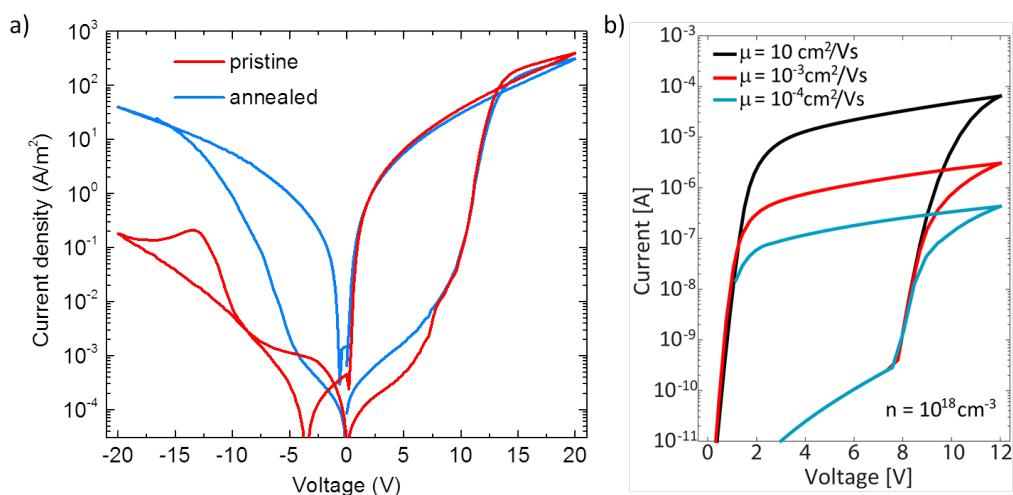
Figure A.8: a) *J-V* characteristics of a phase separated blend memory diode before and after annealing [233]. Changes are specifically observed for negative bias polarity, when the top PEDOT:PSS contact is hole-injecting. b) Calculated *I-V* characteristic for PEDOT:PSS as hole-injection contact (hole-injection from the top, here Au would be grounded). In these simulations, PEDOT:PSS was not treated as metal but as highly doped semiconducting layer that is also discretized and part of the grid. Depending on the mobility defined for PEDOT:PSS, different results for the On-state current are obtained.

For the patterned memory diode, the rectification behavior could be related to the topography; PFO always protrudes, if it is patterned first, and the simulations demonstrated that in the resulting geometry, the stray field at the top contact could be to small to provide sufficient charge injection into the semiconductor. As a consequence, the patterned diode does not switch for negative bias, when PEDOT:PSS is the injecting contact.

The phase separated blend on the other hand hardly shows a pronounced topography. An impact on the injection from the top contact is not expected. This suggests that other aspects of the device cause the rectification behavior. In all device layouts, PEDOT:PSS was considered as electrode, because the polymer indeed exhibits metallic conductivity, when used as thin film. Yet, the PEDOT:PSS thin films on top of the blend were not annealed after spin coating, while PEDOT:PSS films in OLEDs are typically annealed. It was demonstrated in literature that an annealing step can enhance the mobility and thus the conductivity of PEDOT:PSS [289].

Figure A.8a also shows the *I-V* characteristic of the memory diode after annealing. The curve switches for both bias polarities in this case. Hence, low mobility PEDOT:PSS seems to cause poor charge injection, while the situation is significantly improved, if the mobility is enhanced by annealing. In order to corroborate the hypothesis, numerical simulations were performed were PEDOT:PSS was not introduced as metal contact, but as highly doped semiconducting thin film with low mobility. In this case, the hole injection from the PEDOT:PSS top contact is deliberately tested. Therefore, in the simulations, the bottom contact is grounded and positive bias is applied at the top contact. The resulting *I-V* characteristics of the memory diodes for varying mobilities of PEDOT:PSS are presented in Figure A.8. Indeed, if the mobility of PEDOT:PSS is chosen to be very low in the simulations, the On-state current density is significantly decreased.

It is emphasized that data retention of the memory diodes is very good, even if PEDOT:PSS is not annealed. Efficient charge injection requires high mobility, but the compensating charges for the polarized P(VDF-TrFE) can be nicely provided by unannealed PEDOT:PSS. The latter was further confirmed by ferroelectric capacitors, where pristine PEDOT:PSS was used as top contact. They showed excellent retention performance. The fact that PEDOT:PSS can provide rectification in memory diodes is very interesting for applications, since each memory element of a cross-bar array should be rectifying to prevent cross-talk.

Finally, the results above suggest that the rectification behavior observed for the patterned memory diodes is not only due to the topography, but can partly be explained by the low mobility of PEDOT:PSS, which was not annealed after deposition on top of the bilinear array.

The Off-state current of organic ferroelectric memory diodes is expected to be injection-limited. However, injection-limited currents are typically very low. Therefore, it is likely that the measured Off-state current of the experiment is actually a leakage current of the device. In Figure A.9a the current density of a phase separated blend memory diode is plotted versus the applied bias. In order to directly compare the current injected from Au with the current injected from PEDOT:PSS, the latter is here presented as a function of positive bias, although hole-injection from PEDOT:PSS actually occurs at negative bias.

The current density for low bias is equivalent for both cases (Au injecting or PEDOT:PSS injecting) indicating that leakage current is dominating. However, it should be noted that for the very first measurment, the current in the Off-state was always significantly lower. This is demonstrated in Figure A.9b, where the very first measurement of a memory diode is compared with the third measurement. Note that the second measurement was a scan at negative bias to switch off the diode. Interestingly, all positive bias sweeps, which were performed after the first pristine sweep, show the same Off-state current higher than for the pristine measurement. This could be due to charges, which reside in the formed accumulated hole channel due to the stray electric field and the x-component of the ferroelectric polarization.

In order to account for such an effect, the doping density, N_A, was deliberately set to a rather high value of 10^{17} cm^{-3} [290, 291]. With this unintentional doping density, an excellent agreement between experimental values and calculated I-V characteristics could be obtained also at low bias.

The entire I-V characteristic of the phase separated blend diode could
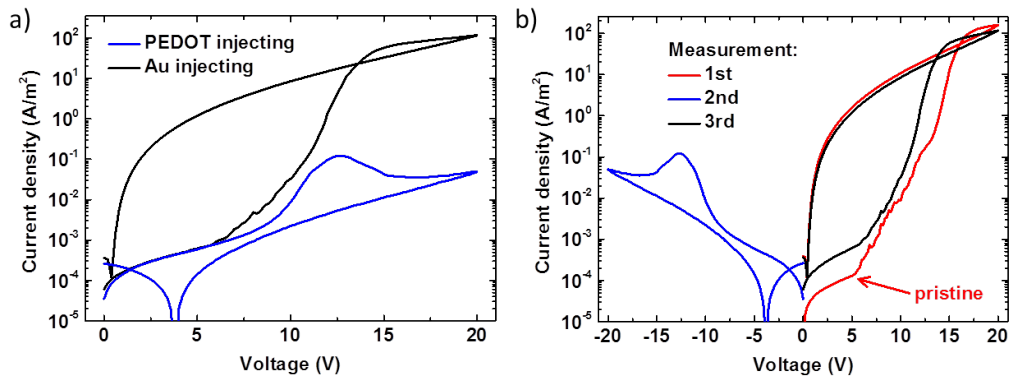
Figure A.9: a) J-V characteristic of a phase separated blend memory diode for different hole-injecting contacts. For comparison, the curve for PEDOT:PSS (normally negative bias) was also plotted for positive bias. b) Comparison of J-V characteristics measured at different points in time [233]. The very first measurement (pristine) shows a lower Off-state current compared to subsequent measurements.

be quantitatively described for positive bias. The internal variables were an-
alyzed at $+20$ V in the main text. In order to demonstrate that the stated
findings also hold for voltages, which are more relevant for practical applica-
tions, Figure A.10a shows the hole density distribution of the phase separated
blend memory diode at $+5$ V. The injected charge carriers are confined at the
ferroelectric-semiconductor interfaces along the whole thickness of the diode.
The two separated 'channels' are also observed at $+5$ V. Figure A.10b is a
zoom of Figure A.10a at the right PFO/P(VDF-TrFE) interface. The charge
concentration at the interface is 5×10^{18} cm^{-3} and thus only a factor of 4
lower compared to the charge carrier density at $+20$ V.

The shape of the hole-density profile in Figure A.10c is also very similar
to the shape at 20 V; only the total number of charge carriers is lower. This
suggests that the confined channel is formed for all bias voltages after the
ferroelectric was polarized, and the actual voltage only determines the total
amount of charges. Finally, Figure A.10d shows the x-polarization compo-
nent, which is still very high for low bias, because it is dominated by the
remanent polarization, which remains, even if the bias is decreased.
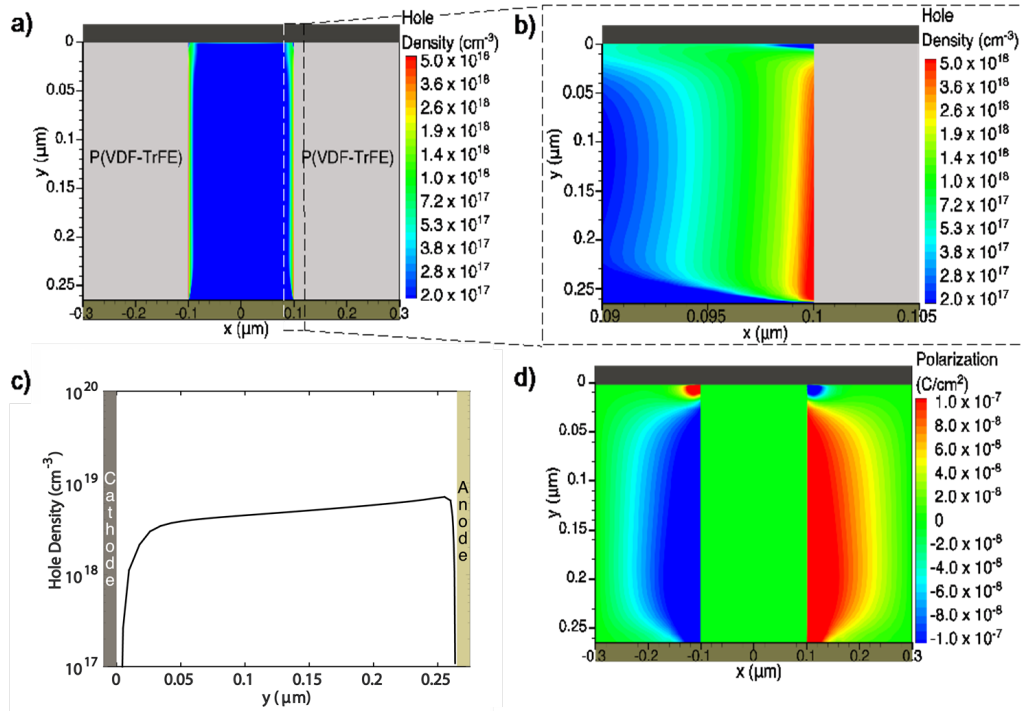
Figure A.10: a) Hole density distribution in the PFO pillar at $V = +5$ V. b) Zoom of
the hole density distribution at the right PFO/P(VDF-TrFE) interface. c) Hole-density at
the PFO/P(VDF-TrFE) interface (cut line at $x = 0.099$ μm), $V = +5$ V. The anode cor-
responds to the injecting contact, while the cathode corresponds to the collecting contact.
d) x-component of the polarization vector at $V = +5$ V. [233]
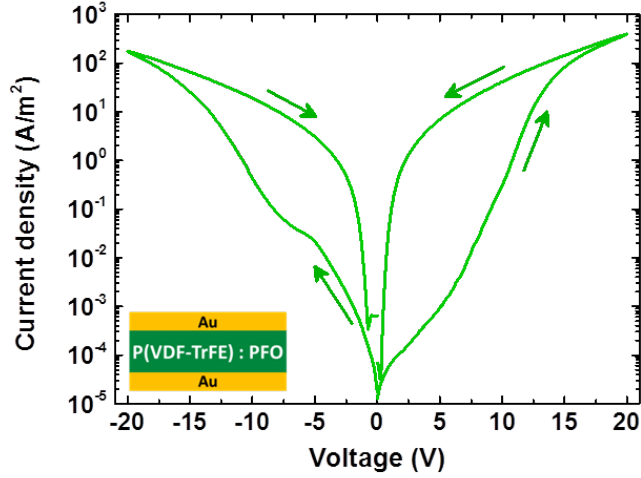
Figure A.11: *J-V* characteristic of an organic ferroelectric memory diode with Au bottom and top contact [259]. The active thin film is a phase separated blend of PFO and P(VDF-TrFE). These diodes were used for the PTC thermistor investigations in Chapter 7.

For the PTC thin film thermistors, Au was chosen not only as bottom, but also as top contact of the diodes comprising phase separated blends. Due to the symmetry of the device, the *J-V* curves in Figure A.11 show switching for both bias polarities. Interestingly, the Off-state current density for negative bias polarity (the top contact is hole-injecting) is higher than the Off-state current at positive bias.

A.3.4 Basics of field-effect transistors

In Chapter 6, the operation of an organic ferroelectric memory diode was compared to that of a transistor. In the following, the basics of a field-effect transistor (FET) are briefly explained.

A FET is a three-terminal device, where the current between the source and drain contacts can be modulated by applying a bias between the gate electrode and the source electrode. Figure A.12a shows a typical device layout. The gate dielectric separates the gate electrode from the semiconducting channel and the source and drain electrodes. If a bias between the source and the gate electrode (gate voltage V_g) is applied, charges accumulate in the semiconducting channel close to the dielectric. The situation can be compared to that of a capacitor. Hence, the accumulated charge can be expressed as

$$Q = C_{diel} \left(V_g - V_{th} \right). \tag{A.3}$$

Here, C_{diel} is the capacitance of the dielectric and V_{th} is the threshold voltage that takes into account that a certain amount of charges is trapped in the semiconductor.

If now additionally a bias between the source and the drain electrodes (source-drain voltage V_{ds}) is applied, then the free charges Q can contribute to the current between source and drain (drain current I_d), which is defined as

$$I_d = \frac{C_{diel}W}{L}\mu_{lin}\left(V_{ds}\left(V_g - V_{th}\right) - \frac{V_{ds}^2}{2}\right), \tag{A.4}$$

where L is the channel length. Equation A.4 holds for low values of V_{ds}. The regime is called the linear regime and μ_{lin} is the corresponding linear field-effect mobility (or mobility in the linear regime).

If the drain voltage significantly exceeds the gate voltage, $V_{ds} > (V_g - V_{th})$, the transistor gets into the saturation regime (μ_{sat}) and the drain current follows

$$I_d = \frac{C_{diel}W}{2L}\mu_{sat}\left(V_g - V_{th}\right)^2. \tag{A.5}$$

The transition between the two regimes is at the pinch-off, which is schematically illustrated in Figure A.12b. The local potential at the pinch-off position is too low to provide sufficient amounts of charge carriers for a high current. Instead, the current is limited by the charge flow across the depletion region; the current saturates.

In the organic ferroelectric memory diode, the origin for the 'pinch-off' is different. It is related to the stray electric field between the polarization charges and the image charges in the top electrode. Nevertheless, the underlying physical relation, $I \propto V^2/l$, is the same as for the FET in saturation at pinch-off, where $I \propto V^2/L$ with L being the channel length (l is device thickness for the memory diode).

For a much more detailed discussion on the operational mechanism of FETs, the reader is referred to excellent reviews in literature [5, 292].
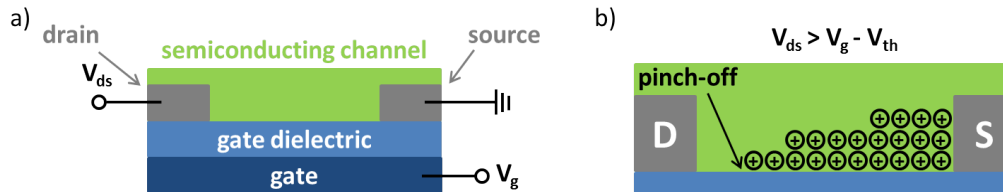
Figure A.12: a) Device schematic of a field-effect transistor. This specific layout is often called bottom gate-bottom contact. It is worth noting that alternative layouts, such as top gate-bottom contact, exist. b) Schematic illustration of the current saturation in the channel at the pinch-off. The picture was adapted from reference [292]

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