A shuttling-based trapped-ion quantum processing node

Dissertation

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vorgelegt von

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Mainz, 31 Oct 2019

Declaration

I hereby declare that this thesis has not been and will not be submitted in whole or in part to another University for the award of any other degree.

Vidyut Kaushal
Mainz, 31 Oct 2019

varnanamarthasamghanam rasanam chandasamapi,
mangalanam ca karttarau vande vanivinayakau.1.

bhavannisankarau vande sraddhavivasaruupinau,
yabhyam vina na pasyanti siddham svantahsthamisvaram.2.

vande bodhamayam nityam gurum sankararuupinam,
yamasrito hi vakropi candrah sarvatra vandyate.3.

sitaramagunagramapunyaranyaviharinau,
vande visuddhavijyänau kavisvarakapisvarau.4.

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-Shri Ramcharitmanas.

Shri Rama Rama Rameti, Rame Rame Manorame, |
Sahasrenama tattulyam, Shri Sita-Ramam Namam Varanane. ||

Shri Sita-Rama Namami

Abstract

Trapped atomic ions in microfabricated segmented ion traps hold the promise of realizing scalable quantum processing nodes. While significant milestones towards noisy intermediate-scale quantum computing (NISQ) have already been demonstrated in the past decade, the realization of platforms allowing for demonstration of e.g. quantum supremacy remains a formidable challenge. Scalability to large number of qubits can be achieved using a combination of trapped-ion qubits that are shuttled inside a segmented ion trap and manipulated in laser interaction zones.

The focus of this thesis is the development of technological key components required for this approach, perform system integration with an existing hardware environment, and to conduct a comprehensive characterization of the system performance. In particular, we discuss the development of a modular based scalable multichannel arbitrary waveform generator (mAWG), which simultaneously updates 80 trap electrodes with programmable voltage waveforms and shapes the duration of 24 laser pulses for entangling gate operations. It has an update rate of 2.7 MSPS for each channel and voltage range of $\pm$40 V with the precision of 1.2 mV. Additionally, the delay between consecutive samples can be controlled in step of 20 ns - important for resolving trap oscillation period during shuttling of ions.

Furthermore, using the mAWG, we present a complete trap-characterization of all motional modes, axial (x) along the trap axis and transverse (y and z) perpendicular to it, for a $^{40}Ca^{+}$ ion, obtaining low heating rates, $\dot{\bar{n}}_{\{x,y,z\}}$={9, 26.6(7), 9.2(3)}, and a long motional coherence times of $\tau_{\{x,y,z\}}$={57(9), 11.6(5), 24(1)} ms.

We also realize various types of elementary qubit register configuration i.e. linear transport, separation and merging of ion crystals, and ion swapping and measure no excitation on the transverse mode induced by these axial shuttling operations, such that two qubit gates with fidelity exceeding 99.5% have been realized. This opens up a path toward NISQ realization. We also show that using this hardware, all type of shuttling operations and even can be executed in parallel at durations of less than 60 µs, thus being well suited for small-scale quantum algorithms. Lastly, we discuss the prospect of scalability in this NISQ platform.

Zusammenfassung

Gefangene atomare Ionen in mikrofabrizierten segmentierten Ionenfallen versprechen die Realisierung skalierbarer Quantenverarbeitungsknoten.Obwohl bereits bedeutende Meilensteine auf dem Gebiet des verrauschten Übergangsgrößen-Quanten-Rechners (NISQ) gezeigt wurden, ist die Realisierung von Plattformen, die den Nachweis der Überlegenheit von Quantenrechnern ermöglichen, nach wie vor eine große Herausforderung. Die Skalierbarkeit hin zu einer großen Anzahl an Qubits lässt sich durch die Verwendung von gefangenen Ionen, die in einer segmentierten Ionenfalle transportiert und in Laserwechselwirkungszonen manipuliert werden können, als Qubits realisieren/verwirklichen.

Die Schwerpunkte dieser Arbeit sind die Entwicklung technologischer Schlüsselkomponenten für diesen Ansatz, die Systemintregration in die existierende Hardwareumgebung und die umfassende Charakterisierung der Systemperformance. Im Besonderen diskutieren wir die Entwicklung eines modularen, skalierbaren, mehrkanaligen Funktionsgenerator mit frei programmierbarer Kurvenform i.e Arbitrary Waveform Generators (mAWG). Dieser aktualisiert gleichzeitig bis zu 80 Fallenelektroden mit programmierbaren Spannungswellenformen und definiert die Form und die Dauer von 24 Laserpulsen für das verschränkende Gatteroperationen. Er hat eine Aktualisierungsrate von 2,7 MSPS für jeden Kanal und einen Spannungsbereich von $\pm$40 V mit einer Genauigkeit von 1,2 mV. Außerdem kann die Verzögerung zwischen aufeinanderfolgenden Abtastwerten in Intervallen von 20 ns gesteuert werden. Dies ist wichtig für die Auflösung der Fallenschwingungsperiode während des Ionentransports.

Zusätzlich stellen wir , unter Verwendung des mAWG, eine vollständige Fallencharakterisierung aller Bewegungsmodi, entlang der Fallenachse (axial) sowie quer und senkrecht (y und z) dazu, eines Ca-Ions vor und quer (y und z) senkrecht dazu, eines $^{40}Ca^{+}$ -Ions vor. Diese ergibt niedrige Heizraten von $\dot{\bar{n}}_{\{x,y,z\}}$ = {9, 26.6 (7), 9.2 (3)} Phononen/s und lange Bewegungskohärenzzeiten von $\tau_{\{x,y,z\}}$ = {57 (9), 11.6 (5), 24 (1)} ms.

Wir realisieren außerdem verschiedene Arten elementarer Qubit-Registerkonfigurationen, wie lineare Transporte, Trennungen und Zusammenführungen von Ionenkristallen und Austausche von Ionen. Wir messen keine, durch diese axialen Operationen verursachte Anregung der Transversalmode, so dass Zwei-Qubit-Gatter mit einer Genauigkeit von über 99,5% erreicht werden. Dies öffnet einen Weg zur Realisierung eines NISQ. Wir zeigen auch, dass mit dieser Hardware alle Arten von Shuttling-Operationen parallel mit Laufzeiten von weniger als 60 µs ausgeführt werden können, was für klein-maßstäbliche Quantenalgorithmen gut geeignet ist. Zuletzt diskutieren wir die Aussicht auf Skalierbarkeit dieser NISQ-Plattform.

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1 Classical and quantum information technology

1.1 Introduction

Digital information technology marks one of the most important technological revolutions throughout the last centuries, impacting almost every aspect of human everyday life and society. The cornerstone its success is the miniaturization of the transistor, which to this day is leading to ever-increasing performance of computer chips. The advancements in this fields roughly follow Moore's law, which predicts the doubling of computing resources every two years. In recent year the miniaturization and performance increase has slowed down, as the reduction in size will ultimately lead to transistors approaching physical limits, where components of the transistor consist of very few atoms and quantum mechanical properties dominate. A different approach to information processing, which makes use of quantum mechanical properties and is not limited but rather makes use of the limitations, is known as quantum information processing.

The idea of doing computations according to the laws of quantum physics was first introduced by Yuri Manin [Man80] and Paul Benioff [Ben80]. Later, Richard Feynman came up with the idea of the universal quantum simulator [Fey82], using quantum computers [Fey86] to understand physical systems which can not be computed using numerical simulations on classical computers or analytic calculations. Ideas for a practical implementation of a quantum computer were pioneered by Cirac and Zoller, proposing trapped ions as a fundamental building block [CZ95], and the subsequent demonstration of quantum CNOT gates [Mon+95a], [Sch+03] has led to a rapid evolution of experiments based on trapped ions.

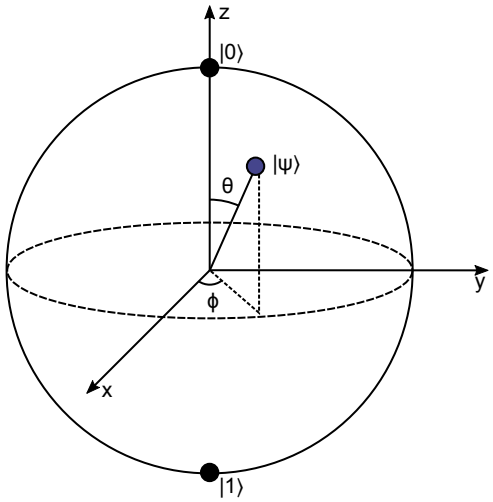


Fig. 1.1 Geometrical representation of a qubit, on the Bloch sphere. It is used for representing qubit state in 3-D space.

The most prominent challenge of realizing a useful quantum computer lies in scaling, i.e., establishing devices operating a sufficient number of quantum bits (qubits). Kielpinski et al. proposed the idea of a scalable trapped ion quantum computer: the quantum charge-coupled device (QCCD) architecture [KMW02] consisting of many interconnected ion traps, realized by segmented linear Paul traps.

In this thesis, a scalable trapped ion quantum computing node using a segmented ion trap is discussed, which allows for the high fidelity operation of registers comprised of ~10-15 qubits.

Classical digital computing and quantum computing

The fundamental unit of classical information technology is the bit, with possible values of **true**(1: digital high) and **false** (0: digital low). It is the basis of all classical operations, as data and algorithms are broken into binary format before execution on the classical processor. Transistors are used to realize binary logical gates, which are the building blocks of computer processors. In the quantum regime, classical bits are replaced by quantum bits, which are non-boolean in nature and the idea of binary values are extended to quantum state levels of $|0\rangle$ and $|1\rangle$ and the possibility of intermediate values as well. The intermediate values are a combination of both possibilities, generally known as superposition states. The computational gates are realized according to the laws of quantum physics and hence referred to as quantum gates.

1.1.1 Qubits and quantum gates

A quantum bit, qubit in state $|\psi\rangle$ is a linear combination (superposition) of the logical basis states $|0\rangle$ and $|1\rangle$: $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$, where α and β are complex numbers such that square of their modulus ($|\alpha|^2$ or $|\beta|^2$) represents the probability of the qubit being found in that state upon measurement. The probabilities are normalized, i.e. $|\alpha|^2 + |\beta|^2 = 1$. The geometrical representation of qubit states is given by the Bloch sphere (see Fig. 1.1), where logical basis states $|0\rangle$ and $|1\rangle$ are represented by the poles and a pure qubit state vector is determined by a point on the sphere surface. Therefore, it is uniquely determined by polar and azimuth angles: $|\psi\rangle = \cos(\theta/2)\,|0\rangle + e^{i\phi}\sin(\theta/2)\,|1\rangle$ [NC11].

Quantum gates are represented by unitary transforms acting on qubit states. Similar to any classical digital logic being constructed by NAND gates, any quantum logic can be constructed from CNOT gates and single qubit rotations. Using these gates, several quantum algorithms have already been proposed theoretically, while several have been demonstrated experimentally. Currently, several research groups around the globe are working on different physical platforms to realize the goal of a useful quantum computer [Deb+16; Mon+16].

1.1.2 Quantum algorithms and physical platforms

Algorithms are designed based on the encoding of information. It has been proven that certain quantum algorithms could substantially outperform the most efficient classical computing solution. For example, Shor's algorithm [Sho97] can be used to find prime factors of an integer number in polynomial time, and Grover's search algorithm [Gro97] outperforms classical algorithms for unstructured database search. These algorithms have been experimentally demonstrated on small quantum processors [Mon+16; Fig+17].

A review of several quantum algorithms can be found in [Mon16]. There are several quantum mechanical systems under investigation as qubit candidates [Win+03; CW08; Ima03; Niz+05; LL01; KLM01]. However, with trapped ions, all fundamental condition [DiV00] for building a quantum computer have been demonstrated successfully [Sch+03; Mon+11] and have also proven as one of the most suitable platforms for large-scale quantum computation [Mon+16; Deb+16].

Shuttling-based quantum processor

In charge coupled devices (CCD), charges containing the information(1 or 0) are moved inside the device for processing. Similarly, in a QCCD, qubits carrying the quantum information

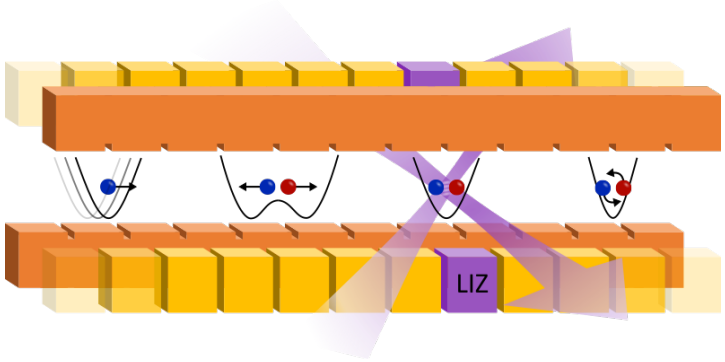


Fig. 1.2 Illustration of a 3-D segmented ion trap and possible movement (shuttling) of trapped ions inside it. The left most operation is transport operation of single ion (or multi-ion crystal) which moves it along trapping axis, the next operation is separation of two-ion crystal into individual ions. Blue segment (Laser Interaction Zone, LIZ) is the processing zone where interaction of ion(s) with lasers take place for quantum information processing. The right most, depicts the swap operation which is performed by physical rotation of an ionic crystal.

are moved (shuttled) within memory and processing regions of a segmented ion trap. As in a classical CCD, the charged information carriers move due to the temporal variation of electrode voltages, in QCCD architecture also charged ions are moved with time varying voltages on electrode leading to movement (shuttling) of atomic-ion inside this. The shuttling operations fall into three categories: transport of ions, separation, and merging of ions and rotation of multi-ion crystals. A cartoon visualizing these operations are shown in Fig. 1.2.

1.2 Structure of this work

As part of my thesis, fundamental technological and methodological building blocks of a trapped-ion quantum computer are demonstrated. The thesis is structured as follows: Chapter. 2 provides an introduction to theoretical frameworks and experimental platforms that have been used for the measurements and analysis of the recorded data. Chapter. 3, discusses the improvements made to the experimental setup as part of this work. Chapter. 4 presents a scalable trap control system developed within the course of this thesis. The Chapter. 5 demonstrates and characterizes several shuttling operations. Finally, Chapter. 6 presents the summary of the results achieved and discusses future experiments. Significant technological developments made during my thesis are presented in the Appendices.

2

Qubit operations

In this chapter, a short discussion on the realization and manipulation of qubits based on trapped ions is presented. The theoretical details given in this chapter provide a basic introduction of the experimental setup and methods used, which have already been covered in previous works from our group [Pos09; Kau18; Rus18]. The material presented here is intended to make this thesis self-contained.

The discussion begins with a basic introduction to ion-trapping principles (see Sec. 2.1). This is followed by the introduction of microfabricated segmented linear ion traps, which has been used in this thesis (see Sec. 2.2). Then, the coherent control and manipulation methods of qubit (see Sec. 2.3) using advance experimental control systems are explained.

2.1 Paul trap

Charged particles cannot be confined in three spatial dimensions by only application of static electric fields [Ear42] only. Therefore, Penning or Paul traps offer solutions by application of a magnetic field [Pen36] or time-varying electric fields [Pau90], respectively. As a Paul trap is employed in this work, a brief discussion on its operational principle is presented here.

Paul traps generate electric quadrupole potentials, which can generally be written as:

$$U = U_{(0)}(\alpha x^2 + \beta y^2 + \gamma z^2), \tag{2.1}$$

Where $U_{(0)}$ is given by the trap geometry and the applied voltages, and {x, y, z} are the spatial coordinates. The potential has to obey the Laplace equation: ΔU=0, therefore

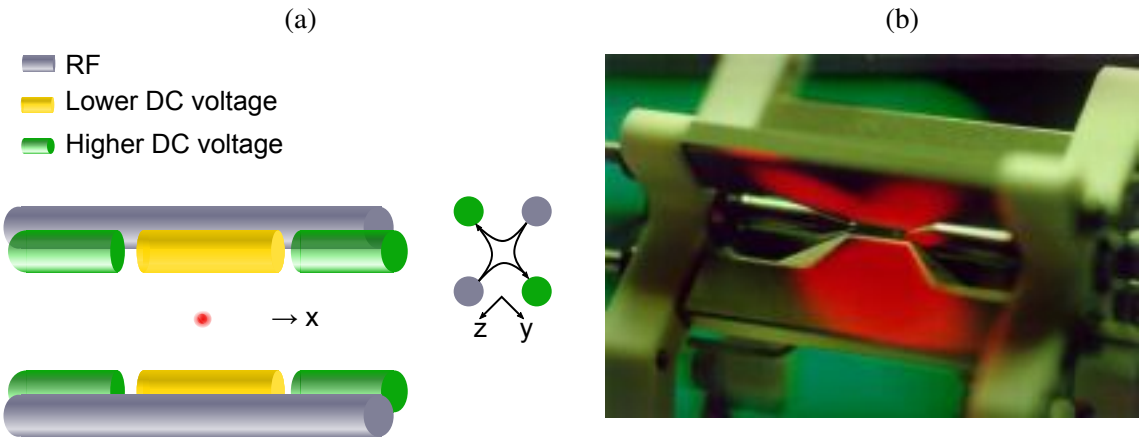


Fig. 2.1 Linear Paul-traps. **(a)** Schematic of a linear trap, in which a radio frequency (RF) voltages are applied to the (grey) electrodes (top and bottom), resulting in an oscillatory quadrupole potential in y-z direction (see side view). Segmented electrodes (golden and green) provide axial confinement. The lower and higher voltage on center and side electrodes give rise to a potential minima in axial direction x. When axial confinement is smaller than the radial (y, z) confinements, linear ion crystals aligned along the x axis can be trapped. **(b)** The Innsbruck's linear Paul trap that can trap the ions chain of $^{40}Ca^{+}$ for several days [Sch+03].

$\alpha+\beta+\gamma=0.$
We consider the following types.

1. α=-2, $\beta=\gamma=+1$
   confinement along x, anti-confinement in the $y-z$ plane.

2. $\alpha=-1, \beta=-1, \gamma=+2$
   confinement along x and y, anti-confinement along z.

3. $\alpha=0, \beta=-1, \gamma=+1$
   no potential along x, confinement along y, anti-confinement along z.

These potentials correspond to commonly used trap geometries. It can be seen that, by using only electrostatic potentials, no configuration can serve to provide confinement along all directions. We employ a linear segmented trap, in which a static (dc) potential of type 2 provides purely electrostatic confinement along the trap axis (the direction along the segments) and static anti-confinement along one of the transverse directions. The latter is compensated for by an oscillatory (RF) potential of type 3, which provides ponderomotive confinement along both transverse directions.

The mechanism underlying ponderomotive confinement can be easily understood by considering a free charged particle of mass m and charge Ze, in a homogeneous electric field of amplitude E_0, oscillating at frequency Ω. This particle will undergo oscillations at velocity amplitude $v_0 = \frac{Ze\,E_0}{m\Omega}$, leading to a cycle-averaged kinetic energy $E_{pond} = \frac{Z^2e^2E_0^2}{4m\Omega^2}$. If the oscillation period $2\pi/\Omega$ is the shortest timescale, the driven oscillation can be seen as an effective degree of freedom carrying energy, i.e., a pseudo-potential. Now, for an inhomogeneous oscillatory field, we obtain a ponderomotive force driving the particle towards the minimum electric field amplitude:

$$F_{pond} = -\nabla E_{pond} = -\frac{Z^2e^2}{4m\Omega^2}\nabla(E_0^2). \tag{2.2}$$

The total electrical potential around the trap center $\vec{r} = 0$ reads

$$U(\vec{r}) = U_{dc}(\vec{r}) + U_{RF}(\vec{r})cos(\Omega t), \tag{2.3}$$

where U_{dc} is of type 2 and U_{RF} is of type 3. In the transverse $y-z$ plane, this gives rise to the equations of motion

$$m\ddot{y} = \left(-Ze\,U_{dc}^{(0)} - \frac{Z^2e^2}{4m\Omega^2}U_{RF}^{(0)}cos(\Omega t)\right)y \tag{2.4}$$

$$m\ddot{z} = \left(+2Ze\,U_{dc}^{(0)} - \frac{Z^2e^2}{4m\Omega^2}U_{RF}^{(0)}cos(\Omega t)\right)z. \tag{2.5}$$

Substituting the dimensionless parameters τ=$\Omega t/2$, $a = \frac{4Z^2e^2\,U_{dc}^{(0)}}{m\Omega}$, $q = \frac{2Z^2e^2U_{RF}^{(0)}}{m\Omega}$ results in the Mathieu equations

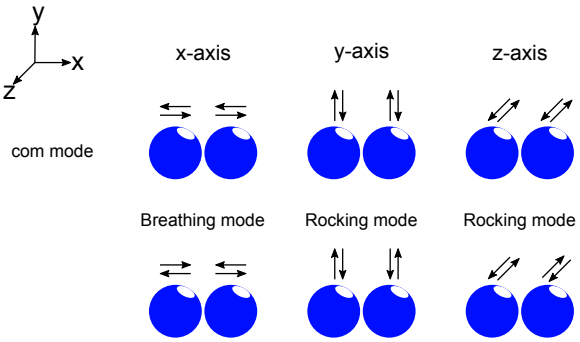
$$\frac{d^2y}{d\tau^2} + (a_y + 2q_y \cdot cos\tau)y = 0 \tag{2.6}$$

$$\frac{d^2z}{d\tau^2} + (a_z - 2q_z \cdot cos\tau)z = 0. \tag{2.7}$$

The solution of Mathieu equation corresponds to a given transverse direction $i = \{y,z\}$ consists of superimposed motion at two distinct frequencies, the slowly varying secular motion (ω_i) and the fast micro-motion with frequency Ω. For stable confinement, a and q parameters have to be chosen inside a stability region [Pau90; Lei+03a].

Ion crystal

(a) Normal modes of vibration in a two-ion crystal



(b) A trapped ion and ionic crystals in a segmented ion-trap

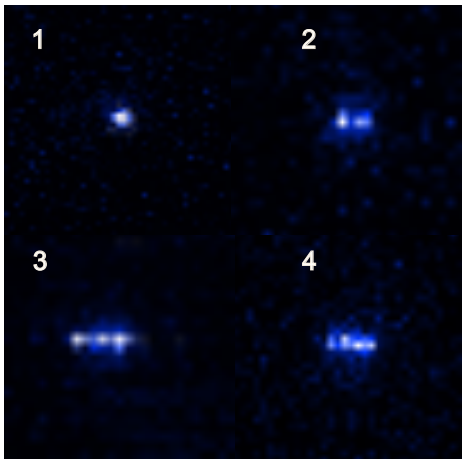


Fig. 2.2 Different vibration modes of two-ion crystal and camera image of trapped single ion and multi-ion crystal. **(a)** Schematic of all six normal (axial (com, breathing), higher-lower frequency transverse (com, rock)) modes of vibration in a two-ion crystal. **(b)** The figures (1, 2, 3 and 4) show camera images of ion and crystals with respective number of ions. All the images have been taken separately at different time-stamps by an EMCCD camera[5].

Clouds of trapped ions, when cooled, can arrange as an ordered structure, i.e., a Coulomb crystal [Blü+88]. If the radial confinement is stronger than the axial confinement, the ion crystal can assume the shape of a linear chain. For increasing size of the crystal, the Coulomb repulsion between the ions can drive the ion crystal through a structural phase transition towards a zigzag structure. The potential energy of a harmonically confined N-ion crystal is given by [Jam98; MSJ03],

$$V = \frac{M}{2}\sum_{n=1}^{N}\sum_{i=\{x,y,z\}}^{3D}\omega_i^2 x_{n_i}^2 + \frac{Z^2e^2}{8\pi\varepsilon_o}\sum_{\substack{m\neq n\\ n,m=1}}^{N}\left[\sum_{i=\{x,y,z\}}^{3D}(x_{n_i}-x_{m_i})^2\right]^{-1/2}, \tag{2.8}$$

Where x_n is the position of nth ion in the ionic crystal, M is the ion mass, and $\omega_{x,y,z}$ are the secular frequencies pertaining to the different directions.

Introducing dimensionless coordinates $u_m = x_m/l$, where $l = \left[Q^2/4\pi\varepsilon_0 M\omega_x^2\right]^{1/3}$, solving for equilibrium positions according to $\dfrac{\partial V}{\partial x} = 0$ yields

$$U_n - \sum_{n=1}^{m-1} \left(U_m - U_n \right)^{-2} + \sum_{n=m+1}^{N} \left(U_m - U_n \right)^{-2} = 0. \tag{2.9}$$

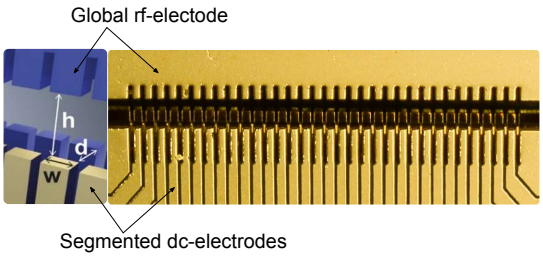
This system of coupled equations can be solved analytically for up to 3 ions, for larger crystals numerical solution is required. Assuming a small displacement from the equilibrium position in a given trap ($x_m(t) = x_0 + C_m(t)$) and expanding Eq. 2.8 to second order around the equilibrium positions, we obtain,

$$V \approx \sum_{n,m=1}^{N} q_n q_m \left[\frac{\partial^2 V}{\partial x_m \partial x_n} \right]_0 = \sum_{n,m=1}^{N} C_{nm} q_n q_m. \tag{2.10}$$

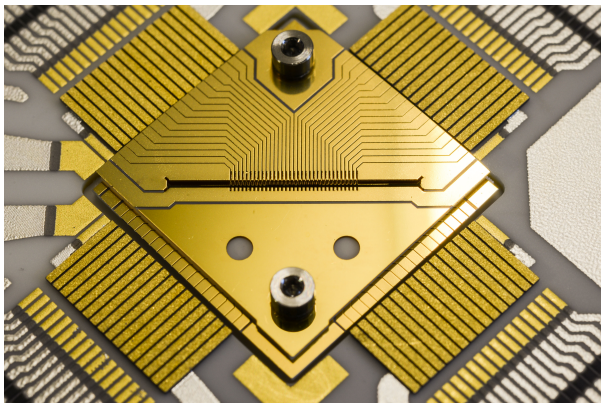
Diagonalization of the real and symmetric $3N \times 3N$ matrix C_{nm} yields a set of $3N$ uncoupled harmonic oscillators, corresponding to collective normal modes of oscillation. The frequencies are given by the eigenvalues obtained μ_n^i, and read as $\omega_n^i = \sqrt{\mu_n^i}$ [Jam98; MSJ03].

For typical operation parameters and atomic ions typically used in experiments, the inter-ion distance of few μm range and secular frequencies of few-MHz range are obtained.

2.2 Segmented ion trap



(a) 3-D illustration of segmented ion-trap



(b) Microfabricated segmented ion-trap in Mainz

Fig. 2.3 Micro-fabricated segmented linear Paul-trap **(a)** 3-D view of segmented ion-trap, the independently controllable segmented dc-electrodes and a global RF-electrode are shown, the dimension w=150 µm(electrode width), h=384 µm (slit width) and d=254 µm (spacing-width). **(b)** Shows the top view of trap and its PCB with electrode wiring and holes. The holes are used for mounting this trap in ultra-high vacuum chamber [Kau18].

For the work presented in this thesis, a micro-fabricated linear segmented multi-layer trap with uniform geometry was used. This trap consists of two gold-coated alumina chips, separated by an insulating spacer layer. Each of the chips contains the trap slit and equally spaced electrodes acting as dc-segments on one side, while the other side of the slit form global RF-electrode (see Fig. 2.3).

The picture of the micro-fabricated segmented ion trap, which is used for the measurement is shown in Fig. 2.3. The spacing between two adjacent dc-electrodes is 50 µm, and the electrode width is w=150 µm, the distance between the two electrode-bearing chips is d=254 µm, while the slit is h=384 µm wide and 12.84 mm long. The ions are moved along the direction of the slit, which is referred to as the trap-axis. The trap-chip is square shaped with outer dimensions of 15 $\times$ 15 mm. It was improved and assembled by Henning Kaufmann and Christian Schmiegelow. A detailed description can be found in [Kau18].

2.3 The $^{40}Ca^{+}$ spin qubit

The Zeeman sublevels of the $4^2S_{1/2}$ ground state of $^{40}Ca^{+}$ are used to encode our Qubit. The qubit states $|0\rangle$ and $|1\rangle$ thus correspond to the alignment of the spin of the valence electron in an external magnetic field (Fig. 2.4). The coherence time of the qubit depends upon the stability of the magnetic field used for generating the Zeeman splitting between the sublevels. The qubit states are separated by about $2\pi\times10.5$ MHz, corresponding to a magnetic field of 0.37 mT, generated by Sm_2Co_{17} permanent magnets. Permanent magnets in combination with a μ-metal magnetic field shielding box were used to demonstrate a long spin-echo coherence time of 2.1(1) s [Rus+16] in this setup. Qubit rotations are driven on a stimulated Raman transition near 397 nm, i.e., via the $4^2S_{1/2} \leftrightarrow 4^2P_{1/2}$ electric dipole transition.

2.3.1 Optical control

The optical transitions and laser sources for manipulation of the $^{40}Ca^{+}$ spin qubit [Pos+09] are discussed below. The relevant energy levels and transitions are shown in Fig. 2.4. The alignment of the different laser beams with respect to the trap axis and magnetic field is shown in Fig. 2.5.

Photoionization

Calcium vapor produced by an atomic oven guided towards the ion trap and two-photon ionization [Gul+01] using two diode lasers near 423 nm and 375 nm generate $^{40}Ca^{+}$ ions in

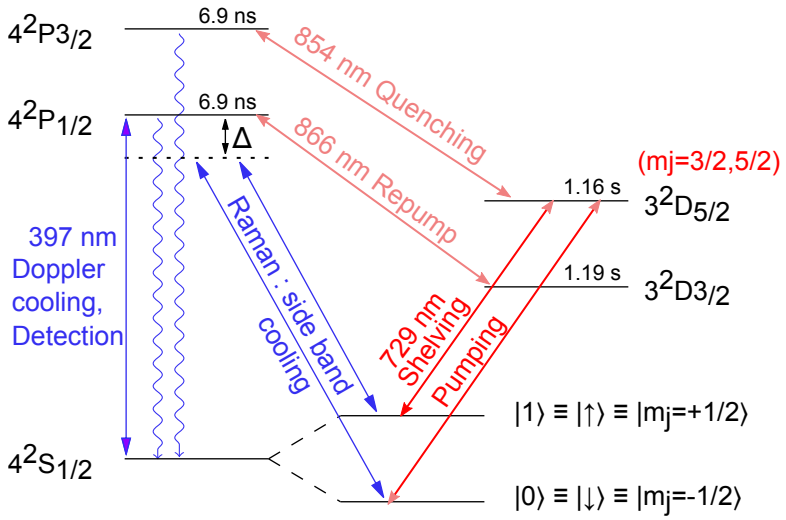


Fig. 2.4 The energy level scheme of $^{40}Ca^{+}$ and all relevant transitions. Five laser sources (866 nm, 854 nm, 729 nm, 397 nm (Doppler) and 397 nm (Raman)) are needed for qubit initialization and state manipulations as well. A magnetic field of 0.37 mT is used for Zeeman splitting ($|\downarrow\rangle$ and $|\uparrow\rangle$), $\Delta_z/2\pi$=10.5 MHz.

the trap. The 423 nm laser frequency is monitored and frequency locked using a wavemeter[1], while the 375 nm is driving a transition to the continuum and does therefore not require any locking. Both beams are coupled into a single-mode fiber and guided to the trap.

Doppler cooling

Doppler cooling of ions is required to localize the ions inside the trapping volume. A 397 nm single-mode laser is employed for Doppler cooling on the $4^2P_{1/2} \leftrightarrow 4^2S_{1/2}$, cyclic transition. The short-lived $4^2P_{1/2}$ state ensures high scattering rates, enables fast and efficient cooling and detection of resonance fluorescence. The trapped ions move in closed orbits inside the trap. Therefore, a single beam is sufficient to cool ions along all spatial directions [IW82; Win+87]. The cooling beam is directed at an oblique angle (45°) with respect to the trap axis and therefore has components along all principal axes of the trap. The mean thermal phonon numbers after Doppler cooling are measured to be $\bar{n}_{x,y,z}$={16, 5, 4} along for the x,y,z secular modes at frequencies $\omega_{x,y,z}/2\pi = \{1.5, 3.8, 4.6\}$ MHz, respectively.

Repumping and quenching

A single mode diode laser near 866 nm is employed to repump trapped population from metastable $3^2D_{3/2}$ state to the $4^2P_{1/2}$ state throughout driving the cyclic transition. A similar

[1] Wavelength Meter WSU 6

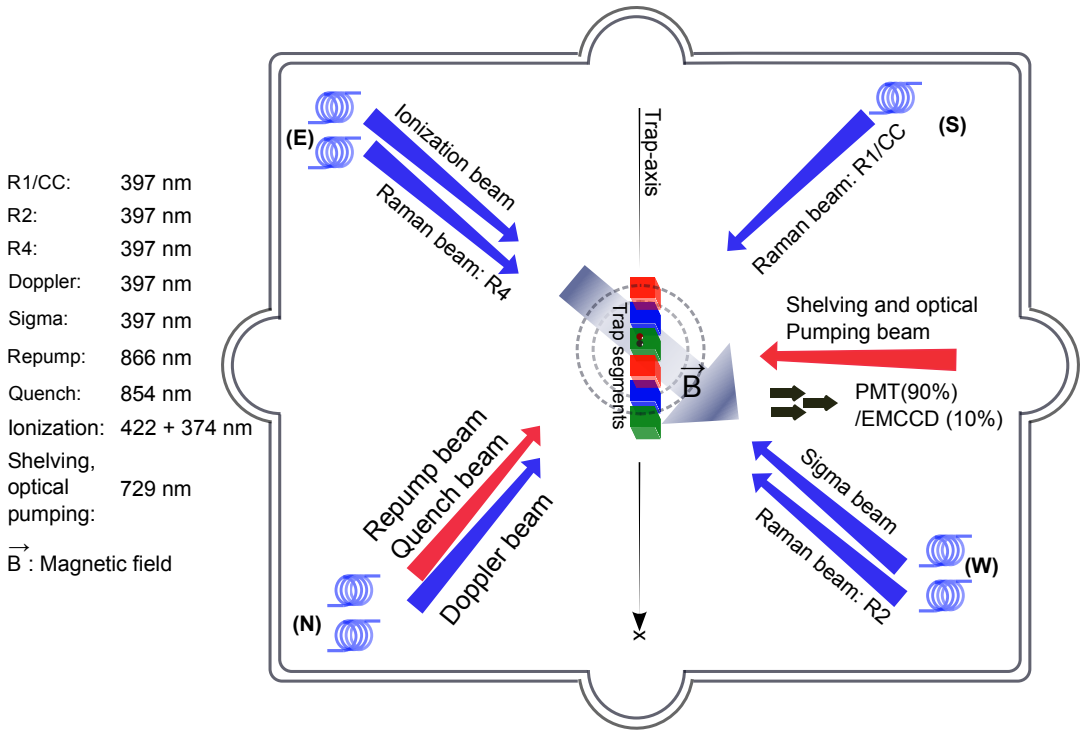


Fig. 2.5 Top view of the laser beams alignment with respect to trap axis. **(E)** The ionization beams (423 nm and 374 nm) and transverse Raman beam (R4) are pointing to LIZ from same direction, i.e in direction of $\vec{B}$. **(N)** Repump (866 nm), Quench (854 nm) and Doppler beam (397 nm) are pointing to ion at 90° with $\vec{B}$ (45° with trap-axis). **(W)** Sigma-beam (397 nm) and Raman-R2 are pointing to ion at 180° with $\vec{B}$. **(S)** Beam R1 and CC are pointing from 90° at LIZ. And IR beam 729 nm is pointing at angle of 45° with $\vec{B}$ for driving quadrupole ($\Delta m=\pm 2$) transition. The Raman beams (R1/CC, R2 and R4) are derived from the same laser source. The effective $\vec{k}$ points along trap-axis for R1/R2 beam , while for R1/R4 points toward transverse directions, direction $\perp$ to trap-axis. More information about the chosen geometrical alignment have been discussed in text.

laser near 854 nm is employed for depleting the metastable $3^2D_{5/2}$, i.e., for resetting the qubit after readout. Two AOMs in double pass configuration are used to control these lasers.

Qubit initialization, shelving and readout

The qubits need to be initialized to a well-defined state for quantum information processing. For our measurements, the qubits ate initialized in $|\uparrow\rangle$. To that end, we drive a narrow electrical quadrupole transition near 729 nm, to selectively transfer the population of $|\downarrow\rangle$ to a Zeeman sublevels of the $3^2D_{5/2}$ state, which is then transferred back to the ground state via quench laser near 854 nm. This is repeated until the population is transferred to $|\uparrow\rangle$ state. A state preparation efficiency of >99% can be achieved in this method [Pos+09]. Alternatively, qubit initialization

can be carried out by employing a circularly polarized beam driving the cycling transition. The spin state of the ions ($|\uparrow\rangle$ or $|\downarrow\rangle$) are read out at the end of each measurement sequence. This is done by using frequency selective, robust population transfer on the electric quadrupole near 729 nm via rapid adiabatic passage [Pos+09]. Here, we efficiently transfer the population from $|\uparrow\rangle$ to the sub-levels (m_j=5/2,-3/2) of the $3^2D_{5/2}$ state, followed by detection of resonance fluorescence upon driving the cycling transition. If the spin state has been $|\downarrow\rangle$, the ion is detected as bright. Otherwise, no fluorescence is detected.

Stimulated Raman transitions

Qubit manipulations are carried out using stimulated Raman transitions. Here, two laser beams detuned from the cycling transitions act together to realize coherent coupling between the qubit states. If the detuning from the dipole transition is much larger than the natural line-width, an effective two-level system is realized. The effective Rabi frequency is given by the product of the dipolar Rabi frequencies, divided by the detuning from resonance. Effective detuning is the difference of laser beam frequency differences and the Zeeman splitting. The effective wavevector k_{eff}, in turn is determined by the wavevector difference of the two beams. If the effective wavevector has a component along an oscillation direction of a given secular mode, coherent coupling to this mode is realized as well. A set of four beams termed R1, CC, R2, and R4 are derived from the single laser source(397 nm) (see Fig. 2.5). The beams are individually controlled using single pass AOMs and individually delivered to the trap via single-mode fibers [Kau18]. Different pairs of beams are used for different purposes:

- **R1/CC:** These are the co-propagating beams with k_{eff} close to zero. Therefore, the coherent coupling is insensitive to the ion motion. With the effective detuning matching the Zeeman splitting, resonant single-qubit rotations can be driven at high fidelity.
- **R1/R2:** k_{eff} is aligned along the trap axis, therefore the coupling is sensitive to ion motion along this direction. This beam pair is used for resolved sideband cooling and probing motional states of axial vibration. Lamb-Dicke parameters of about 0.21 are obtained at an axial secular frequency of $2\pi\times1.5$ MHz.
- **R1/R4:** k_{eff} is aligned orthogonal to the trap axis, therefore the coupling is sensitive to ion motion along the transverse directions. This beam pair is used for resolved sideband cooling and probing motional states of radial modes of vibration. Lamb-Dicke parameters between 0.07 and 0.11 are obtained for radial secular frequencies between $2\pi\times3.0$ MHz and $2\pi\times5.0$ MHz.

- **CC/R4:** This beam pair gives rise to optical dipole forces along the radial direction. It is used for driving entangling gate operations mediated by radial modes [Kau18].

Resolved sideband cooling

High fidelity entangling quantum gate operations generally require the ion motion to be within the Lamb-Dicke regime, i.e. the extent of the ion motion has to be much smaller than the wavelength of the radiation driving the gates [Bal14]. For typical parameters, this requies phonon numbers $\bar{n} \lesssim 1$. Doppler cooling being the first stage yields phonon numbers around $\bar{n} \approx 10$. Then, resolved side-band Raman cooling [Mon+95b] is used for cooling the ion close to the motional ground state. For an ion initially in state $|\uparrow, n\rangle$, a π pulse on the 1^{st} red-side band (rsb) is applied, which probabilistically removes a vibrational quantum upon a spin flip, resulting in the state $|\downarrow, n-1\rangle$. An optical pumping pulse driving the cycling transition serves to reset the spin, such that the state $|\uparrow, n-1\rangle$ is obtained. This sequence is repeated until the mean phonon number is sufficiently low. For multi-mode cooling of the radial motion and/or two-ion crystals, a sequence of blocks of 5 to 100 pulses on the second or first motional sideband of the relevant modes is employed.

Characterization of motional states

In order to verify and optimize shuttling operations, advanced and tailored measurement schemes for characterizing the state of a given motional mode of a single ion or ion crystal are required. A well-established method consists of recording Rabi flops on a coherently driven transition between long-lived internal states of the ions, which features a suitable coupling to the motional mode(s) of interest. In our case, we utilize stimulated Raman transition between $|\uparrow\rangle$ and $|\downarrow\rangle$, driven by laser beam pairs which are directed such that the effective wavevector points along the axial direction or along the transverse directions. The resulting Lamb-Dicke factors characterizing the coupling to the motion range between about 0.05 for lower-frequency transverse center-of-mass mode of a two-ion crystal, up to about 0.21 for the axial vibration of a single ion. The shuttling operations predominantly cause coherent oscillatory motion, therefore one is not interested in full quantum state reconstruction [Mee+96; Lei+03b], but rather in obtaining the mean phonon number $\bar{n}_{\mathrm{coh}} = |\alpha|^2$ pertaining to the displacement parameter α. Resonantly driving Rabi flops on a sideband transition where a π (spin)flip is accompanied by a change of δn phonon, starting with a single ion in $|\downarrow\rangle$, the probability to find the ion in $|\uparrow\rangle$ after exposure time t is given by

$$P_{|\uparrow\rangle}^{(\delta n)}(t) = \sum_{n=0}^{n_{\max}} p_n(\alpha) \tfrac{1}{2} \left(1 - \cos\left(\Omega_{n,n+\delta n} t\right)\right) \tag{2.11}$$

Here, $p_n(\alpha) = e^{-|\alpha|^2}\frac{|\alpha|^{2n}}{n!}$ is the initial Poissonian phonon number distribution yielding the desired information, and Rabi frequencies $\Omega_{n,n+\delta n}$ depend on the phonon number. In order to increase the accuracy of these measurements, Rabi flops can be recorded on several sidebands, which also helps set parameters such as the base Rabi frequency $\Omega_{0,0}$ or the Lamb-Dicke factor. The model Eq. 2.11 can be straightforwardly extended to the presence of spectator modes [Kau+16], which is relevant for characterizing the state of transverse secular modes, where both modes for a single ion feature nonzero Lamb-Dicke parameters. Moreover, the model can be extended to include thermal excitation as well, which is required to characterize separation processes at long duration [Rus+14].

2.3.2 Experimental control system

The experimental control system needs to provide accurate control of different electrical and electro-optical components, some of which even require synchronous real-time control below the microsecond timescale. The main elements of our experimental control system are shown in Fig. 2.6. The control computer is used to design and execute experimental sequences, which are represented in C++ code. The execution is controlled by the in-house developed software platform Master control program (MCP) , a graphical user interface (GUI) based system providing hardware drivers, sequence compilation and data processing modules. The control tasks can be separated into the following three categories:

- **Non-realtime control:** Many control operations are not executed during experimental sequences and therefore do not require synchronous real-time control. These tasks include the calibration of optical frequencies and powers of laser beams driving dipole transitions. This is done by controlling voltage-controlled oscillators and electronic attenuators via control voltages generated using National Instruments Data Acquisition (NI-DAQ) cards. Furthermore, setting trap voltages, switching photoionization lasers or determination of photodetection discrimination thresholds and other operations fall into this category. Moreover, all laser beams supplied to the trap are aligned using motorized stages[2], as the focusing optics are contained within a magnetic μ-metal shielding box, such that it is inaccessible to manual alignment. The motorized stages are controlled via Ethernet connections, more information on this can be found in [Rus18].

- **Real-time control:** The experimental sequences written in C++ are further processed to be compatible with two devices: the segment controller and the laser pulse generator, which act synchronously to move ions throughout the trap and control laser-driven qubit

[2] Picomotor Piezo Center Mount, MODEL: 8807, New Focus

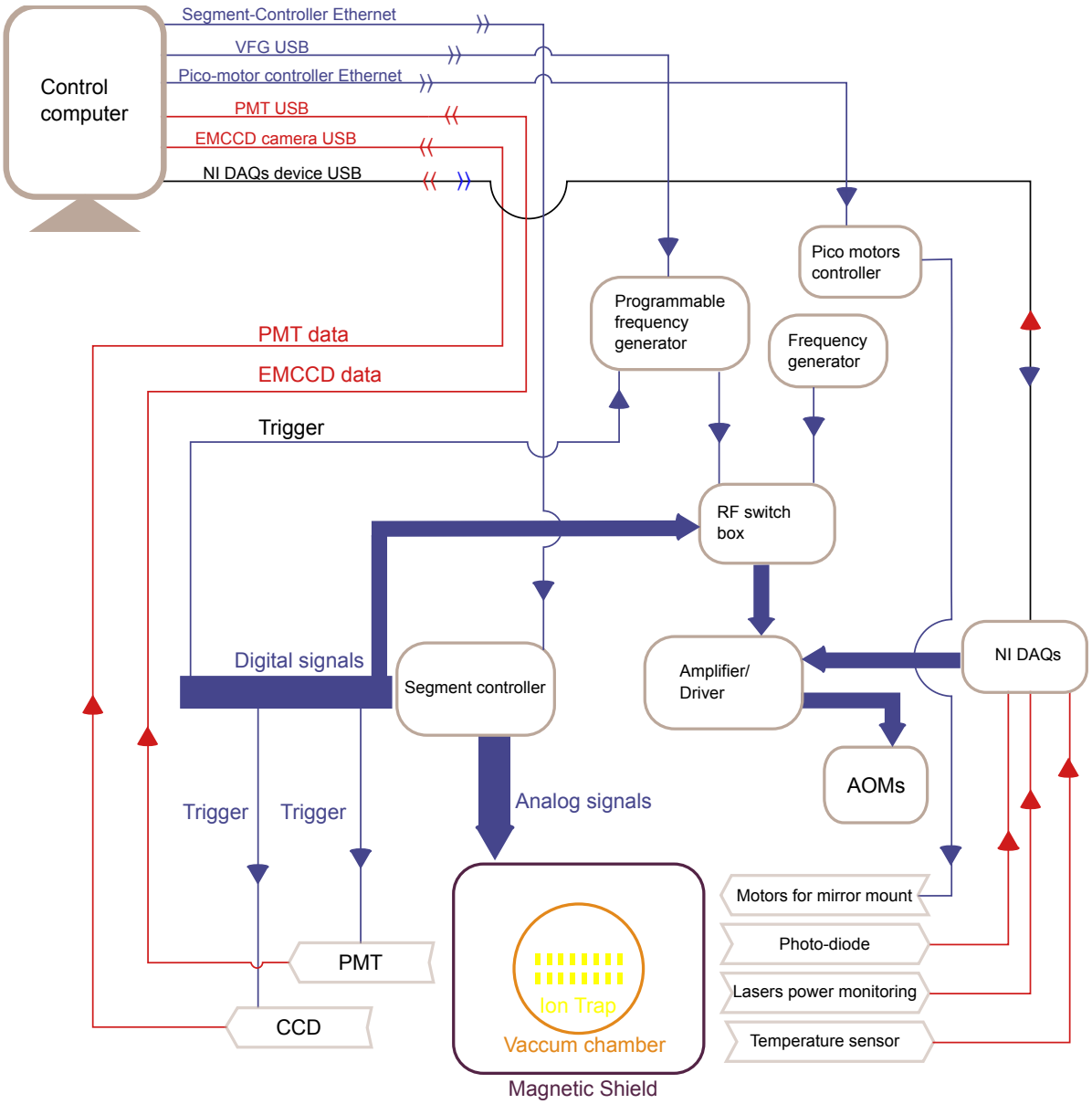


Fig. 2.6 Block diagram representation of several systems and controls used in the lab. The arrow sign (blue and red) shows the direction of data flow. Thick line arrows indicated that more than one signal is transmitted. Blue lines shows the outflow of the data from the apparatus, and red lines indicate inflow of the data into it. Presence of both blue and red arrow on a line indicates that data acquisition is bidirectional. The trap, vacuum chamber, and the magnetic shielding are shown in their respective colors.

operations. The segment controller operates as the master device, sending trigger pulses to the laser pulse generator. It is a custom-made device, and its design, manufacturing, and testing are a major part of the work done as for this thesis. A summary of its functions, specifications and performance are presented in Chapter. 4

While discussion on the design and construction are presented in Appendix. C. It is supplied with digital data via an Ethernet connection, which is consecutively stored in DDR3 memory, from where it is fetched and buffered via block random access memory (BRAM) based stacked first In first Out (FIFO) memory implemented on the FPGA of a Xilinx Zync system-on-a-chip (SoC). From there, the data bits are supplied in real-time to output pins of the Zync and routed to digital to analog converter (DAC)s connected to the trap electrodes, or digital outputs used, e.g., to trigger slave devices such as the laser pulse generator. For the latter, we currently employ the commercially available versatile frequency generator (VFG)[3]. This device generates RF pulses consisting of segments defined by an amplitude, frequency, and phase. The pulse information, including wait-for-trigger commands, is sent to the device via USB and stored in a FIFO buffer. The RF pulses are routed through a network of switches, such that AOMs controlling different laser beams can be supplied, see Fig. 4.2. More information on the switching scheme used can be found in [Kau18]. The real-time control infrastructure features a timing resolution of 20 ns.

- **Data acquisition:** Fluorescence count data obtained using a photomultiplier tube (PMT)[4] is stored on the control computer for further evaluation. Detection windows are defined by triggers generated by the segment controller. An experimental sequence is typically repeated 50-500 times to allow for accurate state population evaluations with sufficiently low statistical errors. Additionally, an electron-multiplying charge coupled device (EM-CCD)[5] camera has been used for monitoring the ions and calibrating the ions positions.

2.3.3 Gates

The versatile shuttling operations needs larger gate infidelity for the implementation of quantum processing node. The required laser-driven qubit operations are discussed in Sec. 2 and partially explained in [Pos+10]. Here, I briefly discuss onto the most sensitive operations single-qubit rotations and two-qubit entangling gates. Single-qubit rotations are driven by a pair co-propagating laser beams detuned from the $S_{1/2} \leftrightarrow P_{1/2}$ by up to $2\pi \times 1\,\mathrm{THz}$, at a frequency difference matching the Zeeman splitting in the LIZ, driving a stimulated Raman transition between $|\uparrow\rangle$ and $|\downarrow\rangle$. As this transition is driven at an effective wave-number of zero, the coupling strength does not depend on the ion motion, which is favorable in conjunction

[3] Versatile 150 MHz Frequency Generator, TOPTICA Photonics AG
[4] H10682-210, Hamamatsu Photonics K.K.
[5] Andor iXon, Model No. DV860DCS-UVB

with shuttling operations. This way, local rotations by e.g. $\pi/2$ can be driven within a few µs, at infidelities in the 10^{-5} regime. The addressing is realized inherently in our architecture with spatially distributed qubits, leading to cross-talk error which are much lower than compared to other architectures.

Two-qubit entangling gates are driven by a pair of counter-propagating far off-resonant lasers beams, coupling only to the transverse ion motion. A spatio-temporally varying ac-Stark shift off-resonantly drives one selected transverse gate mode. Depending on the global spin configuration of the qubits, this leads to transient collective oscillation. This in turn leads to a spin-configuration dependent accumulation of a geometric phase, which realizes an entangling interaction. Such $\sigma_Z \otimes \sigma_Z$-type gates were first realized in [Lei+03b]. While $\sigma_{X,Y} \otimes \sigma_{X,Y}$-type Mølmer-Sørensen gates [SM00; BW08] can also be driven with the available laser beams, a crucial advantage of the $\sigma_Z \otimes \sigma_Z$-type gates lies in the fact that gate interaction commutes with the σ_Z operators. This makes the gate operations independent of the shuttling-induced phases described in Sec. 3.1. The gate mechanism, including all possible gate error sources, are treated exhaustively in [Bal14]. The gates are currently carried out at operation times in the range of 50-100 µs, i.e. slower than the limiting timescale imposed by the transverse secular frequencies. Implementing fast gates such as realized in [Sch+18] would currently not yield an overall performance improvement of our architecture, as the timing budget for any quantum circuit is dominated by shuttling overhead. We currently achieve entangling gate fidelity of about 99.5(2)% [Kau+19].

3

Experimental qubit operations

Quantum information processing with hyperfine spin-qubits requires an experimental setup with ultrastable magnetic fields and minimal electrical noise for driving high fidelity entangling gate operations. More specifically, stability of spin-qubit in presence of permanent magnets, ground state cooling with low pass filter with larger cut-off have been addressed here. Two-qubit entangling gate operations require shuttling insensitive transverse modes and therefore heating rate and motional coherence on all modes are of great importance and improvements made to the existing trap-system will be reported in this chapter.

3.1 Magnetic field sensitive qubits

As discussed in Sec. 2.3, the qubit used in this thesis is based on the Zeeman sublevels of the $4^2S_{1/2}$ ground state of Ca and requires an external magnetic field to split the Zeeman sublevels. Therefore, the qubit states are magnetic field sensitive, which typically limits spin-echo coherence times to 10–100 ms, due to fluctuations of the external magnetic field. In our apparatus, we combine a μ metal enclosure, which is placed around the vacuum chamber (Fig. 2.5) with the use of stable permanent magnets [Rus+16] to achieve highly stable external magnetic fields. Using this setup allowed us to reach significantly improved spin-echo coherence times of 2.1 s and Ramsey coherence times of 300 ms [Rus+16]. Such coherence times are sufficient to realize quantum circuits useful for quantum information applications.

As part of this setup, SmCo permanent magnets are arranged as rings on the top and bottom of the UHV chamber, (see Fig. 3.1), which gives rise to a magnetic field oriented parallel to the magnet rings. To reduce the drifts of qubit frequency induced by variation in temperature of magnets, every fourth magnet is replaced with a NdFeB magnet with opposite magnetization

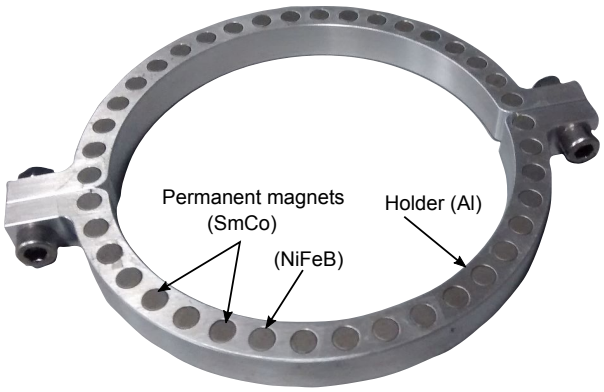


Fig. 3.1 The aluminum frame with embedded SmCo and NdFeB magnets. Every forth SmCo magnet is replaced with a NiFeB magnet in opposite orientation. Two rings are mounted co-axially on the top and bottom flanges of the vacuum chamber to generate a homogeneous magnetic field across the trapping zone.

and significantly higher temperature coefficient. Magnets were specifically selected to result in temperature dependent magnetization variations to cancel each other out. As a result the magnetic field and gradient should be temperature independent to first order.

Logging the temperature of the magnets with a 10 mK resolution and tracking the qubit frequency via repeated Ramsey type measurements over several hours, a linear relation between magnet temperature and qubit frequency of $\sim$1.5 kHz/K was measured. The residual temperature dependence is attributed to variations among the magnets, and residual magnetization of the UHV chamber, despite using non-magnetic 316L steel and thermal expansion/contraction of the chamber. It is assumed that machining of the steel increased the magnetic permeability significantly despite using 316L steel. Furthermore, it is not clear if the entire chamber is made of 316L steel or if some flanges are made of more magnetic steels like 304 steel. The small residual qubit frequency drifts can be accounted for by tracking changes and compensating for.

The magnetic field drifts have an impact on the maximum achievable fidelity of single qubit rotations. These are often characterized by means of randomized benchmarking [Kni+08], in a way where these operations are carried out directly after each other, without any waiting time. Furthermore, very often values resulting from a single qubit or an isolated qubit within a small register are reported. In a realistic multi-qubit system, addressing or switching latency might drastically affect the resulting values. In our particular architecture, shuttling-induced delay times, which can be up to several ms can occur between successive single qubit operations on a given qubit.

The current magnet setup, which is affected by the higher than expected magnetic permeability of the chamber, also gives rise to an in-homogeneous magnetic field along the trap axis. The qubit frequency was measured to varies by $\sim 2\pi \times 80\,\mathrm{kHz}$ across the entire trapping zone. This manifests in shuttling induced phase changes, as described in [Bla+09; Kau+16]. The spurious phase ϕ accumulated by an ion shuttled along the path $x(t)$ during the time between two single qubit rotations taking place at t_1 and t_2 is given by the equation:

$$\phi = \int_{t_1}^{t_2} \Delta\omega_Z\left(x(t)\right) dt, \tag{3.1}$$

where $\Delta\omega_Z(x)$ denotes the difference of the Zeeman splitting with respect to the LIZ. These phases represent deterministic error sources and can thus be mitigated. One possible strategy is the calibration via Ramsey-type measurements. This approach does not scale favorable with quantum circuits sizes, and gives rise to random errors as determined by the phase measurement accuracy. A more scalable approach is to compute the phases from eq. 3.1, while this can be done in a fully automated and efficient fashion, the resulting accuracy is determined by an accuracy of the magnetic field inhomogeneity measurements and the stability of the actual ion trajectories. Ultimately, a working solution will likely be a combination of both approaches, together with an improved magnetic field setup yielding a strongly reduced field inhomogeneity.

Variation of trap-frequencies

To analyze the anharmonic contribution due to DC or RF-segments in the trapping region of the segmented ion-trap, we experimentally determine the variation of axial trap-frequency (ω_x) by varying dc voltages. Similarly, transverse trap frequencies ($\omega_{y,z}$) are measured by varying RF-voltage level ω_x has been scanned for a voltage range of [-8,-1.5] V on trapping electrode (LIZ) while in transverse direction RF-voltage level has been scanned in range of [280, 490] V (PK-PK) on global RF-electrodes. Raman beam pair (R1/R2) has been used for axial trap frequency (ω_x, shown in green in see Fig. 3.2a) while Raman beam R1/R4 have been used for determining higher (ω_z, shown in orange in see Fig. 3.2b) and lower (ω_y, shown in purple in see Fig. 3.2b) transverse frequencies. The standard operating offsets for the measurement discussed here are -6 V at trapping segment and 350 V (PK-PK) for global RF-segments which generate ω_x=$2\pi\times 1.5\,\mathrm{MHz}$ of axial trap frequency, and in transverse direction lower trap frequency of ω_y=$2\pi\times 3.8\,\mathrm{MHz}$ and higher trap frequency of ω_z=$2\pi\times 4.6\,\mathrm{MHz}$), respectively. This measurement was needed to rule out any imperfection in the DC-segment controller discussed in Chapter. 4.

(a) Axial trap frequency

(b) Transverse trap frequency

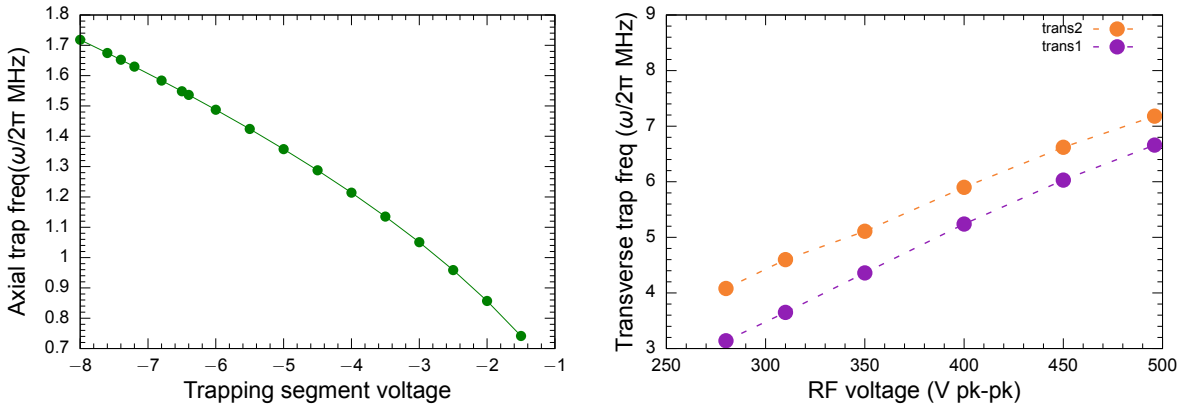


Fig. 3.2 Characterization of axial (ax, ω_x) and transverse (trans, $\omega_{y,z}$) trap frequencies. **(a)** Characterization of axial (ω_x, green) trap frequency as a function of trapping segment voltage, while keeping the trap-RF frequency constant at its standard current operating value. The standard operating value of the global RF-voltage level is 350 V (PK-PK) at frequency, f=33.04 MHz. The voltage at all other segments (except trapping segment) are set 0 V. The standard trapping voltage on the trapping segment is -6 V. **(b)** Characterization of both the transverse modes (trans1 (ω_y, purple) and trans2 (ω_z,orange)) as a function of RF-trap (PK-PK) voltage.

3.2 Ground state cooling

As ground state cooling is not the only operation performed in our experiments, but is usually followed by multiple shuttling, entanglement gate and detection operations the system cannot be optimized to achieve optimal ground state cooling only. Especially shuttling operations require fast changing voltage waveforms and therefore low pass filters with a cut-off in the frequency range of ∼kHz are used. These low pass filters allow for more technical noise to affect the secular motion and ground state cooling capabilities compared to the ones used for experiments without shuttling featuring much lower cut-off frequencies.

To determine the ground state cooling capabilities, I will therefore perform measurements using two sets of low-pass filters with cut-offs at 50 kHz and 100 kHz. More details concerning the filters and other parts of the wiring system can be found in it (see Appndx. C).

Rabi oscillations of the ground state cooled ions for the carrier (car) frequency, red and blue sidebands were recorded and are shown in Fig. 3.4. Mean phonon numbers ($\bar{n}$) are extracted by fitting the rsb and bsb sideband oscillations (see Sec. 1). Phonon numbers achieved after ground state cooling for both filter setups and the three secular motions are shown in see Tab. 3.1.

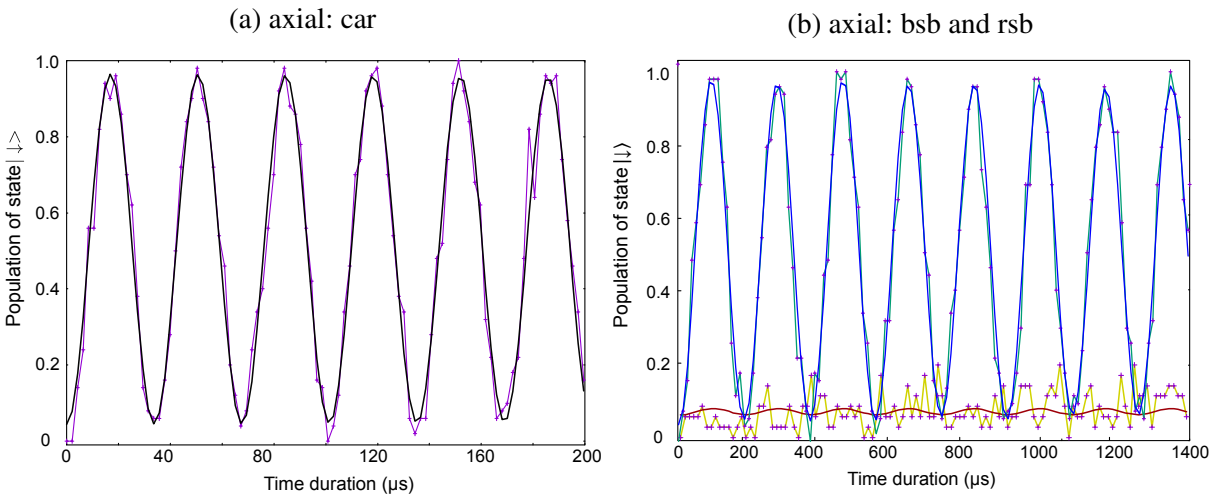


Fig. 3.3 Rabi oscillation of ground state cooled ion on axial motional mode. **(a)** The carrier frequency from experimental data and its non-linear fit are shown in purple and black, respectively. The base Rabi frequency of car transition was $\Omega_{car}^{\omega_x}/2\pi$=25 kHz. **(b)** The sidebands rsb and bsb frequencies from experimental data are shown in yellow and green, while their non-linear fits are shown in blue and red respectively. The sidebands (rsb/bsb) transitions are oscillating at $\Omega_{rsb/bsb}^{\omega_x}/2\pi$=5 kHz. These fitted curves to experimentally measured data points are used to calculate the mean phonon number ($\bar{n}$). The value of $\bar{n}_{\omega_x}$ is 0.02(1) ph. The current state is achieved using a low-pass frequency filter with f_c=100 kHz at secular frequency of ω_x=$2\pi\times$1.5 MHz.

		Mean phonon occupation number($\bar{n}$)		
secular frequency	η	50 kHz (old)	50 kHz	100 kHz
ax ($2\pi\times$1.48 MHz)	0.2	0.01(5)	0.06(7)	0.02(1)
trans1($2\pi\times$3.6 MHz)	0.08	0.33(1)	0.05(7)	0.05(3)
trans2($2\pi\times$4.6 MHz)	0.09	0.05(7)	0.01(5)	0.02(1)

Table 3.1 The comparative ground state cooling results of the motional state in newer and previous experimental setup.

The mean phonon occupation number ($\bar{n}$) achieved after ground state cooling of calcium ions in the experimental setup, which was improved for this work, shows similar phonon numbers (see Tab. 3.1) on axial modes compared to previous measurements presented in [Kau+14; Rus+14]. The transverse modes (trans1 and trans2) show significantly lower mean phonon numbers and therefore better cooling. The overall performance of the modified setup shows a clear improvement over the old system allowing for faster waveforms making use of the higher cut-off frequency and therefore making faster shuttling operations possible.

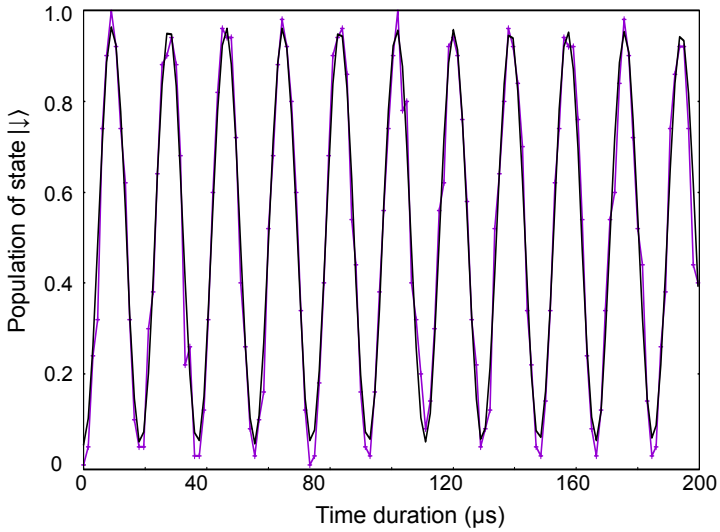


Fig. 3.4 Rabi oscillation of carrier transitions of ground state cooled ion on transverse mode. The carrier frequency from experimental data and its non-linear fit are shown in purple and black, respectively. The base Rabi frequency of this transition is $\Omega_{car}^{\omega_{y,z}}/2\pi$=50 kHz. The secular frequency of trans1 and trans2 are $\omega_y/2\pi$=3.8 MHz and $\omega_z/2\pi$=4.6 MHz respectively. The experimental state and color scheme of plot are identical to Fig. 3.3. The sideband (rsb/bsb) for both transitions (lower and higher frequencies) of this mode are shown in Fig. 3.5.

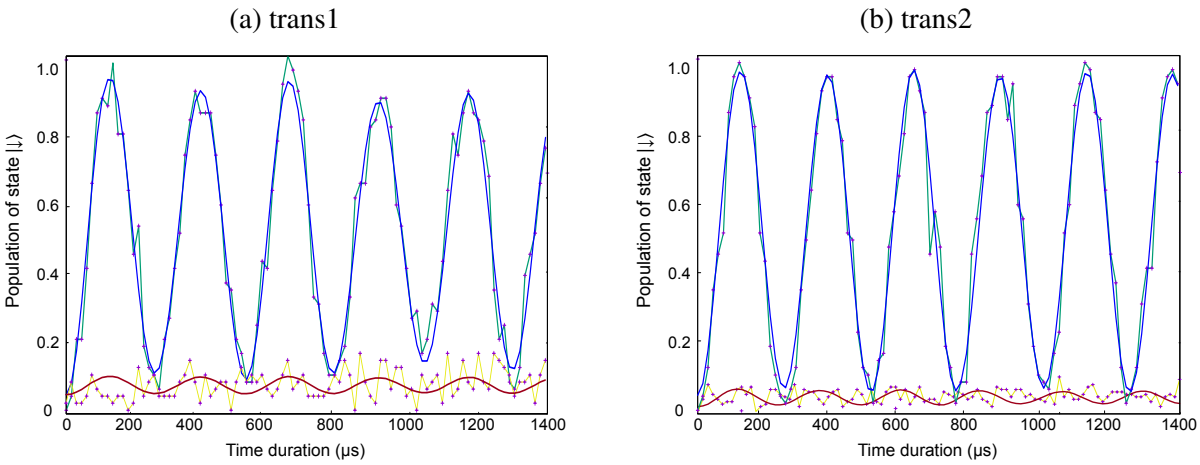


Fig. 3.5 Rabi oscillation on sidebands (rsb/bsb) transitions of ground state cooled ion on transverse mode. **(a)** The base oscillation frequency of sidebands at lower frequency mode ($\omega_y/2\pi$=3.8 MHz) is $\Omega_{rsb/bsb}^{trans1}/2\pi$=3.3 kHz. **(b)** And, for higher frequency transverse mode $\omega_z/2\pi$=4.6 MHz is $\Omega_{rsb/bsb}^{trans2}/2\pi$=3.7 kHz. The experimental state and color scheme of plot are same as stated in Fig. 3.3.

3.3 Heating rate

Making use of the previously established ground state cooling of single trapped ions a heating rate measurement can be performed. Heating of the ion is an increase in vibrational occupation of the secular modes due to electric field noise coupling to this motion. Of the entire spectrum of electric field noise, only frequencies equal to the secular frequencies and also equal to the drive frequency or a combination of both cause heating. The rate of mean phonon occupation number increase (i.e rise in the ladder of vibrational energy level) is defined as the heating rate [Tur+00b; Bro+15]. Based on multiple experimental results from various groups [Bro+12] a power law as mentioned below was found:

$$S(E) = \omega^{-\alpha} d^{-\beta} T^{+\gamma} \tag{3.2}$$

Where ω is the acting secular frequency, d is distance of the trapped ion from the trapping surface, T is the temperature of ion trap and α, β and γ are their respective scaling exponents. The relations between spectral noise density and heating rate (expressed as $\dot{\bar{n}}$) and with ω representing secular frequency of trapped-ion is equal to,

$$\dot{\bar{n}} = \frac{q^2}{4m\hbar\omega} S(\omega) \tag{3.3}$$

and

$$S(E) = 2\int_{-\infty}^{\infty} \langle E(t)E(t+\tau)\rangle e^{-i\omega\tau} d\tau \tag{3.4}$$

Where S(E) is the spectral noise density of the electric field [SOT97; DJ+; Bro+12]. Temperature of the trap electrodes or ion-electrode distance can not be varied in our setup and therefore only variation of the heating rate as a function of secular frequency will be discussed.

Main sources for heating are technical noise i.e. noise coming from the lab environment or multi-channel arbitrary waveform generator (mAWG), which after filtering still has a significant component at the relevant frequencies and anomalous heating. This form of spectral frequency noise is not fully understood and therefore called anomalous noise. Johnson–Nyquist noise, which is inherent to any electric circuit is significantly lower in the relevant frequency spectrum and is generally not relevant in ion trap setups.

Using ground state cooling and measuring the mean phonon number $\bar{n}$ of all motional modes after waiting for various period, one can determine the rate of heating on modes. Results of such measurements for different low-pass filters are show in Fig. 3.2.

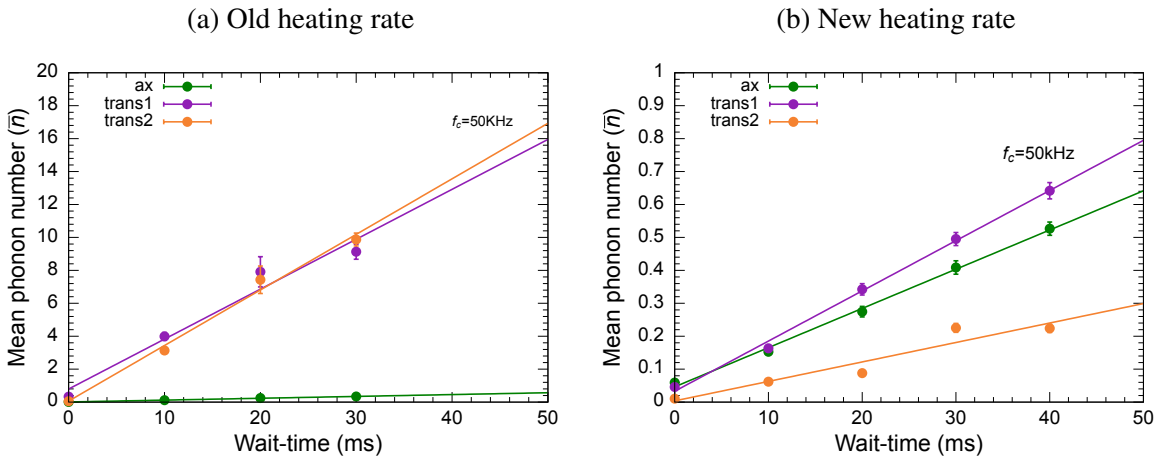


Fig. 3.6 Heating rate measured at all motional modes (ω_x, ω_y, ω_z), in (a) previous and (b) new experimental control setup. Other experimental conditions during both measurements were identical. The respective secular remain as state earlier (ω_x=2$\pi\times$1.5 MHz, ω_y=2$\pi\times$3.8 MHz, ω_z=2$\pi\times$4.6 MHz). The cut-off frequency of low pass filters used in both measurement is f_c=50 kHz. **(a)** For previous setup, heating rate measured are 11.4(2) ph/s (green) on ω_x, 363(6) ph/s (purple) on ω_y and 318(16) ph/s (orange) on ω_z, respectively. **(b)** For newer setup, heating rates have improved marginally on ω_x with 9(1) ph/s and large improvement with 15.0(8) ph/s, 5.4(7) ph/s on lower (trans1, ω_y) and higher (trans2, ω_z) transverse modes have been measured. The color scheme is consistent with (a) for respective modes.

The heating rate on the axial mode remains consistent within the error bar limit independent of changes made in the experimental system. Before optimizations, the heating rate measured on axial (ω_x=2$\pi\times$1.49 kHz), lower transverse mode (ω_y=2$\pi\times$3.81 kHz) and higher transverse mode (ω_z=2$\pi\times$4.6 kHz) were 11.4(2) ph/s, 363(6) ph/s, 318(16) ph/s, respectively. After improvements were made, newer values of $\dot{\bar{n}}^{50\ kHz}_{\omega_{x,zy,z}}$={11.5(5), 15.0(8), 5.4(7)} ph/s were measured on respective motional modes.

The low pass filters used in both case feature a cutoff of f_c=50 kHz. The latest measurement with f_c=100 kHz, shows heating rates of $\dot{\bar{n}}^{100\ kHz}_{\omega_{x,zy,z}}$={9(1), 26.6(7), 9.2(3)} /ph/s on respective modes. Like previous measurement, only transverse modes show and increased heating rate by a factor of $\sim$1.7, while the heating rate on the axial mode remains similar within error bar limit and hence not affected by this change. This behavior is rather unusual, and we believe it is caused by technical noise, which is close to the axial mode secular frequencies and to these frequencies $\pm$ the drive frequency. Another factor could be common-mode noise on all dc segments, due to remaining ground loops or other technical noise, to which the axial motion would be less sensitive. The results of previous setup [Kau+14; Rus+14] and the improved setup are summarized in Tab. 3.2.

ω	η	$\bar{n}(ph/s)$			r=$\frac{\bar{n}_{100\ kHz}}{\bar{n}_{50\ kHz}}$	S_E(v^2/m^{2}Hz)		
		50 kHz (old)	50 kHz	100 kHz		50 kHz (old)	50 kHz	100 kHz
ω_x	0.2	11.4(2)	11.5(5)	9(1)	0.78	$1.12\text{x}10^{-13}$	$1.12\text{x}10^{-13}$	$9.21\text{x}10^{-14}$
ω_y	0.08	363(6)	15.0(8)	26.6(7)	1.77	$8.45\text{x}10^{-12}$	$3.51\text{x}10^{-13}$	$6.52\text{x}10^{-13}$
ω_z	0.09	318(16)	5.4(7)	9.2(3)	1.70	$9.62\text{x}10^{-12}$	$1.5\text{x}10^{-13}$	$2.85\text{x}10^{-13}$

Table 3.2 Comparison of heating rates on all three motional modes of a trapped ion using two different type of low pass filters with cut-off of f_c=50 kHz and f_c=100 kHz

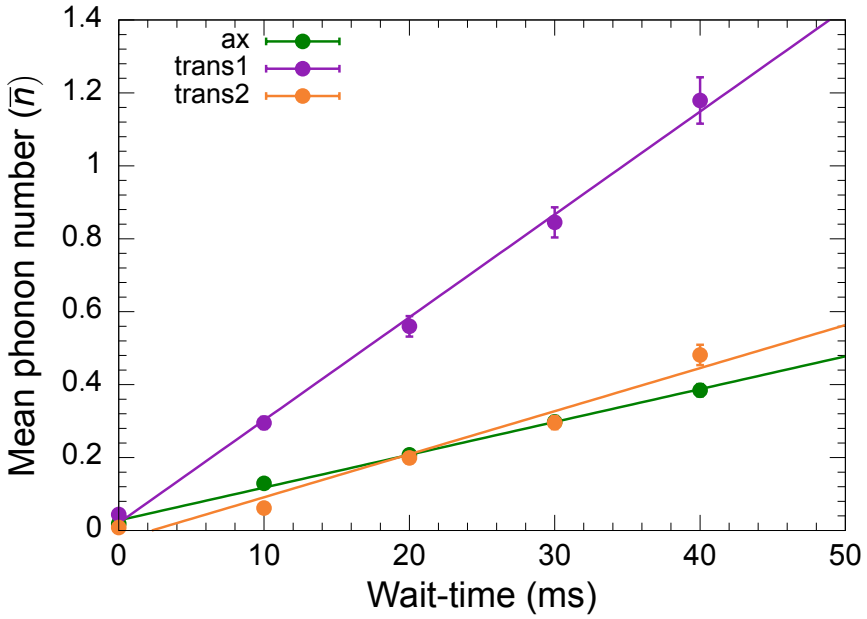


Fig. 3.7 Heating rate measured on all motional modes with higher cut-off (f_c=100 kHz) of low pass filter. Heating rate on different motional modes are $\dot{\bar{n}}^{100\ kHz}_{\omega_{x,y,z}}$={9(1), 26.6(7), 9.2(3)} ph/s. Other experimental conditions remain identical as of earlier discussed results. And the color scheme of this plot and trap-frequencies during this measurement are also consistent with Fig. 3.6, discussed earlier.

Variation of heating rate with trap frequency

The heating rate measurement as function of axial motional mode trap frequency has been shown in Fig. 3.8. A fit was made assuming a power law relation between heating rate and respective motional mode frequency of type (A/ω_x^{α}) as suggested in eq. 3.2. The measurement was performed by adjusting the voltages applied to the trapping segments and therefore changing the axial confinement strength, which also leads to a change of axial trap frequency. The new trap frequency is measured using the sideband spectroscopy. A fit with a power law ($f(\omega_x)$=a$\cdot\omega_x^{-\alpha}$) is plotted for the heating rate data measured for different axial trap frequency in Fig. 3.8. The power law fit of function type yields α=1.3(1), which is in agreements (α=[1:2]) with several measurements from other ion trapping groups (Fig:3 in [Bro+15]),

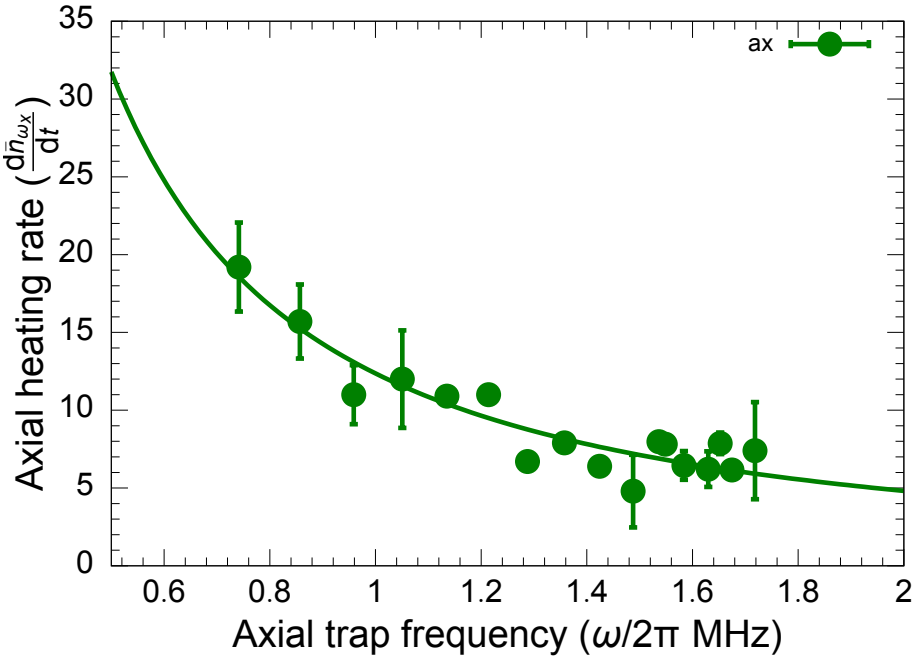


Fig. 3.8 Heating rate, $\dot{\bar{n}}_{ax} = \frac{d\bar{n}}{dt}$, as a function of axial trap frequency (ω_x). The highest measured heating rate is 19(2) ph/s at ω_x=$2\pi\times$0.742 MHz, while the lowest heating rate of 5(1) ph/s has been measured at ω_z=1.48 MHz, the commonly used axial secular frequency in the lab. The weighted power-fit (solid line) derived from the data is, $\frac{d\bar{n}}{dt} = 12.4(4)\omega^{-1.3(1)}$. Exponent ($\alpha$) of the power fit is in good agreement with the commonly observed values in other publications (Fig.3, [Bro+12]). The error bars in some measurement points are invisible as they are small in comparison to the point used in the graph. For this measurement, low-pass filter has the $f_c = 50$ kHz.

[Hit+12; Dan+14; Tur+00b].

The figure shown in Fig. 3.9 shows the variation of heating rate on higher frequency radial modes (trans2, ω_z=4.6 MHz). The maximum heating rate of 11(1) ph/s at ω_z=$2\pi\times$4.08 MHz (trap-RF=280 V (PK-PK)) and minimum of 2.0(3) ph/s ω_z=$2\pi\times$5.11 MHz (trap-RF=350 V (PK-PK) has been measured. The frequency of trap-RF was $\Omega_{RF}/2\pi$=33.04 MHz).

motional mode	$\dot{\bar{n}}_{min}$(ph/s)	$\omega_{x,y,z}(\dot{\bar{n}}_{min})$	$\dot{\bar{n}}_{max}$(ph/s)	$\omega_{x,y,z}(\dot{\bar{n}}_{max})$	A	α
axial	4.8±2.3	1.48 MHz	19(2)	0.741 MHz	12.4(4)	1.3
transverse(trans2)[1]	2.0(3)	5.11 MHz	11(1)	4.08 MHz	89.09±153.5	1.67±1.087

In conclusion, the heating rate has been improved and distinct dependence of the heating rate and used filter was measured. Use of a low noise voltage source in combination with the

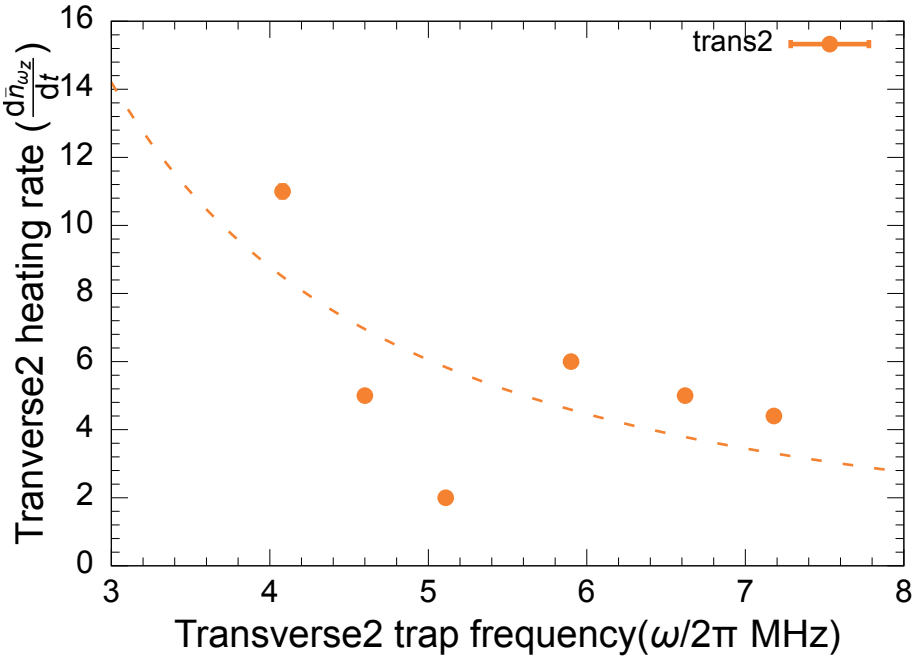


Fig. 3.9 Heating rate, $\dot{\bar{n}}_{trans2} = \frac{d\bar{n}}{dt}$, as a function of higher transverse trap frequency (ω_z=2π×4.6 MHz). The highest measured heating rate is 11(1) ph/s at ω_z=2π×4.08 MHz, while the lowest heating rate of 2.0(5) ph/s has been measured at ω_z=2π × 5.11 MHz. An expected exponential variation of these distributions has been drawn (dashed line) from the data itself. The error bars in some points are invisible as they are smaller than size of the point used.

developed filtering yielded very low axial heating. Transverse mode heating was not as low as expected and further improvement of the technical noise and potentially an upgrade of the RF voltage delivery system is required. Plotting the heating rate measurements versus secular frequency yield results consistent with the power-law commonly observed in other experiments but also indicates the role of technical noise on the transverse modes. Neglecting other error sources, measured heating rates allow for up to 10^3 consecutive two-ion entangling gates at a duration of 50 µs (see Sec. 5) without significant decoherence.

3.4 Motional coherence

The motional decoherence is a characterization of the dephasing contrast of spin and motional superposition state. A long motional coherence is required for high fidelity geometric phase gates, as it is the second largest contribution in the error budget of these qubit gates [Bal14]. Hence, the characterization of motional coherence is critical before trying to achieve high fidelity in quantum information processing (QIP) based experiments. Also, the success of QIP with scaled qubits depends on maintaining high gate fidelities independent of the number of

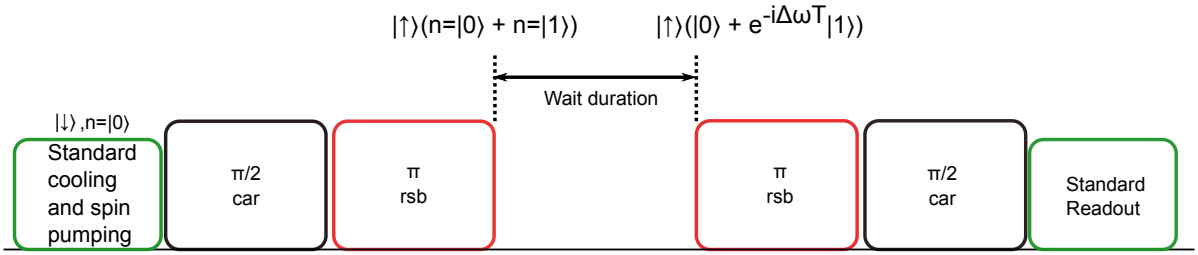


Fig. 3.10 Ramsey sequence for measuring motional decoherence.

qubits [Bal+15].

Noisy DC and RF trap voltages lead to fluctuating secular trap frequencies, which lead to dephasing of motional superposition states occurring during entangling gate operations. White trap frequency noise leads to exponential decay of motional coherence at rate γ_m. We measure these rates on all three secular modes of a single ion in the motional ground state in the Laser interaction zone (LIZ) by means of a motional Ramsey scheme. The following steps are performed: i) A qubit superposition $(|\uparrow\rangle + |\downarrow\rangle)|0\rangle$ is created by a resonant $\pi/2$ rotation, ii) a π rotation on the red sideband of the mode of interest creates the superposition $|\uparrow\rangle(|0\rangle + |1\rangle)$, iii) dephasing takes place during a variable wait time T, iv) another π rotation maps the motional superposition back into a spin superposition, and v) a $\pi/2$ spin rotation with(without) $\pi/2$ phase shift is used to measure the spin $\hat{\sigma}_X(\hat{\sigma}_Y)$ operators. The resulting measured Ramsey contrast decreases with T. The results for all secular modes are shown in Fig. 3.11.

In spite of substantial effort for attenuating the technical noise(see Sec. D), 50 Hz ac-line pickup was noticed in the experimented, therefore, ac line sync (line-trigger, LT) are used to attenuate the impact of continuous and periodic ac-line noise in the experiments. The measurements have been carried out with (with LT) and without (without LT) and comparative results in the newer setup are as: In the latest measurement, $56(8)$ ms without LT and $57(9)$ ms with LT have been measured on axial mode. This is comparable to previous data of $58.7(8)$ ms without LT and $58(1)$ ms with LT, measured in previous [Kau18] setup before improving it.

There is a large contrast in decoherence duration on both transverse modes. A comparable value within error bar limits which was previously measured with LT can now be measured without using LT (without LT).

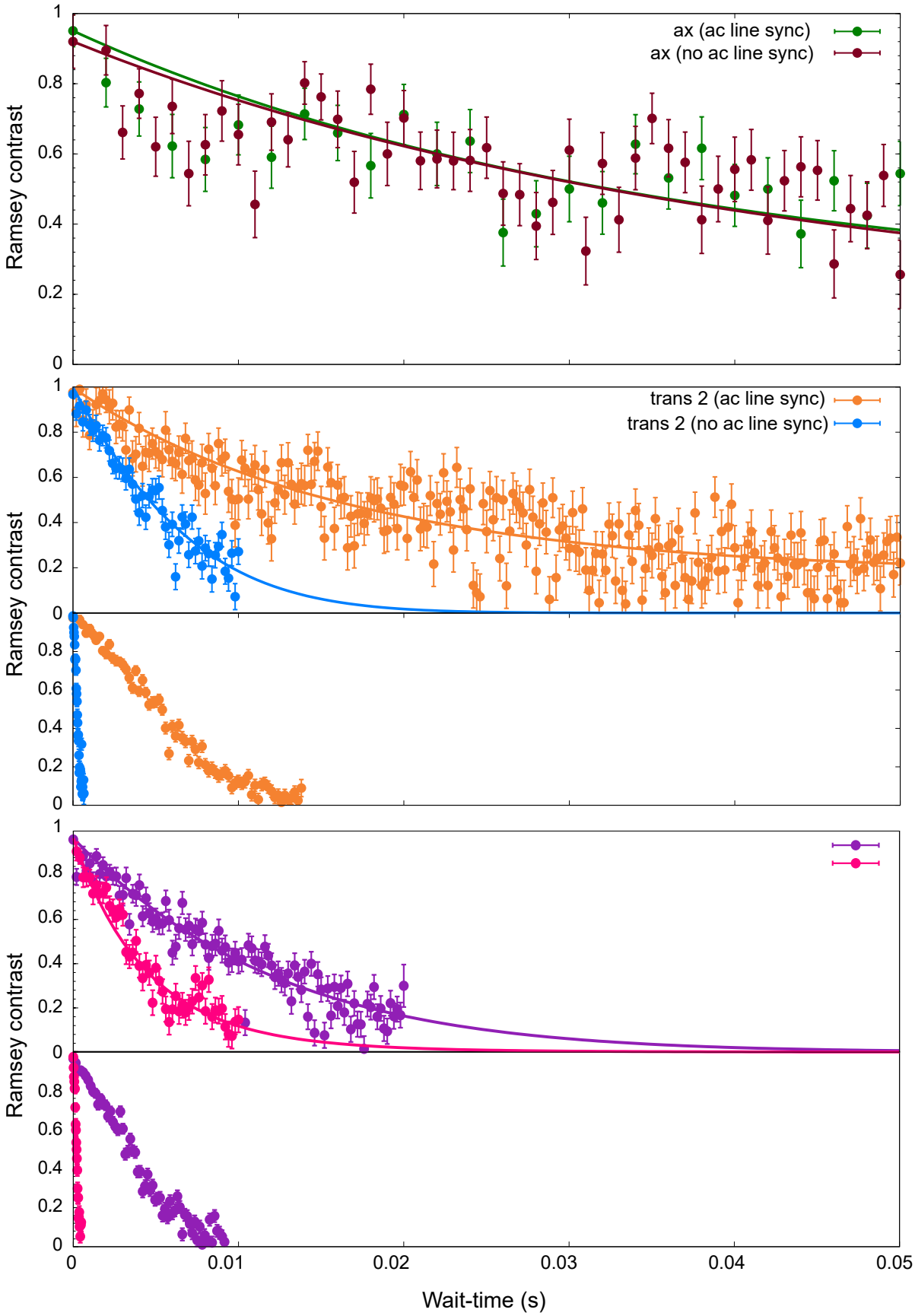


Fig. 3.11 The motional coherence contrast measured for all principle modes with(LT)/without(no LT) synchronizing with mains ac-line. The secular frequencies for all the modes is same as that of previously discussed heating rate measurements (ω_x=$2\pi\times1.48$ MHz (ax), ω_y=$2\pi\times3.80$ MHz (trans1), and ω_z=$2\pi\times4.6$ MHz (trans2)).

The top-most plot shows Ramsey contrast for axial motional mode(ω_x) with LT (green) and without LT (brown). The contrast duration of ~56(8) ms and ~57(9) ms have been measured with LT and without LT, respectively. The middle and lower plot compares the ramsey contrast of higher (trans2) and lower (trans1) frequency transverse mode in newer and previously used experimental setup, respectively. In both plots, upper plots shows the imroved contrast, while lower one of respective plots are from previous measurements [Kau18]. In the middle plot, contrast for trans2 with LT (orange) and without LT (blue) are shown. The contrast durations of 24(1) ms and 6.4(3) ms were measured for trans2 mode with LT and without LT in newer setup, respectively. While previously, the best case measured value were 6.47(7) ms and 0.323(4) ms measured with LT and without LT on trans2 mode, respectively. In the lowest plot, contrast for trans1 with LT (purple) and without LT (pink) are shown. The contrast durations of 11.6(5) ms and 4.6(3) ms were measured for trans1 mode with LT and without LT in newer setup, respectively. While previously, the best case measured value were 4.39(6) ms and 0.248(4) ms measured with LT and without LT on trans2 mode, respectively.

On lower frequency transverse mode (trans1), similar improved results have been measured. Previously, 0.248(4) ms and 4.39(6) ms were the best measured value for without LT and with LT cases respectively. In current setup, improved value are 4.6(3) ms and 11.6(5) ms for the cases without LT and with LT, respectively. The contrast duration with LT observed in old setup can be measured in free running system (without LT) now, this shows that there is substantial reduction in 50 Hz main line noise. The comparative plot of different dephasing contrast recorded from previous and currently deployed experimental setup have been shown in Fig. 3.11 and results of these plots have been tabulated in Tab. 3.3.

mode	old measurement		new measurement		% decrease (⇓)/increase (⇑)	
	τ (ms)	τ_{LT} (ms)	τ (ms)	τ_{LT} (ms)	w/o LT	w LT
axial	58.7(9)	58(1)	56(8)	57(9)	$\approx$	$\approx$
trans2	0.323(4)	6.47(7)	6.4(3)	24(1)	~1981⇑	~375⇑
trans1	0.248(4)	4.39(6)	4.6(3)	11.6(5)	~1854⇑	~264⇑

Table 3.3 Comparative chart of motional decoherence in old and new experimental environment.

Both transverse modes show improvements consistent with measured heating rate, however still far away from expected theoretical value [Tur+00a] ($1/\bar{n}$) based on the previously discussed measurements of heating rates. There is still room for improvement especially on the transverse modes as there is a relatively large difference between expected and measured values. Based on the measurement data presented here, many observations can be inferred: 1) The contrast value that had been observed with LT in the old set-up can now be measured in the new setup without

LT and this is true for both lower and higher frequency transverse modes. 2) The relative increment of trans2 and trans1 is proportional to the transverse mode trap-frequency. 3) Like heating rate, the motional coherence on the axial mode (ω_x) also remain consistent within the error bar limits, which means that noise causing fast dephasing is completely uncorrelated to the axial mode and hence does not add to the decay of the state.

In conclusion, for the axial mode, the contrast decay is consistent with being caused by anomalous heating, $C(T) = \exp(-2\dot{\bar{n}}T)$, and no effect of the ac mains is seen. By contrast the coherence times on both transverse modes are significantly shorter, and a beneficial effect from triggering the measurements to AC mains can be clearly recognized. While the lower-frequency transverse mode falls short of the higher frequency one, the contrast decay for the ac-line synchronous case is again consistent with the anomalous heating. The higher-frequency transverse mode exhibits a shorter coherence time compared to the axial mode, despite featuring a quantitatively similar heating rate. The data shows that our system is capable of offering sufficient bandwidth for fast shuttling operations, while at the same time anomalous heating rates and motional coherence times allow for high-fidelity gates driven on the transverse modes. However, there are several discrete frequencies components which are not correlated to the 50 Hz noise and are leading to dephasing of all motional modes. More thorough investigation is needed to establish and correlate these frequencies dependent noises to different secular modes.

4

Scalable control hardware for shuttling operations

4.1 Introduction

Performing the qubit operations on any arbitrary ion using a single laser interaction zone (LIZ) requires an advanced shuttling capabilities ranging from simple ion transport over multiple trap segments to splitting or merging of ions and rearranging of ions in a string. To perform these operations a trap segment control hardware is required which should be capable for doing these shuttling operations. Also, on-growing complexity to handle qubit storage for scalable quantum computing, additionally, the control hardware should also be scalable in nature. The general purpose control hardware is designed like an advanced and scalable mAWG, which can supply time-dependent voltage waveform to individual trap electrodes and simultaneously control the duration of laser pulse for controlled light-matter interaction. While performing the sensitive qubit operations, mAWG must also ensure that stable, accurate and low noise voltages are provided for the confinement of ions. In this chapter, I discuss the general system architecture of the mAWG that is used for experiments. A detailed technical description of this can be found in Appndx. D. Details on the wiring from mAWG to trap electrodes, which are optimized for optimal performance under real lab condition has been discussed (see Appndx. D).

Previous to these developments (N_Bertha or mAWG) described in this thesis, an old waveform generator (Bertha) had existed in our research group, which was improved prior to mAWG. I briefly summarize design and limitations of old design and present the reasons for development of the new system from scratch. Then, beside general outline of the system architecture of mAWG, and operational principles of the individual components have been

thoroughly discussed. At last, the performance report of this mAWG in time and frequency domain has been presented.

Older shuttling hardware (Bertha)

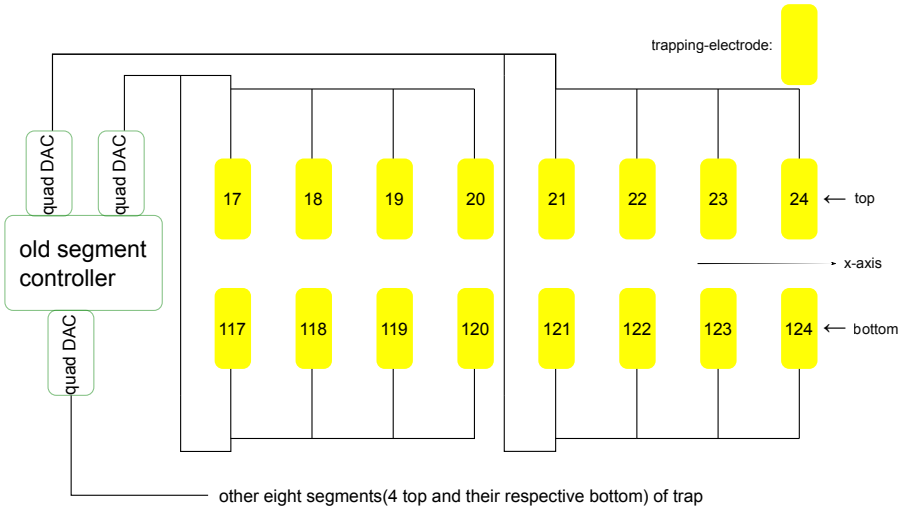
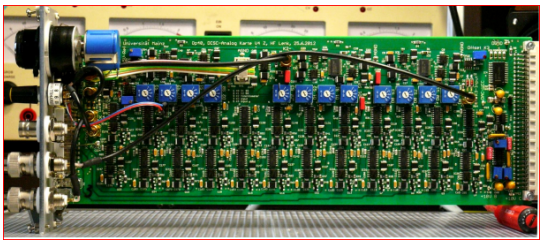


Fig. 4.1 The routing layout of analog channels with the electrodes of the ion-trap. This configuration was used with old analog cards (see Fig. 4.2a) installed in old segment controller (see Fig. 4.2). The layout idea of this analog card was to connect four top trap-electrodes with active channels of a quad-DAC. While, four bottom trap-electrodes were connected to complement channels of the same quad-DAC. On each of the analog card, there were three quad-DACs (DAC8814), so twelve active and twelve complement channels were connected to the top and bottom DC-electrode of the ion-trap. The active channels are the individual channel of quad-DACs, while the buffered channels are called as complement channels. Please note that the intermediate low pass filter has not shown in the figure, although it is always present between trap electrode and voltage source.

In-house developed, the previous shuttling hardware (or segment controller)(Bertha) was the first generation of mAWG designed by Kilian Singer, Sam Dawkins and Heinz Lenk at the University of Mainz. This system is still used in different research labs of Quantum, Uni-Mainz. It features low noise, precise and fast voltage update to ion-trap electrodes and hence this has been instrumental in several successful scientific investigation [Fel+15; Roß+16; Sch+16; Rus+17; Wol+18; WSS18; Bra+16; Bra16; Kau+19; Von+18]. It houses five analog cards (see Fig. 4.2a and Fig. 4.2), where each of the analog cards contain three quad-DACs which altogether form twelve independently controllable analog-channels (active channels) for electrodes of ion-trap. It has twelve additional channels, which are derived from each of the active analog channels. These channels can be also controlled independently. This way,

every analog-card output twenty-four analog voltage channels. These derived channels are called as complement channels. There is also provision for adding or subtracting an additional voltage-offset to these active and its complement channels. For, e.g., the desired offset of 2 V will increase the voltage of active and subsequently decrease on the complement channel by 2 V, within range of ± 10 V. There are five different ways of adding voltage offset to these channels. They are internal DACs (two), external channels (two), a on-board powered potentiometer. The external voltage sources add noise to the internal analog channels, so they are not recommended for including offsets to the programmed voltage, and hence the external input channels has to be terminated by 50 Ω-termination. Two internal DACs channel are recommended for adding voltage offsets to the programmed channels (Channel: 7 & 11 should be used for this purpose). If either or both of these channels are used as compensation source then they cannot be used to power respective electrodes of the ion-trap, and the voltage on these channels will be 0 V.

(a) Old analog card



(b) Old shuttling hardware (Bertha)

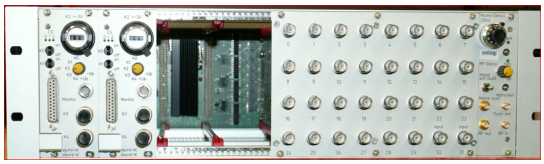


Fig. 4.2 Previous used analog card and the shuttling hardware (Bertha). **(a)** The old analog cards output voltages to twenty-four trapping-electrodes with on-boards available twelve active and its complement buffered analog channels. Each of the channel has voltage range of ± 10 V. (b) The old segment controller (Bertha) houses four analog cards, therefore ninety-six analog channels for shuttling operations and thirty-one digital TTL signal for shaping the laser-pulse for qubit manipulation inside the segmented ion-trap. The figure **(b)** shows shuttling hardware unit with two analog cards (left side in their respective slots with SUB-D 25 connector) and BNC slots (right-side) for providing digital TTL signals.

In general, the analog channels exploit the fact that top and bottom electrodes has same voltage for the generation of harmonic confinement in 3-D segmented Paul trap [S+06], so an active and its complement channel are generally used for biasing top and bottom electrodes. A fully populated old segment controller with analog cards can provide a total of ninety-six analog channels for the electrodes of any segmented ion trap.

The Virtex-5[1], Field programmable gate array (FPGA) is used to generate the digital signals for programming the quad-DAC of analog-modules via serial programming interface (SPI) interface. The onboard operational-FPGA generates sixty-four data bus lines for this purpose. The analog module has four analog cards, where each of these cards use seven digital lines for controlling on-boarded three quad-DACs. The digital lines consists of three data-lines, three chip-select-lines, and one load-line. A total of twenty-nine (one is clock line) lines are used for driving analog module and thirty-one lines are used for the shaping of laser-pulse duration during qubits manipulation. An analog card and its half populated control hardware has been shown in Fig. 4.2.

Limitation of older shuttling hardware

The performance of old segment controller was optimal with some serious limitation that was acting as bottleneck for qubit storage and gate fidelity. Among several limitations, two main drawback was untraceable reason for higher decoherence on the radial modes and its saturated support for enhancing the shuttling threshold performance already achieved by it. Also, our segmented ion-trap was underutilized as precise and independent access to all its DC-segments were not possible due to presence of quad-DAC[2].

Although the total number of channels stated were large (ninety-six), only limited channels can be simultaneously. Each channel of quad-DAC can only be programmed at the interval of 600 ns. So, wait duration between first and last programmed channel of quad-DAC was 1800 ns, potentially making it slow enough to deter performance in faster shuttling operation. This drawback reduces number of analog channels from 96 to 12 (independently controllable channels). The total number of electrodes in the segmented ion-trap is 32, which is larger than the available resources. The power-supplies were also the ill-planned, hence suspected to be the reason for larger decoherence rate (see Sec. 3.3) on radial secular modes. The range of the voltage was also limited to $\pm$ V, which is far below than upper threshold voltage-limit (~50 V) of the charge coupled device (QCCD) [Kau18; Mau16]. Also, voltage range was bottle-neck for improving the performance of shuttling operations [Kau+14]. And lastly but not the least, the FPGA used as driving firmware had a smaller memory of 64 MB, providing slow access to its memory resources and also non scalable in nature. These limitations were critical in a sense as larger sequences such as the implementation of shuttling operations with quantum error correction will be impossible. Also, the presence of stronger FPGA in the market has limited the support for this firmware, and therefore, the inclusion of any advanced feature to

[1] Virtex-5 FXT Mini-Module Plus
[2] DAC8814 from Texas instrument

this design was impossible. So, to overcome these limitations, another improved release of the segment controller has been designed.

4.2 New generation shuttling hardware (N_Bertha)

Newer shuttling hardware (N_Bertha) is second generation of mAWG, which has been developed for scalable quantum computing at University of Mainz. Although this newer mAWG is not an incremental development from its predecessor, however the main goal of voltage supply to the trap-electrodes and control of the laser pulse duration is similar with several add-on significant features in it. It is developed on newer algorithms which is compatible for both new generation SoC-FPGA and 7-series FPGA. It forms the basis of scaling the segment control hardware for managing large qubit storage and also provide flexibility for adding several advanced feature like feed-forward (see Sec. 6) to it. The system architecture of this mAWG type controller has been discussed in this section. (Due to wide range of importance, it is also addressed contextually by names like Segment controller, Voltage controller, or mAWG).

The idea of latest SoC-FPGA based an advanced segment controller hardware design is also motivated to provide a module based technological basis to meet the on-growing complexity of segmented ion-trap based QIP experiments. The new mAWG makes use of a Zynq System-on-chip (SoC) controller, which supplies digital data channels driving up to eighty independent digital-to-analog converters (DACs) in real-time for programming via SPI interface (see Fig. C.31). It can store voltage waveform data up to 1 GB in on-board memory and supply 24 additional digital I/O channels which can be used e.g. for shaping the duration of laser pulses. A schematic showing the interplay of SoC, analog cards, digital modules and other essential components is presented in Fig. 4.3. In this section, general working principle and its real-time performance have been presented. However, a detailed technical description as suggested can be found in Appendix (Appndx. C and see Appndx. D) which is relevant for real-life development of such system.

The mAWG is controlled and supplied with waveform data by the experimental host computer using an Ethernet connection. The host computer can send large data sequences to CPU cores on the Zynq, which are then saved to onboard RAM memory by ARM processor (processing system, PS). After receiving a trigger command from the host PC via Ethernet, the FPGA (programmable logic, PL) section of SoC-FPGA accesses the stored data sequence and streams it without interruption at digital I/O pins which is then redirected to analog and digital output modules of mAWG. The DAC modules convert the digital signals to voltage waveform,

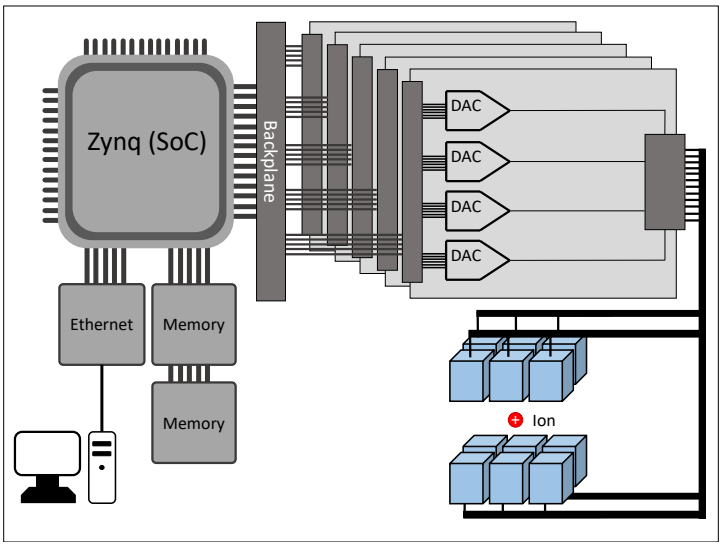


Fig. 4.3 The schematic primarily showing the interplay of individual modules of the mAWG and also critical parts of the experiment, ranging from control computer (and SoC-FPGA, analog and digital modules) to ion trap electrodes. The computer writes the digital data to SoC-FPGA memory via Ethernet. This data is sent to the analog and digital modules to general the respective (analog and digital) signals.

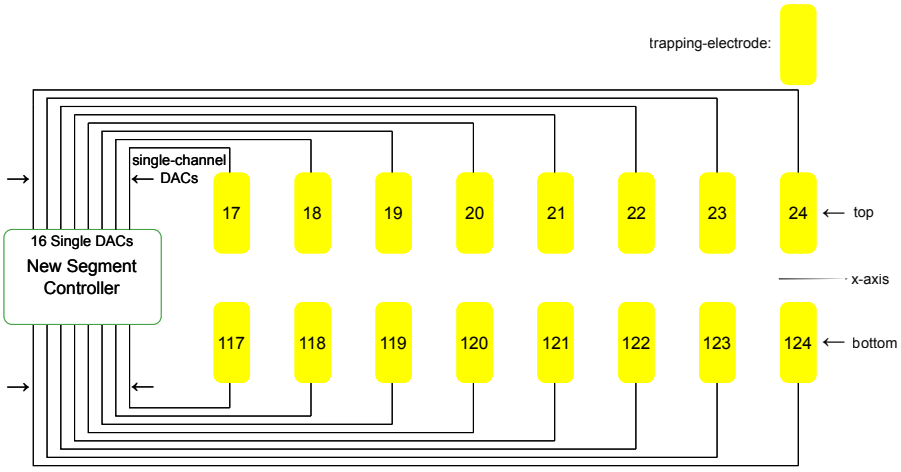
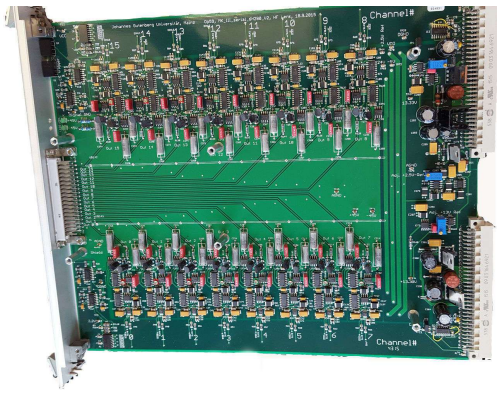


Fig. 4.4 The routing layout of the analog channels of new analog card (see Fig. 4.5a) which is used in new segment controller (see Fig. 4.5b). The layout idea of this analog card connects four top and bottom trapping-electrodes with dedicated independently controllable channels. The group of channels connected to top and bottom electrodes are addressed as north and south group respectively. A total of eight analog-voltages are provided by each of the groups of analog cards. Please note that the intermediate low pass filter used between electrode and analog channels has not shown in the figure, although it is always present.

While the digital modules buffers these digital data for faster switching of connected load (also compatible for 50 Ω). Simultaneously, digital data from external measurement devices can also

(a) New analog card



(b) New segment controller (Bertha)

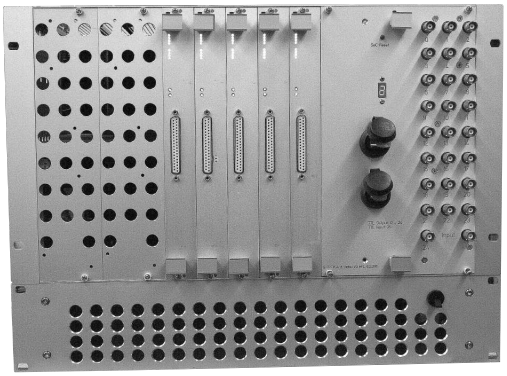


Fig. 4.5 Newer analog card and newer shuttling hardware (N_Bertha or mAWG) housing for supporting 80 analog voltages and 24 TTL signals. **(a)** New analog card that supplies DC-voltages to 16 electrodes of the segmented ion-trap with on-boards available 16 analog channels using Sub-D 37 connector. Every channel has a voltage range of ± 40 V and are independently controllable. One or more channels can also be used at same time (simultaneously). **(b)** New segment controller (N_Bertha) houses five analog cards, therefore eighty parallel analog channels are available for shuttling operations and twenty-four digital TTL signal for shaping the laser-pulse for qubit manipulation inside the segmented ion-trap. The figure (b) shows fully populated N_Bertha with five analog cards (left side in their respective slots with SUB-D 37 connector) and BNC connectors (right-side) for providing digital TTL signals.

be received by an internal SoC-FPGA module and recorded in memory by FPGA sections. The recorded data is written to an internal cache and later moved via the central memory to the host PC or further evaluated on the Zynq.

An overview of the general specifications achieved by the mAWG is given in Table 4.1. More detailed specifications for the individual modules currently in use with mAWG are given in the following sections.

4.2.1 SoC-FPGA module

We employ a Xilinx Zynq-7000 SoC ZC702 Evaluation Kit, which provides the ZynQ-SoC, memory, and Ethernet interface, as the central control unit, mainly relevant from our developed design perspective. It has XC7Z020 Zynq chip, which is empowered by a dual-core ARM Cortex A9 667 MHz CPU and an Artix-7 FPGA with 85000 programmable logic cells. The SoC-ZC702 evaluation board features a total of 1 GB DDR3 memory, a 1 Gb/s Ethernet connec-

Characteristic	Value	Unit
internal digital lines	132	
max internal clock rate	400	MHz
signal clock rate	50	MHz
sample hold time resolution	20	ns
max. data transfer rate	730	MBit/s
sequence memory	900	MB
min. sample update time	360	ns
max. number of analog channels	80	
output voltage range	$\pm$ 40	V
analog resolution	1. 2	mV
slew rate	20	v/µs
noise floor	<100	µV

Table 4.1 The internal specifications of N_Bertha (mAWG), which are fundamental to system as these are used for controlling the digital and analog modules associated with it.

tor and corresponding controllers, multiple USB connections, a total of 200 digital in/outputs, onboard flash memory and other components. Other FPGA chips feature significantly more freely configurable I/O pins and other device resources, but a memory, Ethernet and USB controllers will use most of these resources. The Zynq system uses ARM cores and software drivers to interface external controllers with the SoC. If similar design implements in a purely FPGA based system, multiple complex Intellectual property (IP) cores would be required to provide the same functionality and also use up a significant portion of the total available logic cells.

Communication between Zynq and host computer is established using an Ethernet-based TCP/IP connection utilizing on-board Ethernet controller and managed by an ARM core. The available USB connections are used to upload the drivers and software running on the ARM core and also to program the FPGA logic cells. During operation, data sequences are sent to the Zynq, exclusively using the 1 Gb/s Ethernet connection, which was optimized for low latency ($<$1 ms) and high throughput ($>$750 Mb/s). This ensures that experiments requiring multiple long data sequences, exceeding the 1 GB on-board memory, can be executed in efficient way. The mAWG system can also be used for processing photon detection data in order to determine logical states of trapped ions. Making use of the low latency connection, sequences featuring conditional branching can be deployed in the Zynq memory, e.g. for realizing error correction sequences.

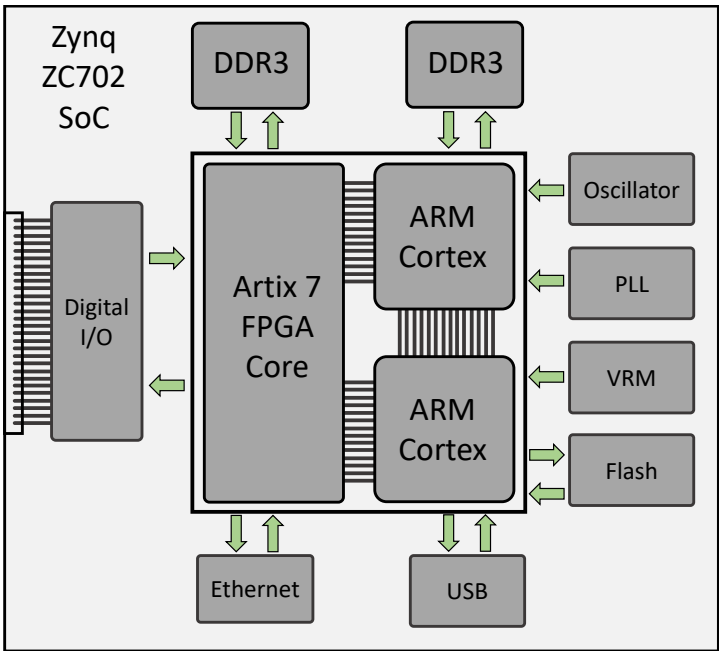


Fig. 4.6 Simplified overview of the Zynq ZC702 SoC evaluation kit showing the relevant on-board controllers and components. The connections between the SoC and external on-board components are illustrated.

On the host computer, an in-house developed control software (MCP) is interfacing with all connected devices of the experiment, including the mAWG. The MCP is a GUI wrapper capable of executing several C++ programs in parallel. It generates data for various ion shuttling operations using different precompiled library modules. The mAWG uses data sequences in binary format and outputs the digital signal at bounded I/O ports of SoC-FPGA. The binary data are directly converted by the DAC modules to produce the requisite analog voltages level. Additional execution control commands allow self-triggered sequencing by preprogrammed time-span, looping of a sequence and wait-for-trigger from external source (syncing to external triggering eg. ac line sync).

Making use of the highly configurable nature of the Zynq, future developments will focus on implementing a more advanced storage and control system for the experimental sequences. The newer storage scheme will introduce splitting methodology for redistributing a large sequence into sub-sequences for each analog and digital output channels. And the control system will enable the controlled streaming of data sequences in real-time. Besides storing longer and more complex sequences, this will make it possible to perform conditional branching without requiring further information exchange from the host computer. It will enable the possibility to hand over the entire experimental control to Zynq, while the host computer still has full access

to the individual sub-sequences and manage the stored sequence record if needed. The general information exchange is equivalent to data exchange with longer latency as of Ethernet based communication.

4.2.2 Backplane and digital output modules

The binary digital data generated on SoC-FPGA is redirected to analog module for voltage generation via a custom developed backplane. Zynq, I/O connections, are directly connected to the back-plane via an adapter-board which translates tiny high-density pin-connector to a coarse compatible connector (see Sec. C.1). It distributes various digital signals of SoC to analog output modules and digital output modules. The back-plane receive signal for analog output modules. There is no signal processing or conditioning on the backplane. Therefore, the back-plane is engineered to process digital data and clocks signals into a format usable by the DACs. As part of this, the data and clock signal timings are adjusted to ensure the tight timing constraints of the DACs. Multiple active components are therefore used on the backplane to distribute the main clock, more specifically buffering clock drivers, from one incoming signal to all connected analog modules and their corresponding 80 DACs. The issue of timing errors of this clock can also be addressed by using a clock delay circuit, which can be manually adjusted for the macroscopic delay. However, the actual delay is adjusted using software timing-constraint during design development.

Digital signals are not distributed directly to multiple output channels but buffered, which helps in correcting any timing mismatch between digital signals of clock and data as well. It also allows for the adjustment of digital voltage levels. The incoming digital signals from the FPGA is 0-3 V level transmission standard, so the level is amplified to 0-5 V level before feeding into the DACs.

After processing data and clock signals on the backplane galvanic isolators are used to separate the grounds of Zynq I/Os and the DACs. These isolators help in preventing the ground loop, accidental noise leakage from the digital signal processing and Zynq into DACs and also help in protecting the FPGA from voltage surge that might occur if one of the analog output channels is damaged.

Connections between the Zynq I/Os (via high density pin-adapter) and digital modules do not require any processing or galvanic isolation. The digital I/O modules are connected to I/Os of the FPGA via the adapter, without the use of any active components. Galvanic isolation and

level translation buffers are placed on the digital I/O modules that electrically separate 5 V TTL mAWG output or input stages from the Zynq. The function of these isolators is identical to the previously described ones. As the digital-I/O modules have very few active components between module I/O and Zynq I/O stages over-voltage and electrostatic discharge protection provided by the galvanic isolators is even more crucial.

Input and output ports of the digital module are used to control laser pulses, readout of a photon counter and general triggering purposes in the lab. Each module features 24 digital outputs and two inputs with a maximum update rate up-to 50 MHz (20 ns), however internally concurrent logic can also be used for faster realization. Also, two input channels can be used for high-speed input signals, such as pulses generated by a photo multiplier tube (PMT) and external triggering for synchronizing the experiments to any desired source (For, eg. ac line sync) respectively.

4.2.3 Analog output modules

Analog output modules are used to convert the incoming digital data of the Zynq, which are processed on the back-plane into analog output voltages. The multiple stages of the analog modules allow for a high current $\pm$ 40 V output range on all the channels. Design decisions for the used components are based on the requirements of performing fast shuttling operations and also confining the ions during quantum operation. Based on these operations the following criteria were set: Voltage update rate of $\geq$ 2 MSPS, the voltage range of $\pm$ 40 V, an accuracy of 16 bit, the stability of at least one least significant bit (40 V / 16-bit), and lowest possible voltage noise.

An outline of the analog modules, shown in Fig. 4.7, gives a schematic of the individual components used for the analog output modules.

The component with utmost significance on the performance of analog output modules is DAC. The Analog Devices model (AD5541) was chosen based on its optimal technical feature which were significant for performing low heating shuttling operations. Some relevant figure of merits are 2. 5 mega samples per second (MSPS) using SPI interface, its low noise voltage output 11.8 nV/$\sqrt{\text{Hz}}$ and 16-bit resolution with a relative non-linearity accuracy of $\pm$ 0.5 least significant bit (LSB). Faster DACs with comparable noise and accuracy are available, but they may require either parallel interfacing of data-line or kind of packaging which might not be easy for debugging. The parallel interface will enhance the data-line requirement by

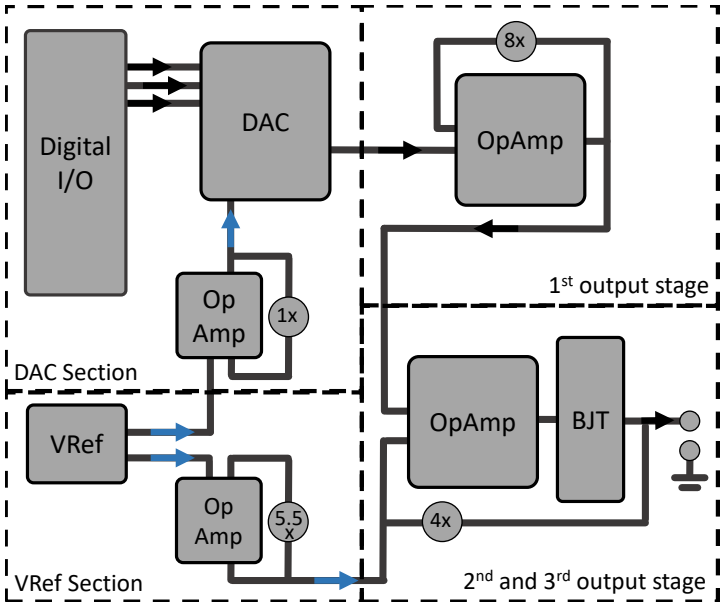


Fig. 4.7 Essential components of a single analog output channel. The DAC section features an AD5541 DAC supplied with data by digital hardware and a reference voltage supplied by the VRef section, buffered by an OpAmp close to the DAC. The 1st output stage yields a 8x voltage amplification, followed by the 2nd and 3rd output stage which amplify the voltage further by a factor of 4 and perform a level shift. It contains bipolar junction transistors (BJTs) to increase the maximum output current.

16-times. Supplying 80 DACs would require nearly 1300 data output channels and leading to a considerable increase of complexity of the entire device. Other mAWGs used for control of trapped ions [Bai+13; Bow+13] feature parallel DACs, allowing for higher update rates, but require a more significant number of FPGA controllers for a similar or lesser number of analog outputs. For the intended operations being performed with this mAWG, the 2.5 MSPS update rate is sufficient.

Four signals are needed for programming the DAC using SPI interface. They are data, chip-select or channel select (also called as word clock), clock and load lines. The start of chip-select line initializes the shift of incoming data signals by the DAC. For reducing required digital I/Os, four DACs are grouped and supplied using same word-clock, clock signal but different data line for each of the DACs. The update timing is same so even if the voltage on one of the channels is changing other channels of this group is refreshed with the same voltages. The load-line is tied to active-high always, which reduces the need of any load line and hence there is no digital line dedicated for load lines. The end of the chip-select enables the outputs at their ports. By not using programmable load-line, eighty digital I/O resources of

SoC-FPGA are saved.

One analog output module is equipped with sixteen DACs[3] which receives sixteen identical clock derived from same clock-line, sixteen independently programmable serial data-line and four chip-select lines through the back-plane. Chip select is required for the DAC to move serial data into the shift register of the DACs and enable the output, therefore it can be used to turn off voltage updates on selected groups of four DACs. Output range of the DACs is set to 0–2.5 V by a reference voltage, which is generated by a central voltage reference circuit[4] and consecutively buffered at each DAC using an operational amplifier.

Output voltages of the DACs require further amplification and the uni-polar range needs to be extended to achieve the necessary bipolar ± 40 V range. Also, the system should also be able to supply limited inrush required current for the connected devices. Although, the analog modules of the mAWG is designed for supplying voltages for the electrodes of an ion-trap Fig. 4.3, which has low capacitive and large resistive impedance, large currents are required during ramping of the large voltage range using a low pass filter close to the switching frequencies. This features is prevalent when operating an QCCD for performing shuttling and quantum operations as well.

The amplification output stage consists of three sections, preamplification with a gain of 8x, a level shifting and final voltage amplification with a gain factor of 4x and the current buffering with unity gain. The first stage makes use of a typical op-amp circuit with an Operational amplifier (OpAmp)[5] and a resistor array to achieve the stable gain level ensuring that the current drawn from the respective DAC is low. Despite the high gain of 8x, this amplification stage maintains a broad bandwidth of more than 3 MHz with a slew rate of 20 V/µs. The OpAmp[5] adds additional $\sim 8\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ noises at the input of the existing noise of the signal coming from the DAC. A factor of 8x will then amplify the total noise, which will also include noise from clock signals bleeding through, glitches from switching voltages and Johnson noise stemming primarily from the used resistors, putting the lower noise limit of the signal to $\sim 160\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at this stage.

The second stage uses a specialized OpAmp[6] , which features large rail to rail voltage amplification up to ± 70 V. The analog module does level shifting before amplifying the input

[3] AD5541A (Dev18)
[4] ADR441
[5] AD8510ARZ (Dev17)
[6] LTC-6090

signal further by a gain factor of 4x. The level-shifting is accomplished using the onboard voltage reference and equipping each channel with a trim resistor to adjust the voltage offset, therefore ensuring a suitable symmetric bipolar output. Although, it offers high output voltage range with the slew rate of 20 V/µs and $<$2 MHz bandwidth during voltage swing within $\pm$40 V range. The specified input voltage noise of it is $\sim$14 nV$/\sqrt{\text{Hz}}$, which adds to the floor-noise of $\sim$160 nV$/\sqrt{\text{Hz}}$ on the signal after the first amplification stage. The upcoming section has discussed the new noise floor after all these amplification stages. But, these noise characteristics set the lower limit to $\sim$700 nV$/\sqrt{\text{Hz}}$.

The output signal is finally buffered using a matching set of complementary bipolar junction transistors to match inrush current demand if any. These are placed in a push-pull output driver configuration with unity gains and inrush current up to ~2 A. The output of this final stage is used by the second stage as feedback, ensuring any deviation from unity gain is corrected for by the previous op-amp. This push-pull transistors of current-amplification stage is limited supply an output power of 2 W and is intended for low capacitor charging and discharging. This is designed to drive filter circuits during faster update of waveform while performing ion shuttling operations.

Each analog output module features 16 output channels, which are meticulously designed to prevent onboard cross-talk between the analog channels. For translating the fast updating analog signals to the trap-electrodes, custom-made co-axial twisted cables are used. More details on the custom-made wiring and filtering for the analog outputs are provided in see Appndx. D.

Performance of the analog cards

In the following section, the frequency and time domain performance of analog channels of mAWG are discussed. The frequency domain analysis mainly focuses on spurious free dynamic range (SFDR) and the noise behavior in the frequency ranges relevant for the ion traps, while discussion in time domain includes voltage stability, non-linearity errors, general glitch impulse area (GIA), slew rate and settling time. Although, results of single channel has been discussed here, nevertheless similar results has been measured for all the channels. No discrepancies in the general performance of any two channels has been seen so far.

Frequency domain analysis

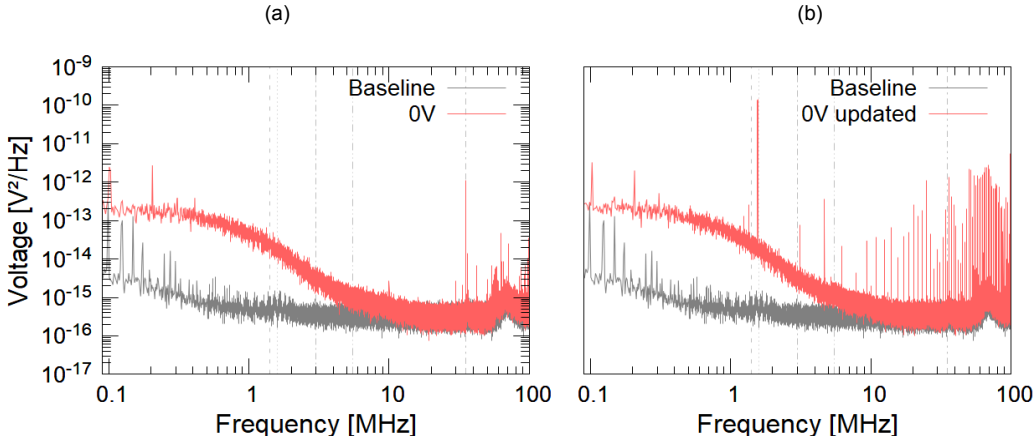


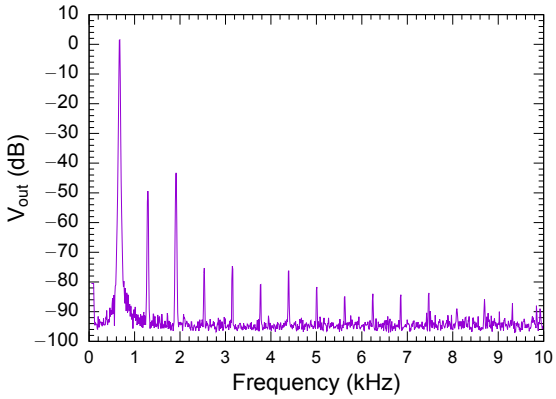
Fig. 4.8 The general noise spectrum of any analog channel in mAWG, which has been measured using Anritsu MS2781B spectrum analyzer. (**a**) The black noise spectrum is the baseline measurement which is measured for noise floor level and calibration. An active probe connected to the spectrum analyzer only, is used for this. While red spectrum is measured with DAC set to 0 V. (**b**) The baseline measurement remains same while 0 V is continuously being updated at analog channel.

Noise measurements were measured with spectrum analyzer[7] which has a frequency measurement range of 100 Hz–8 GHz and a bandwidth resolution of 10 Hz. Displayed average noise of the spectrum analyzer is on the order of -167 dBm. The spectrum analyzer was used in combination with an active probe[8], compatible for a frequency range of 5 Hz–500 MHz. The active-probe has a 3 pF input capacitance and 100 kΩ input resistance, which ensures that the measurement equipment itself does not load the measured analog signal. The frequency response of the active probe in this range is independent of the input frequency.

To establish a baseline of the noise spectrum, input noise in range of 1 kHz–100 MHz spectrum was measured with the active probe attached to the spectrum analyzer input. In combination with the measured noise baselines, multiple spectra were recorded for 0 V voltage output from the mAWG with and without digital updates at DAC input, as shown in Fig. 4.8 (a). At 0 V the analog DACs and first amplification stage are at half scale output and are not expected to perform better or worse compared to other output voltages. Generating a static voltage without digital updates represents an ideal case for low noise performance and can be used to confine ions during gate operations. Outputting static voltages with constant digital updates of the same digital data is a common case when some voltages are kept static, and

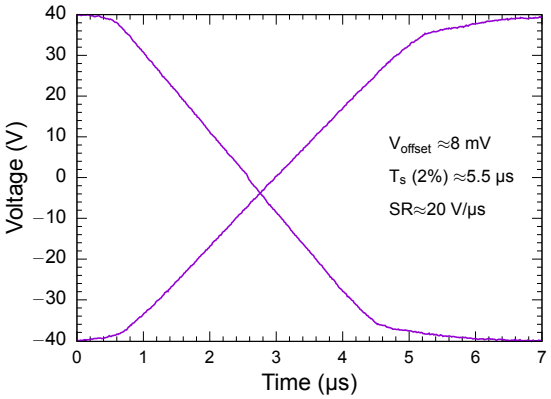
[7] Anritsu MS2781B
[8] Agilent 41800A

(a) SFDR



(a) The SFDR measured using 625 Hz signal generated by DAC[3]. The updating digital signals at 50 MHz are used to generate a sinus signal (Amp.=5 V pk-pk) with 4500 samples. The instrument is first normalized with 10 dB attenuation then the generated sinus signal is measured. The bandwidth of this instrument[a] was limited 1.5 GHz, so measurements in the Hz-region are prone to frequency offsets.

(b) Slew rate and settling time



(b) General slew rate and settling time of either of the analog channels. Slew rate of 20 V/µs and max. settling time of 5.5 µs within 2% of end to end swing voltage ±40 V have been measured. For smaller voltage steps, settling time is faster [Dev18].

[a] HP8568 spectrum analyzer

others need to be switched for shuttling. Digital updates need to be sent even if the voltage is kept static since multiple DACs share a chip select channel. Noise spectrum for this case including the baseline is shown in Fig. 4.8.

Noise baseline and measured noise show a significant increase in the lower frequency range, which is expected due to flicker noise, which follows a $\frac{1}{f}$ behavior combined with Johnson noise stemming from the input resistances. Johnson noise is frequency independent but a $\frac{1}{f}$ behavior is expected when using an active probe, since the ohmic resistance diminishes with higher frequency due to the frequency dependency impedance of the capacitor placed in parallel with the ohmic resistance. Furthermore additional noise peaks at 100 and 200 kHz can be seen in the recorded output voltage noise, which can be explained by the use of multiple switch mode power supplies in the vicinity of the measurement setup. At higher frequencies, above 30 MHz, a clear increase in the baseline and narrow signal peaks can be seen due to commercial frequency bands range used for various applications.

Both noise measurement spectra in Fig. 4.8 show a significantly higher noise floor on the order of $\sim 3\,\mu V/\sqrt{Hz}$ in the lower frequency region below 1 MHz which declines and matches the noise baseline, on the order of $\sim 31\,nV/\sqrt{Hz}$ close to 10 MHz. DACs in combination with op-amps are expected to contribute at least $700\,nV/\sqrt{Hz}$ of noise which declines in frequency range beyond the bandwidth (2 MHz) of the op-amp used in the amplification stages. At low frequencies (1 kHz) the reference voltage circuit will increase the minimum noise floor to $> 2\,\mu V/\sqrt{Hz}$, which is further increased by resistors and other components like external linear power supplies. At higher frequencies these contributions diminish as flicker noise follows a $\frac{1}{f}$ behavior and Johnson noise will also be less due to the decreased impedance of the capacitive-reactance in the circuit.

When digital signals for the same voltage are sent rest of three DACs in the group, the noise spectrum exhibited by the analog updating channel is shown in Fig. 4.8 (b). It generates several harmonics in the frequency spectrum. These harmonics has no relevance in the experiments as they are well attenuated by the low pass filters (see Sec. D.6). The digital signals at the DAC input ports always updates with static clock frequency so secular frequencies are also generally adapted to avoid these harmonics.

The amplitude of these harmonics can be quantified through SFDR measurement. For this, a sinus waveform of frequency 625 kHz and amplitude 5 V with 5000 analog sample has been generated by one of the DAC, while rest of three DACs were being updated with 0 V (see Fig. 4.9a). The instrument[9] is first normalized with 10 dB attenuation and static voltage of 0 V. Then, SFDR of 50 dB has been measured between carrier and its worst harmonics, which is second harmonics in the frequency spectrum. The bandwidth of this instrument was limited 1.5 GHz, so measurements in the Hz-region are prone to frequency offsets.

Time domain analysis

Slew rate

One of the critical parameter is the real world slew rate capabilities of the system, which will put a limit on how fast a full-scale voltage swing can be achieved. Such a full 80 V voltage change was recorded using the oscilloscope and is shown in Fig. 4.9b.

Maximum slew rate reached was 20 V/µs, which is limited by OpAmp[6] used at second amplification stage. Other components of the analog output stage do not impose further re-

[9] HP8568 spectrum analyzer

strictions and the OpAmp can reach maximum specified slew-rate. At the beginning and end of a full voltage swing, as can be seen Fig. 4.9b, the slew rate is limited, which is caused by build is trim capacitors, required to prevent overshooting and ringing under normal operation. Slew-rate reductions do not occur for smaller voltage swings. Full scale voltage swings are not commonly used when shuttling ions and the amplification stage is therefore not recommended for end to end voltage swing however if needed there is no harm in using for experiment specific needs. Slew rate is a critical parameter for the shuttling of ions as it limits the speed if ions being transported from one electrode to the next. Due to the use of filters, the slew rate is also of critical importance when employing a software correction for the distortion caused by these filters.

The main instrument for determining long-term voltage stability, non-linearity and voltage accuracy was high precision digital multimeter from Agilent[10]. Different voltage-range of multi-meter was changed dynamically from $\pm$100 mV to $\pm$100 V for measuring the voltage (voltage range of $\pm$40 V) of mAWG. For lower voltage range, stability of voltage was measured with 100 nV accuracy and the expected noise floor of the multimeter of 3 nV well below the resolution limit of (1-LSB). While in upper voltage range, the instrument measures the voltage with an accuracy of 100 µV and a noise floor well below that.

INL and DNL

Non-linearities at the output of the DAC and at amplification stages can cause inaccurate voltages, which cannot be corrected by adjusting the digital waveform data. DACs have inherently integral non-linearity (INL) and differential non-linearity (DNL) . Therefore, the measurement for quantifying non-linearity errors should also include the inaccuracies added by amplification stages, therefore, the figure (see Fig. 4.10a and Fig. 4.10a) shows INLs and DNLs of the entire mAWG system. DNL of the system is shown in Fig. 4.10b (a) and within the expected values of 1-LSB (LSB equals 1.2 mV) mostly below $\pm$0.5-LSB. This shows that even with two-stage amplification in the analog module, the analog voltages are monotonic and there are no missing codes. Since DNLs are caused by non-absolute resistor values and therefore not an exact step of 1 LSB between subsequent output voltage at the amplification stage is expected. Hence, the final stage does not show any significant effect on the DNL when expressed in LSBs. These small deviations are reproducible which shows an absence of any external drift, therefore it should not affect trapping storing or shuttling ions any further. The output voltage will not be exactly as intended but regular calibrations of the ions relevant transition frequencies using

[10] Agilent 34411A 6.5 (Tec17)

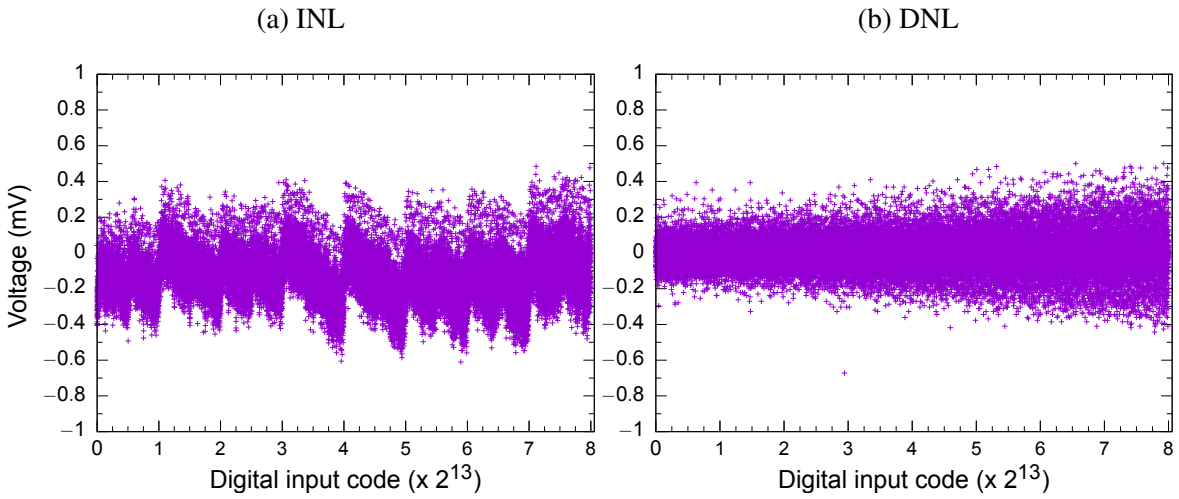


Fig. 4.10 Non-linearity errors of analog channels. **(a)** DNL and **(b)** INL are the non-linearity error measurements of a analog channel. This measurement has been done at the final amplification stage (see Sec. 4.7). The measured non-linearity errors are always <1-LSB, which imply that the voltage will be stable within the resolution limit of 0.0012 V.

external inputs, like frequency tuning of the lasers these minor misalignment are of no further relevance.

Integral non-linearities (INL) of the DAC cannot be measured independently of non-linear gains in the amplification stages and are therefore measured for the entire mAWG system. INL is defined over the entire output range and caused by nonlinear gains or other factors that vary across the DAC chip, for example varying dopant levels, voltage drops, length of diffusion, oxide thickness gradients thermal gradients or similar effects in the active components of the amplification stages. As shown in Fig. 4.10a, INLs and DNLs of the entire system INL are well within one LSB, correction is not possible using a software calibration and similar to the DNL other experimental parameters can be used during calibration runs to negate these minor non-linearities.

Glitch

Measurement of fast non-periodic distortions of waveforms like a voltage glitch occurring during a DAC output change is ideally achieved using a high-speed oscilloscope. We used an MSOX3104A mixed signal oscilloscope with a measurement bandwidth of 1 GHz and a maximum voltage resolution of 8 bits (12 bits using averaging) and voltage accuracy of 0.6 mV. The limited resolution and accuracy make the oscilloscope unsuitable for noise analysis

but are sufficient to investigate glitches caused by DAC output changes and also for determining slew rates. The GIA is measured in nV-s.

Glitches occur whenever the DAC switches from one voltage output to another. For many voltages switches the glitch is very small or not even visible when recording the output voltage on the oscilloscopes. When a significant amount of bits are switched for example the most extreme case of switching all bits of the 16-bit DAC output at once a big glitch occurs as can be seen in Fig. 4.11.

In general, a voltage GIA is observed when flipping of MSB causes the flipping of all lower bits (e.g. 0x7FFF_h $\rightarrow$ 0x8000_h), but in our case we observe these glitches at two instances. Beside the standard glitch, another GIA during the switching of lower significant bits has also been observed (see Sec. 56). The magnitude of standard glitch which occurred during switching of MSB are 7 nV-s (voltage transition of 0 V to 0.0012 V (0x8000_h to 0x7FFF_h)) (see Fig. 4.11a) and 5.7 nV-s (voltage transition of 0.0012 V to 0 V (0x7FFF_h to 0x8000_h)) (see Fig. 4.11b). While unconventional GIA (see Fig. 4.12) of magnitude 12.5 nV-s (for change in DAC input from 0xXX0X_h to 0xXXEX_h) (see Fig. 4.12a) and 35 nV-s (for change in DAC input from 0xXXEX_h to 0xXX0X_h) (see Fig. 4.12b) have been measured. X denotes any arbitrary bits. More information of non-conventional glitches is dicussed in Sec. 56.

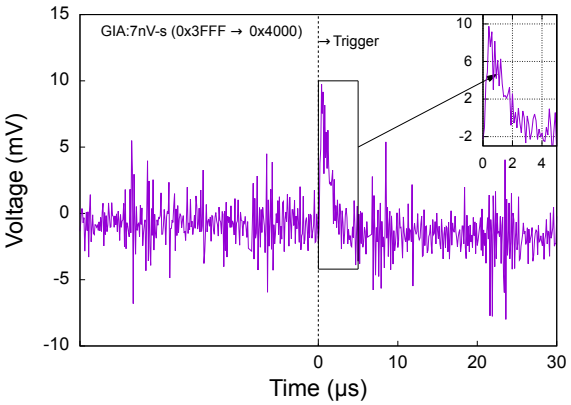
This is caused by many current sources switching at the same time and overshooting of inbuilt amplification stages, which can't be filtered entirely using passive components. However, a sample and glitch hold circuit can be used for designing a precision DAC system which would be free from glitches but this will require additional electrical components on the analog PCB cards. This is not feasible due limited space which is mainly used by DAC and it's amplifying stages.

Voltage drift

Using the digital multimeter voltage stability of the analog output was recorded over a period of more than 160 min every second and is shown in Fig. 4.13a. Measuring once per second ensures the multimeter reaches nearly the optimum accuracy due to averaging of power line cycles. As can be seen in Fig. 4.13a the mAWG output voltage features a small slow voltage drift on the order of $\pm$ 50 µV over hours and short time fluctuation $\pm$ 200 µV on a time scale of 1 sec.

The presence of initial offset is inevitable for any electrical design, but lower and stable offset are keys to a precision voltage source. The figure shown in Fig. 4.13b shows general

(a) GIA for transition of DIC from 0x8000 to 0x7FFF



(b) GIA for transition of DIC from 0x7FFF to 0x8000

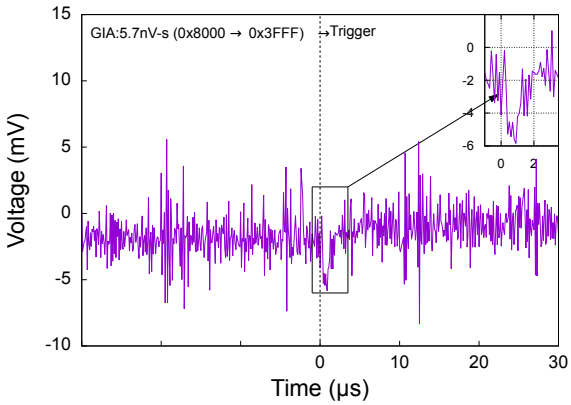
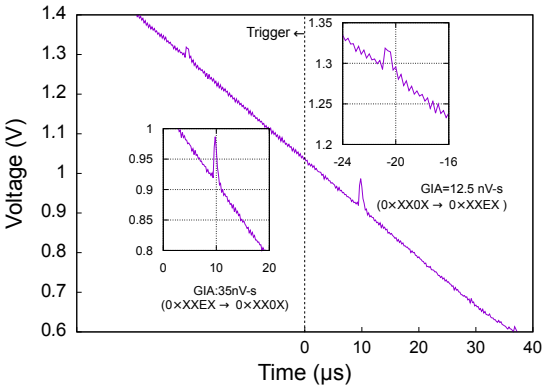


Fig. 4.11 GIA measured during the transition of MSB **(a)** GIA=7 nV-s has been measured during voltage transition of 0 V to 0.0012 V (0x8000_h to 0x7FFF_h). **(b)** GIA=5.7 nV-s has been measured during voltage transition of 0.0012 V to 0 V (0x7FFF_h to 0x8000_h).

(a) Bumps: Rising of glitch amplitude during increasing DAC output



(b) Dips: Lowering of glitch amplitude during decreasing DAC output

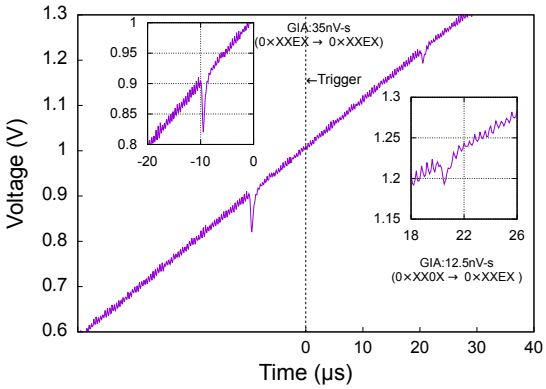


Fig. 4.12 Glitch observed and measured during the change of lower significant bits (4^{th} significant bit). The magnitude of smaller and larger glitch are 12.5 nV-s (for change in DAC input from 0xXX0X to 0xXXEX) and 35 nV-s (vice-versa) respectively. This type glitch has a rising amplitude (**(a)** Bumps) if the output of DAC has increasing slope while lowering (**(b)** dips) amplitude is seen at decreasing output of the DAC.

offset-pattern of analog channels of the analog cards. These pattern is seen due to non-accurate capacitance used with the reference power-supply of the DAC and their amplification OpAmp. Offset variation up to $\pm$20 mV has been measured in the analog channel of any analog cards.

(a) Voltage drift

(b) Variation of offset error

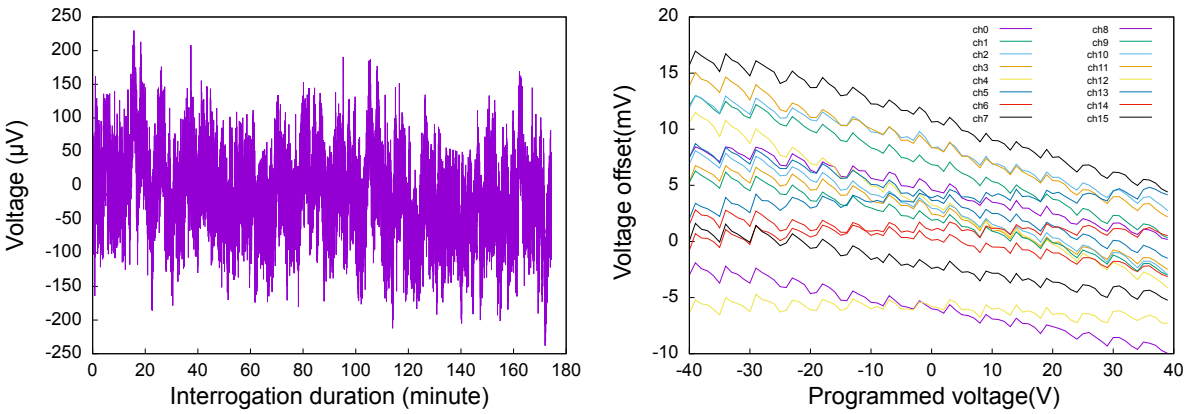


Fig. 4.13 Long term voltage drift of a channel and general pattern of initial voltage offset at all the channels of a analog card. **(a)** A programmed voltage at a analog channel remain stable for $\geq$ 3-hrs with accuracy of 50-100 μV, well below resolution limit (1.2 mV). **(b)** Offset analysis for all 16-channels of the analog card at multiple voltages in the range of $\pm$40 V varying in the step of 1 V. Although it is a board specific measurement, the range of offset is similar for all the cards. The upper limit derived from the offset measurement on several (50) analog cards is $\pm$20 mV.

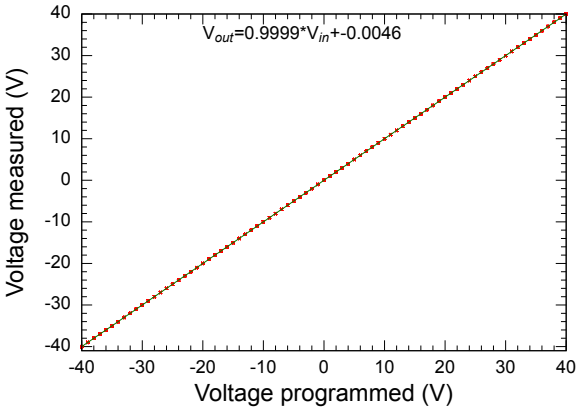
None of the analog channels of any cards has shown deviation from this pattern. These offset are static in nature, hence, does require calibration during the experiments.

Fluctuations on times-scales well below the secular frequencies will not cause heating to the ultra-cold trapped ions. But excessive slow fluctuation will negatively impact the quantum gate performance due to changes in the position with respect to the applied laser fields therefore leading to fluctuations of the laser intensity. The most critical operation is separation of ion from two-ion crystal, which require the consistency in voltage within the resolution regime (~1 mV). The drift in voltage stability or offset will lead to ion-loss in shuttling based experiments.

The performance report of mAWG analog channels in time and frequency domain has been summarized in Tab. 4.2.

In conclusion, the analog channels are generally used with low pass filters ($\leq$100 kHz). Therefore, the update rate beyond 1 MHz would be underutilization of resources in our case. As low pass filters are essentially needed for performing advance shuttling operations with preserved quantum state of ions, so the channels are designed for driving these filters

(a) Relative precision of Analog channel



(b) Programmed and measured voltage difference

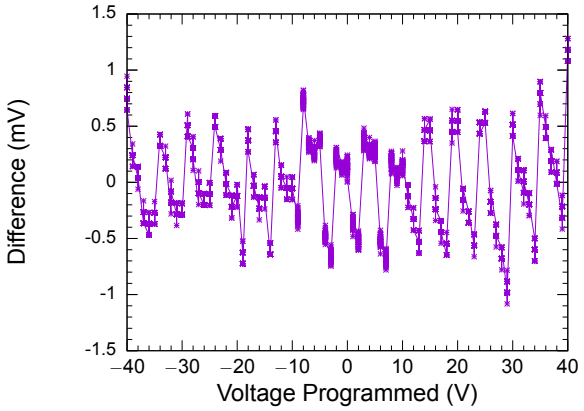


Fig. 4.14 Precision of randomly chosen analog channel. **(a)** The general output of randomly chosen analog channel (red dots) has been plot against generalized transfer function averaged from 5 analog cards (green line, 80 channels). The fit transfer function has a slope of 0.999(1) with the offset of 0.0046 mV. **(b)** The general difference (green-line and red-dots of **(a)**) of generalized DAC linear transfer function (expected voltage) and measured voltage, such plot has been observed for all the channels in several analog cards, a maximum variation of $\approx \pm 1$ mV has been measured.

Characteristic	**Value**	**Unit**
Noise level static output 1-30 MHz	730	$\mu V//\sqrt{Hz}$
Noise level output update 1-30 MHz	730	$\mu V/\sqrt{Hz}$
Noise level signal output 1-30 MHz	900	$\mu V/\sqrt{Hz}$
Integral non linearity	0.6	LSB
Differential non linearity	0.6	LSB
Max. GIA	35	nV-s
Slew Rate	20	V/s
Voltage Stability	± 200	μV

Table 4.2 Noise summary report of the scalable segment controller shuttling hardware (mAWG).

also. Each of these channels, is capable of supplying ~100 mA current to drive the load, while maintain exceptional voltage integrity (see Sec. C.4). The analog channels are slow (~400 ns) and might eventually appear as not right choice for shuttling based quantum operation, in contrast, the mentioned update rate of analog channel, time-resolution (dwell time limit) of 20 ns, and voltage resolution of 1 mV along with tested noise as figure of merit, N_Bertha is optimally performing advanced fast shuttling operations in the lab.

5

Advanced shuttling operations

5.1 Introduction

Making use of the newly developed, scalable voltage resources, mAWG (Chapter. 4) and the characterized experimental qubit operations (Chapter. 3), it was possible to experimentally realize multiple shuttling operations ranging from linear transport to separations and swapping. These operations and their effect on the motional state of the ions were characterized in detail and will be discussed in this chapter. First, general heating of all modes in standard linear transport of ions will be discussed. Followed by separation induced motional heating demonstrating how faster transport can lead to less motional excitation. And finally I will investigate crystal swapping performed with two-ion, three-ion and four-ion crystals and the resulting motional excitation. Compared to previously reported results [Wal+12; Rus+14; Kau+17] the new mAWG allows for higher voltages, which results in higher axial secular frequencies and therefore a higher cut-off frequency filter set can be used. Experimental results presented here involve higher voltages, higher cut-off of low pass filters (see Sec. D).

5.2 Advanced shuttling operations

In the 3D trap used for shuttling operations presented in this chapter, 64 electrodes constitute 32 arrays of Paul traps. During shuttling operations single or multiple ions are moved mostly in axial direction by changing voltages applied to at least four DC electrodes in time. For e.g. starting with a negative trapping voltage applied to segment n and all other segments at 0 V, when we ramp the voltage at segment n to 0 V and ramp the neighboring segment $n+1$ to a negative voltage, the electrostatic potential well will shift along the trap axis, from Seg. n to $n+1$.

Significant work goes into finding the optimal voltage waveforms to perform specific shuttling operations, which allow for fast shuttling which could result in minimal motional excitation. Some optimization process will be discussed and results presented in the following sections. The entangling gates and readout are only sensitive to transverse motion, therefore, the predominantly axial excitation during can be tolerated to some extent.

However, excessive axial excitation amplitudes are to be avoided, as there is residual coupling to axial motion throughout gates and readout, anharmonic coupling between axial and transverse collective modes and large axial excitation can also render separation/merging operations unreliable. Large oscillation amplitudes in axial direction comparable to laser focus size can also lead to undesired intensity modulation during gate operations. Furthermore, the trap geometry is non-ideal, i.e. not entirely uniform and symmetric. Therefore, shuttling along the trap axis also leads to parasitic transverse excitation.

The excitation caused by shuttling operations is commonly larger in the axial mode as the ions are accelerated in axial direction and also have to be decelerated again. Furthermore, the transverse frequencies remain unchanged during transport process while the axial confinement usually varies, which can lead to additional excitation.

In this chapter following shuttling operations will be discussed, optimizations and resulting motional excitation presented:

- **Linear transport:** Movement of single ions or small ion crystals along the trap axis. This operation is explained in Sec. 5.2.1.
- **Separation/merging:** Ion crystals are split into single ions and/or smaller crystals, or the reverse process is carried out. This operation is explained in Sec. 5.2.2
- **Swapping:** Physical swapping through rotation of ion crystals. The ability to carry out this process can have a significant impact on the performance of architecture. This operation is explained in see Sec. 5.2.3.

These shuttling operations are essential building blocks of a quantum processor node making use of laser interaction and memory zones, similar to the one proposed by Kielpinski et al. [KMW02]. The trapped ions encoded with the quantum information are stored in the memory zone, that can transported in parallel to the multiple processing zone for simultaneous execution of multiple logic gate operations [KMW02; DJ+]. Time scale of these operations has to faster or comparable to that quantum logic operations (~10-100 μs), so that the ions can be

transported back before loss of encoded quantum information [Mon+11]. Therefore, a large focus of the optimization presented here, besides minimal motional excitation will also be on the improvement of shuttling speeds.

5.2.1 Advanced linear transport

Linear transport is the basic shuttling operation, which is performed for the characterization of all operations including separation and merging and swapping. Therefore, it is essential that linear shuttling is well optimized and the influence of this transport on the motional excitation is well-known, serving as a baseline. To characterize all transport operations the ion or ions have to be transported to the laser interaction zone (LIZ) to determine the motional excitation (see Sec. 1). The exact location of the LIZ in the trap can be chosen relatively freely (it can be altered to fit the requirement of experiment-specific shuttling operation) and is currently positioned at the location of electrodes 19 and 119 ("1" is used to identify opposite segment). Similarly, for neighboring (Seg. 20 and Seg. 21), there exist an electrode Seg. 120 and Seg. 121, and so on. Both top and bottom electrodes are controlled independently by voltage outputs of the mAWG to create a harmonic confinement.

Voltage ramps for a shuttling operation out of the LIZ are shown in figure Fig. 5.1, transporting the ion from the LIZ (Seg. 19, and Seg. 119) to the adjacent neighboring site (Seg. 20, and Seg. 120), where the voltage at LIZ segments are ramping up, while simultaneously, the voltage at adjacent neighboring segments are ramping down. On most adjacent DC electrodes and electrodes placed symmetrical with respect to the current ion position, e.g. electrodes 19 and 21, for ions stored at segment 20, the same voltage is applied with the addition of a small offset in the voltage added for micro-motion compensation [Pos+09].

When creating the required voltage waveforms transport trajectory are fit to the potential minima at the center of each of the trapping segments from start to end segment. The potentials are engineered for harmonic confinement using six DC electrodes of three segments, the current position and the two neighboring segments.

Voltage ramps are smoothed to avoid unnecessary excitation caused by sampling limitation of the analog voltages. During shuttling, ions currently move from one segment to an adjacent segment (distance 206 µm), then wait there for a certain (dwell time) then continue to towards the next segment. Besides optimizing the trajectory with corresponding voltage waveforms, the dwell time is an important optimization parameter, so the measurements for various dwell times are presented here. The scanned dwell time provides a relation between axial-trap frequency

and motional excitation with the period of $2\pi/\omega_x$ in due process. Furthermore, we do observe a similar dependency with the oscillation period of ≈650 ns (ω_x=2π×1.5 MHz).

Real-time transport trajectory in experiments

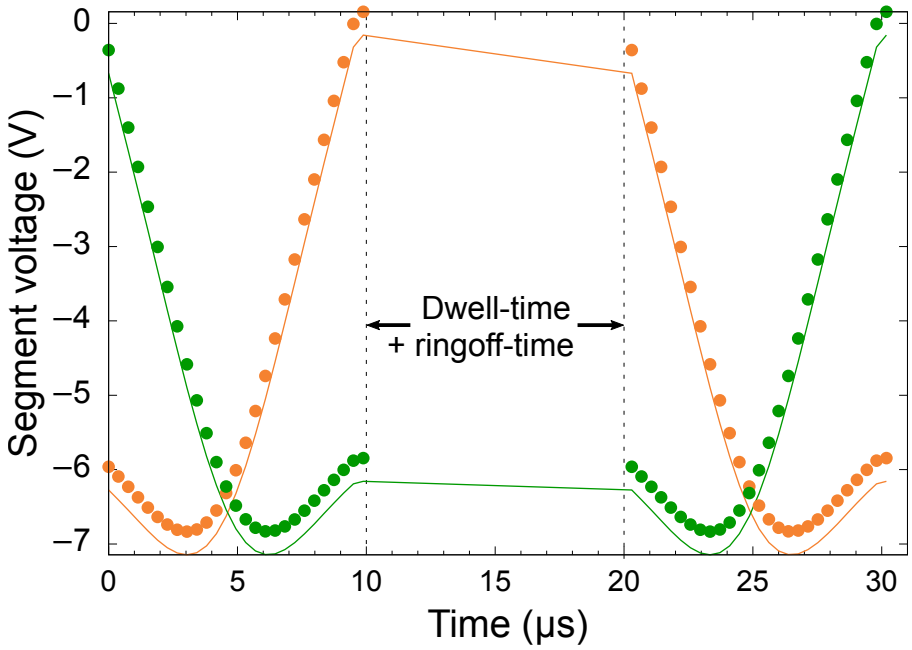


Fig. 5.1 A real-time experimental voltage ramp for transporting ion from one segment to its neighboring segments and then transport back to starting point. It represents pairwise energy neutral transport ramp, which starts with an initial sequence (5.785 ms) of Doppler and sub-Doppler cooling, and state initialization followed by transport and manipulation. Transport duration of (10 µs) in onward and reverse journey, ring off-time (10 µs) which allow the voltage to settle and dwell time (20 ns) have been used in this sequence [Wal+12]. Ring off time is experiment specific and are generally altered for experiment-specific need (between 1-30 µs). In our 3D trap, as two voltage sources are used for building the harmonic confinement for trapping the ions. Both the electrodes are generally programmed to identical voltage, however a tiny offset of voltages are added and subtracted for compensating the micro-motion [Pos+09]. Similarly, a harmonic potential at the neighboring segment is controlled. Solid line, shows the top electrode while the round circle shows the variation of voltage on bottom electrode. Orange color is representing the variation of voltage (-6 V→0 V) on the segments in LIZ while, green color represents variation (0 V→-6 V) at the neighboring segments.

The factors that primarily affect the transport trajectory are update-time of the analog sample, cut-off frequency of the low pass filter that distort the signal and the ring-off time, which helps reduce effect of non-optimal voltage waveforms and allows the ions come to rest

after applying the shuttling voltage waveforms. The analog voltage update rate is N×360+20 ns, where N is the number of analog samples. This results in a transport duration of 10 µs, 27 analog samples updates on the involved segments, (only two segments are considered during segment wise transport). The low pass filter has cutoff f_c=100 kHz. There is ring-off time 10 µs included in each shuttling sequences. Further discussion of transport trajectories for the segmented ion-trap used in this these can be found in [R+06; S+06; Sin+10; Rus12].

Axial mode: Pseudoenergy metric and Sideband spectroscopy method

For the optimization of shuttling waveforms a rough estimate of the gained motional quanta measured in a short time scale is more beneficial than precise but slower measurements using sideband spectroscopy. A way to achieve such an estimate is the use of so called pseudoenergy measurements, which were introduced in [Wal+12], and are realized by applying stimulated Raman transitions with on the first blue and red sidebands and also the second red sideband for fixed pulse areas of 3π, 2π and 2π respectively [Wal+12]. The expression for pseudoenergy metric is given by [Wal+12],

$$E_p = 2[P_{\uparrow,+1}(3\pi) - P_{\uparrow,-1}(3\pi) - P_{\uparrow,-2}(2\pi)] + 7/2; \tag{5.1}$$

Where $P_{\uparrow,\delta n}$ is the probability of finding the ion in state $\uparrow$ after driving a stimulated Raman transition and +1 corresponding to the first blue sideband -1 to the first red and -2 to the second red sideband. Using this measurement is two orders of magnitude faster compared to performing a detailed sideband spectroscopy. Pseudoenergy measurements are only viable for limited phonon excitation numbers below 50 and need to be calibrated performing full sideband spectroscopy measurements.

The figure shown in Fig. 5.2 shows the plot of data recorded for estimation of motional excitation on the axial mode at (ω_x=1.5 MHz) using the pseudoenergy method.

Making use of the established pseudoenergy a linear transport operation was optimized for various dwell times, the waiting time of the ion between two transport operations. The parameter is of great importance and does not follow a linear scaling as the exact moment ions are transported back determines at what position the ion is in its secular oscillation. Experimental results for linear transport operations showing the gained normalized pseudoenergy vs dwell time are shown in Fig. 5.2.

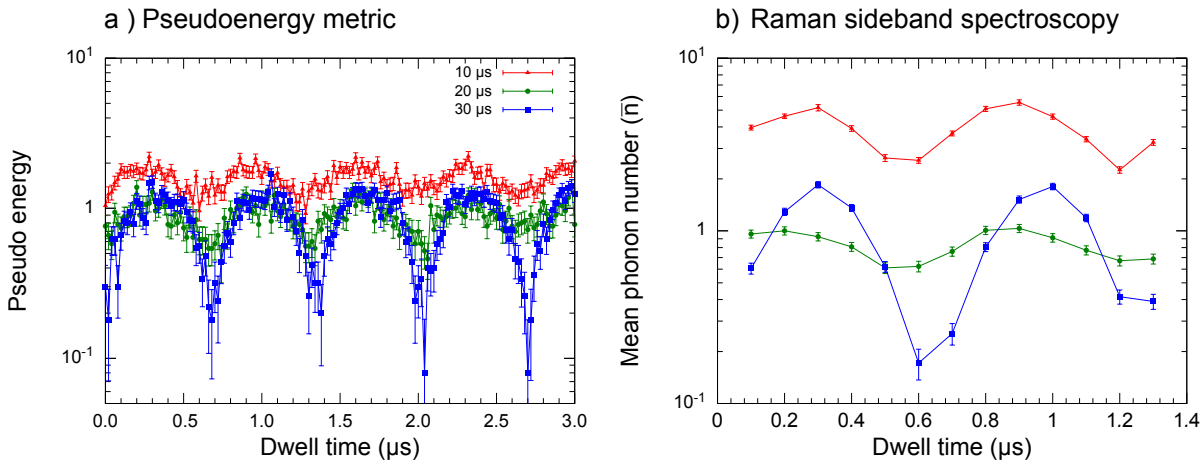


Fig. 5.2 Mean motional excitation on the axial mode using pseudoEnergy metric and Raman sideabnd spectroscopy methods. Single trapped ion is transported from trapping segment, LIZ (Seg. 19) to the neighboring segment (Seg. 20, 206 µm away) and allowed to wait, then transported back to LIZ. This wait time (dwell time) between two fast transport has been scanned in steps of 20 ns for (a) and 100 ns for (b), for multiple transport durations (10 µs (red), 20 µs (green), 30 µs (blue), for both plots). **(a)** It shows the motional excitation measured coarsely using pseudoenergy metric for the mentioned transport durations for larger dwell-times. **(b)** This measurement shows motional excitation measured precisely for mentioned transport durations for limited dwell-times durations. From either measurements, gained momentum does not cancel completely for the transport duration below 20 µs. However, for the transport duration of 30 µs, it is completely canceled with final gain in motional excitation at (0.01 ph) with periodic oscillation at period of $2\pi/\omega_x \approx$650 ns. It is pairwise self-neutral transport scheme [Wal+12], where ion travels 206 µm. The mean excitation is still comparable among all separation durations, so, 10 µs can also be used as standard duration for transport ion over one segment.

One can see that a measurement using the pseudoenergy allows for a detailed analysis and optimization of the dwell time. Using sideband spectroscopy measurements the results can be validated and the exact amount of gained motional quanta for optimized linear transport is obtained. From these optimizations and measurements we can conclude the following:

Gained motional quanta vs dwell time for the transverse modes ($\omega_y = 2\pi \times 3.8\,\text{MHz}$ and $\omega_y = 2\pi \times 4.8\,\text{MHz}$) was determined using sideband spectroscopy and is shown in Fig. 5.3 **(a)** and Fig. 5.3 **(b)**, respectively. The plots shown in Fig. 5.3 show absence of any excitation due to transport up-to 10 µs on the transverse modes, making it ideal for implementation of high fidelity entangling gate.

For determination of exact phonon number, sideband spectroscopy has been employed for the axial and transverse mode separately (see Sec. 1). For the analysis of transport induced excitation on axial mode, dwell time has been scanned from 100 ns to 1300 ns at the interval of 100 ns, for each duration 10 µs, 20 µs and 30 µs (see Fig. 5.2). The measured mean motional excitation for different transport duration are as:

1. For 10 µs, a maximum of 5.54(19) ph at the dwell stay of 900 ns while a minimum value of 2.25(9) ph at the dwell stay of 1200 ns has been measured.

2. For 20 µs, a maximum of 1.03(5) ph at the dwell stay of 900 ns while a minimum value of 0.60(4) ph at the dwell stay of 500 ns has been measured.

3. For 30 µs, a maximum of 1.85(7) ph at the dwell stay of 300 ns while a minimum value of 0.17(3) ph at the dwell stay of 600 ns has been measured.

Comparing with the earlier reported result of the letter [Wal+12], the upper limit of the modulating dwell-time dependent excitation for the comparable transport duration (11 µs) is lesser, on contrary the lower limit is larger. It infers, that the current experimental conditions is optimized for longer transport duration. However, at the transport duration (30 µs), the minimum of 0.17(3) ph has been measured. This shows that the momentum gained during short transport operation is not canceled in the return transport, which is also inferred through measurement in pseudo energy metric. All other of pseudoenergy metric is in complete agreement with sideband spectroscopy based measurement, as expected.

1. The heating of the ion is more when ion is transport to neighboring segment in 10 µs. While for transport duration greater than 20 µs, the coherent excitation is similar. This means that limitation of transport duration in current system is 20 µs.

2. For an optimal self-neutral scheme, the minimum transport duration is 30 µs. The complete cancellation of the momentum due to return transport is not optimal for the smaller transport duration, hence there is residual excitation.

3. There is also phase dependency among the recorded excitation for the different transport duration, in self-neutral scheme.

Due to multiple filters (f_c=10 MHz at trap-PCB and low pass at feedthrough), the programmed waveforms are not updated at the electrodes as intended, therefore the trap electrodes still see residual update of waveform even when the shuttling operation has completed. Beside this, there is ringing duration inherent to programmed voltages which needs to settled

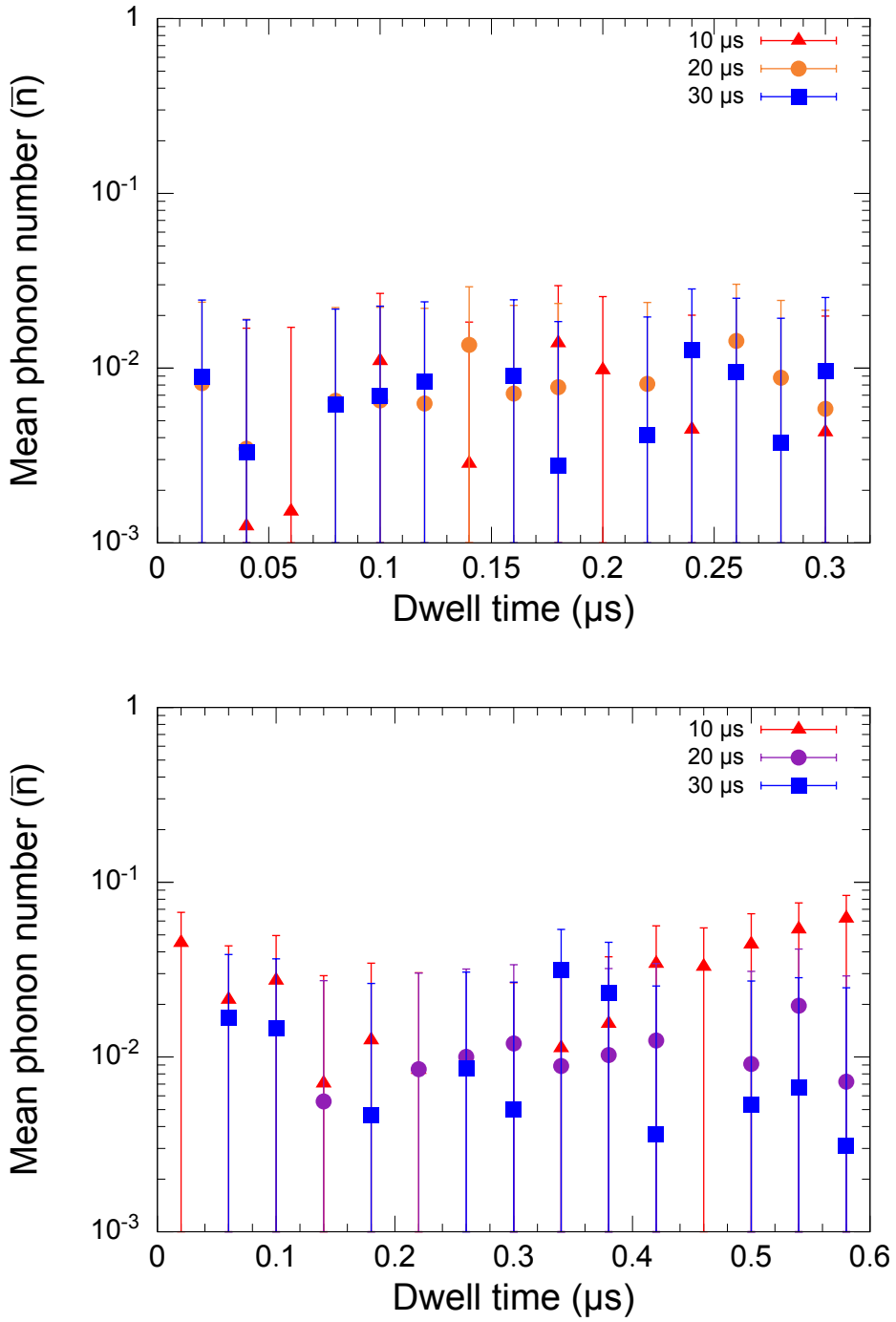


Fig. 5.3 Mean motional excitation measured using sideband spectroscopy on the transverse modes induced due to transport of single ion from one segment to neighboring segment (206 µs). It has been scanned as function of dwell-time for multiple transport durations (10 µs (red) , 20 µs (orange (trans2), purple (trans1)), 30 µs (blue), for both plots). **(a)** The higher frequency transverse mode (trans2, ω_z=2$\pi\times$4.6 MHz **(a)**) has been scanned in step of 20 ns starting from 20 ns to 300 ns for the mentioned transport durations. **(b)** Similarly, the lower frequency transverse mode (trans1, ω_y=2$\pi\times$3.8 MHz) has been scanned in step of 40 ns starting from 40 ns to 580 ns, for similar transport durations. The difference in scanned time-step of dwell duration is motivated to resolve the trap oscillation period of lower and higher transverse modes. No excitation of trans1 modes has been observed while trans1 has shown negligible gain. Hence, no dependency of respective trap oscillation period is seen on transverse modes.

Transport duration	ax ($2\pi\times1.5$ MHz)		trans1 ($2\pi\times3.8$ MHz)		trans2 ($2\pi\times4.6$ MHz)	
(µs)	min.	max.	min.	max.	min.	max.
10	2.2(1)	5.54(19)	<0.01	0.06(2)	<0.01	<0.01
20	0.60(4)	1.03(5)	<0.01	~0.01	<0.01	<0.01
30	0.17(3)	1.85(7)	<0.01	~0.01	<0.01	<0.01

Table 5.1 Summary of motional excitations of all motional modes ($\omega_{x,y,z}$) during linear transport operations for various transport duration times. Lower frequency transverse mode shows almost negligible excitation and the higher frequency no mode shows no excitation. Phonon numbers for the axial mode show a clear dependency with transport time.

before laser manipulation of qubit can be performed. Both of these factors requires additional ringoff time to be added at the end of the shuttling operation before the manipulation of qubit can be started.

The ring off-time in the experiment varies from 10 µs to 30 µs, depending upon how strong is voltage ringing. Generally, larger is the slew rate, stronger is voltage ringing. Therefore, in order to resolve the quantum phenomena within the trap-oscillation duration, we introduce the idea of dwell-time, which a wait duration for smaller time (time scale of 20 ns).

A significant gain in phonon numbers for the axial mode and a 10 µs transport time indicate that this will be the practical limit for the current system. The major limitation for faster transport times are the essential low-pass filters, which distort the faster waveforms required for shorter transport times. In the future a higher cut-off frequency can be tested, which will negatively impact heating rates during all operations. Another way of reaching shorter transport times without increase the cut-off is the use of a sophisticated filter compensation software module. This module is currently in development and makes use of filter response curves and Fourier transformations. To compensate for non-linear behavior of the acmAWG additional adjustments will need to be made. We expect that a successful implementation of the filter compensation will reduce the gained motional phonons for short transport times like 10 µs and allow for even shorter transport times.

Implementing linear transport over longer distances, over multiple trap segments, an optimal transport trajectory can be designed enabling much faster transport over x segments then 10 µs times x. This way quasi ballistic transport between the start and end segment is realized. This scheme has been successfully demonstrated with significantly less excitation compared to fast segment-wise transport [Nic17].

Fast linear transport with minimal motional excitation, a critical building block of a quantum processor node, was established and demonstrated in this work. Although sufficient, future developments will focus on using improved filters and filter compensation with more advanced transport protocol to further reduce transport times and phonon excitation. In addition, the platform can be used to test ideas using optimal control [Für+14] and further improvements to transport ramps [Pal+13].

5.2.2 Separation of a two-ion crystal

Two-ion crystal separation, in combination with two-ion swapping and the previously discussed linear transport are critical building blocks of a quantum processor node and allows for individual addressing of ions using a laser interaction zone without having to rely on tightly focused laser beams. The process of separating two ions in one potential well requires very specific and well optimized voltage waveforms applied to multiple trap segments. Similar to linear transport, separation operations need to be performed as quickly as possible without adding a significant amount of motional quanta to the ions motional modes. In contrast to linear transport the axial confinement and secular frequencies vary significantly during the operation and the applied voltage waveforms are mostly optimized to keep the secular frequency as high and stable as possible during the separation.

The first experimental demonstration of two ion crystal separation was demonstrated in [Row+02], followed by faster 80 µs diabatic separation presented in [Bow+12; Rus+14], also achieving a lower motional excitation. Making use of the general improvements to the experimental setup discussed in the previous section and also the improved mAWG and optimization of two and more ion crystals separation operations will be demonstrated in this section. After calibrating voltage waveforms the shuttling processes for various separation times were optimized. During this process we also were able to determine the minimal axial frequency during separation to be 275 kHz, which was higher than in previous experiments and led to the use of higher cut-off frequency filters 100 kHz instead of 50 kHz. Higher cut-off filters allow for faster voltage waveform changes and consequently to fast separation.

Principle of ion crystal separation

RF and DC voltages are applied to the trap electrodes and commonly create confining quadrupole-fields along the transverse (ω_y, ω_z) and axial (ω_x) directions. During separation DC voltages are adjusted to split the confining harmonic potential well, into double potential wells, as illustrated in Fig. 5.4. The underlying theory and experimental implementation have been

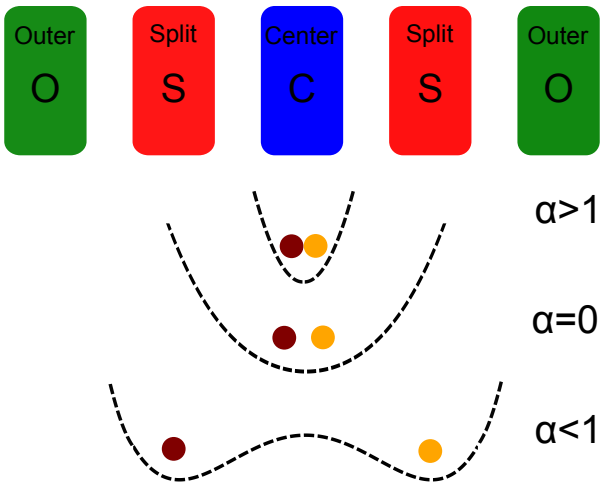


Fig. 5.4 Illustration of separation process. The harmonic confinement used to trap both the ions is changed to quartic and finally double well potential to facilitate the separation of ions from a two-ion crystal, where each separated ions end up into a separate harmonic potential created at the split segments. Center (C), Split (Split), Outer (O) are the trap segments that contributes to this process (See Fig. 5.8 for more information.)

extensively discussed in [HS06; Kau+14; Rus+14]. However, a brief discussion is presented here.

The electrostatic potentials during the separation process can be characterized using a multi-pole expansion around the center of mass of the two-ion system.

$$V(x,t) = \beta(t)x^4 + \alpha(t)x^2 + \gamma(t)x \tag{5.2}$$

Coefficients α, β, γ are determined by ion-trap geometry and applied voltages and vary significantly during the separation operation. Variations of α represent the nature of the electrostatic potential, starting at $\alpha > 0$ for the initial potential well going to $\alpha = 0$ at the moment of splitting the well into two and ending in $\alpha < 0$ for separate double potential wells. At the moment of splitting the well $\alpha = 0$, also know as the critical point, the quartic term β is responsible for widening the potential well and needs to be maximized to keep the axial motional frequency as high as possible. This is done applying large voltages to suitable neighboring electrodes, effectively pulling the harmonic potential into two parts. The larger voltage range of the mAWG of (± 40 V) helps with this process and allows for larger axial secular frequencies 275 kHz at the critical point. Finally, a tilt voltage is applied to the potential, which splits the widened flat harmonic well into two wells and is represented by the γ parameter.

These coefficients (α,β and γ) are parameterized in term of bias voltages and electrostatic properties of trap.

$$\alpha = U_C\alpha_C + U_S\alpha_S + U_O\alpha_O + \alpha^{'} \tag{5.3}$$
$$\beta = U_C\beta_C + U_S\beta_S + U_O\beta_O + \beta^{'} \tag{5.4}$$
$$\gamma = U_C\gamma_C + U_S\gamma_S + U_O\gamma_O + \gamma^{'} \tag{5.5}$$
$$\omega_x^2 = 2e/m(U_C\alpha_C + U_S\alpha_S + U_O\alpha_O + \alpha^{'}) \tag{5.6}$$

Voltages applied to the used electrodes are denoted with subscript (C,S,O), which stands for center, split and outer electrode respectively.

Making use of these equations effects of applied voltages especially on α, β and γ parameters of the confining axial potential are calibrated for each of the electrodes (C,S,O. The trap frequency relation given by (ω^2=2αe/m) is exploited to calibrate α for each trap electrode, measuring ω with the use of sideband spectroscopy. Afterwards β is calibrated by measuring the ion distance in a pure quartic potential.

Tilt voltages and corresponding γ parameter are calibrated by observing the ions in camera, in case if it is not well compensated both ions will move in either well of slowly generated double well potential during separation. Then, successful separation of the two-ion crystals is checked for a wide range of tilt voltages by slowly varying the tilt offset in step of 1.2 mV. Voltage adjustments are very sensitive and separation completely stops working beyond 30 mV. In contrary to theoretical predicted CP-offset windows of 20 mV, which is needed for ion separation in Lamb-dick regime, the experimental findings so far suggests that a much smaller, CP-offset windows of 1-2 mV, is required. Otherwise, strong acceleration during voltage ramping may increase heating of ions in the range of 10-100 phonon. The calibration methods are explained in more detail in [Rus+14].

The process of generating voltage waveforms starts with the calibrated static voltage sets. Waveforms start and end the sequence with optimal values for one and two harmonic wells for the α parameter. During the splitting process voltages are set for maximum β and ideal γ. The static voltages (U_c, U_s, U_o) are set for initial, critical and end point of the separation operation.

Finally, a sinusoidal path for the ions is chosen based on (eq. 5.7) that follows these preset conditions and address the distance between two ions during the separation process. This

distance (d_{eq}) is monitored and corresponding α is calculated to evaluate the time-dependent voltage ($U_c(t), U_s(t), U_o(t)$) at C, S, O segments.

$$d_{eq}(t) = d_i + (d_f - d_i)(t/T)^2 sin^2(\pi t/2T) \tag{5.7}$$

Where $d_{eq}(t)$ is the equilibrium distance between two ions at any time. Parameters d_i, d_f are initial and final separation distance respectively, T is the duration for a complete separation process.

In the current experimental setup with the described ion-trap [Rus18; Kau18], calibration of α and β have to be occasionally repeated as laser-induced charging of the trap surface [Har+10; Wan+11] leads to drifts of these trap parameters. The tilt voltage has a strong effect on the very sensitive parameter γ and therefore requires frequent calibration especially for faster separations (<60 µs).

Characterization of critical parameters during separation

Besides optimizing static voltages sets α, β and γ parameters and the separation waveforms we can further investigate the heating rate during the separation process and stability of secular frequency in axial direction. The significant drop of the axial confinement and therefore the secular frequency at the critical point results in the heating rate becoming are more important factor due to its $\dot{\bar{n}} \propto f^{-2}$ scaling. In addition to the higher heating the changing axial confinement can also cause a gain in motional quanta independent of heating due to electric noise.

Variation of secular frequencies during separation

During the separation of two-ion crystals, axial confinement is reduced when approaching the critical point, which leads to an increase in heating of the axial mode and also independent of electrical noise strongly varying axial confinement leads to an increase in motional quanta in this mode. Measurement of axial secular frequencies makes use of sideband spectroscopy with a Raman beam pair, described in detail in [Pos+09]. The R1/R2 beam pair is employed to measure the axial frequency while the R1/R4 beam pair has been used to confirm stable transverse mode frequencies (see Sec. 1).

The progress of separation of individual ion from ionic crystal is defined on an arbitrary normalized time-scale (a.u), which is also called as reaction-coordinate (*rc*). The a.u.=0 (or rc=0) is defined as the start of separation process, *rc*=1, separation process reach at critical point

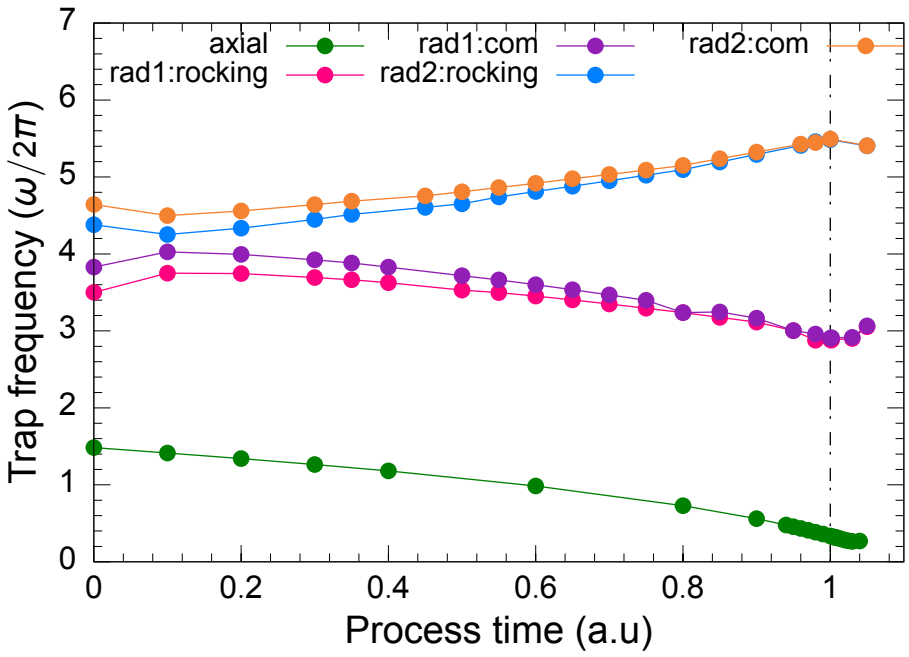


Fig. 5.5 The variation of the secular frequency (on the principle mode (ax, trans1(ROCK, COM), trans2(ROCK, COM), see Sec. 2.1 and Fig. 2.2) during the separation of two ions crystal along the reaction coordinate unit. The reaction coordinate is arbitrarily chosen linear time scale to quantify the two-ion crystal separation process on linear scale [Kau+14; Rus+14]. At critical point (a.u.=1), axial confinement is very weak with $\omega_x = 2\pi \times 275\,\text{kHz}$, while the transverse ROCK and COM modes merges at secular frequencies of $\omega_{y,z} = 2\pi \times \{2.89\,\text{MHz}$ and $5.48\,\text{MHz}\}$, but still remains much larger than the axial trap frequency.

and *rc*=2 crystal separates out as individual ions trapped at two different harmonic potentials.

For the measurement of the transverse modes, resonating peaks has been followed carefully, as a single beam-pair (R1/R4) is being used to investigate both center of mass (COM) and out-of-phase (ROCK) modes of both lower and higher frequency transverse modes. The frequency of normal modes has been closely monitored till *rc*=1, as after this crystal separates successful thus ROCK mode will cease to exist. Hence, transverse COM mode will approach to the standard transverse frequency as of the single ion. A similar scheme with the fixed maximum voltage at the Outer electrodes has been used to measure the critical point trap frequency of the axial modes. The variation of axial, and both transverse mode (lower and higher) frequency (both COM and ROCK) has shown in Fig. 5.5.

At start of the separation process, the ax (COM) trap frequency is $2\pi \times 1.5\,\text{MHz}$ which decreases to $2\pi \times 275\,\text{kHz}$ at *rc*=1. The transverse confinements for two-ion crystal are

ω_y^{COM}=$2\pi\times$3.8 MHz and ω_y^{rock}=$2\pi\times$3.4 MHz for COM and ROCK mode on lower (trans1) frequency transverse mode, while higher (trans2) frequency modes are ω_y^{COM}=$2\pi\times$4.6 MHz and ω_y^{ROCK}=$2\pi\times$4.4 MHz for COM and ROCK mode respectively. The trans1 mode (COM and ROCK) frequency reduce to a minimum value of $2\pi\times$2.89 MHz while trans2 mode (COM and ROCK) frequency increases and merge at the maxima of $2\pi\times$5.48 MHz.

Heating rate at critical point

The heating rate measured at the frequencies equivalent to CP trap-frequencies are 6(1) ph/s on the trans2 modes ($2\pi\times$5.48 MHz), 28(5) ph/s trans1 ($2\pi\times$2.89 MHz), and 34(9) ph/s on the axial mode ($2\pi\times$748 kHz). During the separation (at rc=1) of two-ion crystal, both the normal modes of the higher and lower transverse modes (COM/ROCK) merges to a single value as degeneracy is lifted (see Fig. 5.5), leaving only three degrees of freedom for each ion. Therefore, a measurement has been done with single ion where axial as well as both transverse frequencies have been manually tuned close to the measured respective frequencies at critical point to get a classical idea of thermal excitation limit caused during the separation of two-ion crystal. Recalling the results presented earlier (see Sec.3.7) with f_c=100 kHz has $\dot{\bar{n}}_{\omega_x,\omega_y,\omega_z}$={11.(2), 26.6(7), 9.2(3)} ph/s, where $\{\omega_x,\omega_y,\omega_z\}$={1.5, 3.8,4.6} MHz. For trans2 motional mode critical point frequency is larger than the standard working frequency (ω_{cp}^{trans2}=$2\pi\times$5.48 MHz > ω^{trans2} = 4.6 MHz) so marginally smaller heating rate is observed, similarly for trans1 ($\omega_{cp\text{trans1}}$=$2\pi\times$2.9 MHz > ω_{trans1} = 3.8 MHz), marginal rise in heating rate is expected. Similarly, the rise in axial heating rate has been measured for critical point frequency.

The heating rate for trap-type A with critical point trap frequency (ω_x=$2\pi\times$180 MHz) [Kau+14] is

$$\dot{\bar{n}} = \Gamma_h(pred.) = 6.3\omega^{-1.8}\ ms^{-1} \tag{5.8}$$

However, in current case critical point trap frequency (ω_x=$2\pi\times$275 MHz), and the experimentally observed variation of heating rate (see Fig. 3.8) is

$$\dot{\bar{n}} = \Gamma_h(exp.) = 12.4(4)\omega^{-1.3(1)}\ ms^{-1} \quad (Sec.\ 3.8) \tag{5.9}$$

where ω is $\omega_{x,y,z}/2\pi$.

The anomalous axial heating rate measured at the critical point using (eq. 5.8) is $\dot{\bar{n}}^{pred.}_{180\,\text{kHz}}$ = 65.18 ph/s, while from the measurement discussed in this thesis (see Sec. 3.3), it is $\dot{\bar{n}}^{exp}_{275\,\text{kHz}} \approx$ 66.41 ph/s. Both predicts similar rate of heating at the critical points. However, using the exper-

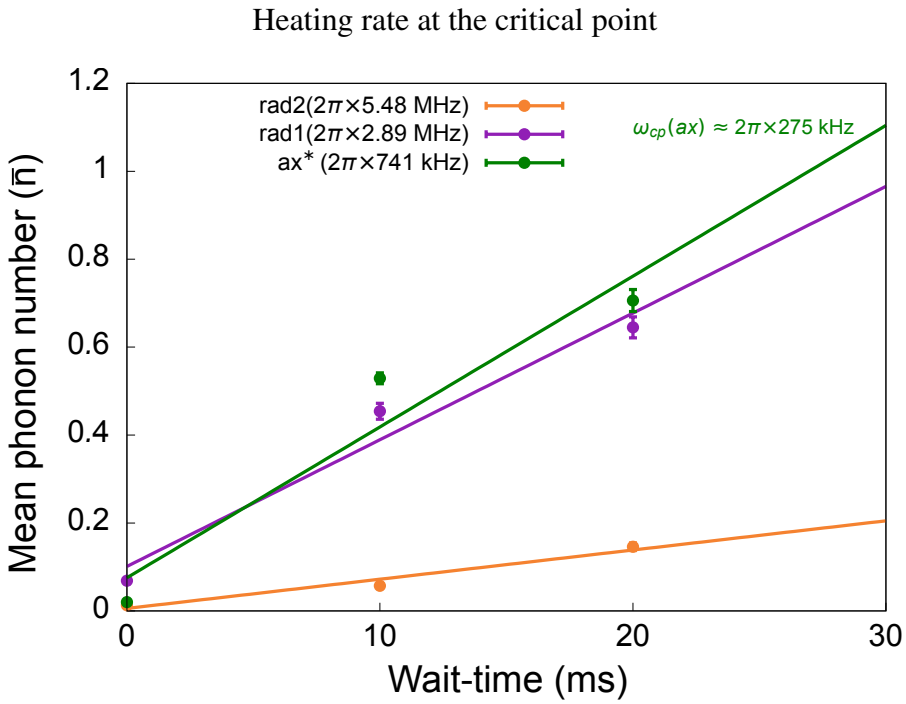


Fig. 5.6 Heating rate of single trapped ion at secular frequencies equivalent to the critical point during the separation of two-ion crystal. The higher and lower transverse frequencies (trans2, $2\pi\times5.48$ MHz and trans1, $2\pi\times3.48$ MHz) are manually tuned to critical point transverse frequencies while for axial mode, the lowest possible measurable axial secular frequency in our trap is (ax_* ($2\pi\times0.748$ kHz)), for lesser frequency harmonic confinement is too week to trap the ion. The heating rate on axial motional mode is 34(9) ph/s ($2\pi\times0.741$ MHz, green), on trans1 motional mode 28(5) ph/s ($2\pi\times2.89$ MHz, indigo) and on trans2 ($2\pi\times5.48$ MHz, orange) motional mode it is 6(1) ph/s measured with old low pass filter of $f_c = 100$ kHz.

imentally deduced expression (eq. 5.9), the heating rate at lowest measurable trap frequency (ω_x=$2\pi\times0.741$ MHz) is $\dot{\bar{n}}$= 18.36 ph/s, which is much smaller than the actual observed value $\dot{\bar{n}}^{exp}_{0.741\,\mathrm{kHz}}$=34(9) ph/s. The only difference between current measurement (f_c=100 kHz) and the one discussed in earlier section (f_c=50 kHz) (see Sec. 3.8), is the use of low pass filter. This heating rate is larger by factor of ~1.79, which has been so far observed only on the transverse modes is apparent at lowered axial trap frequency. The increase in thermal noise due to the filter, also appear on axial mode at lowered frequency. This needs further investigation to assert if thermal heating from filter impedance is causing this, it will be interesting to observe under what circumstance it couples to axial mode.

Experimental methods and results

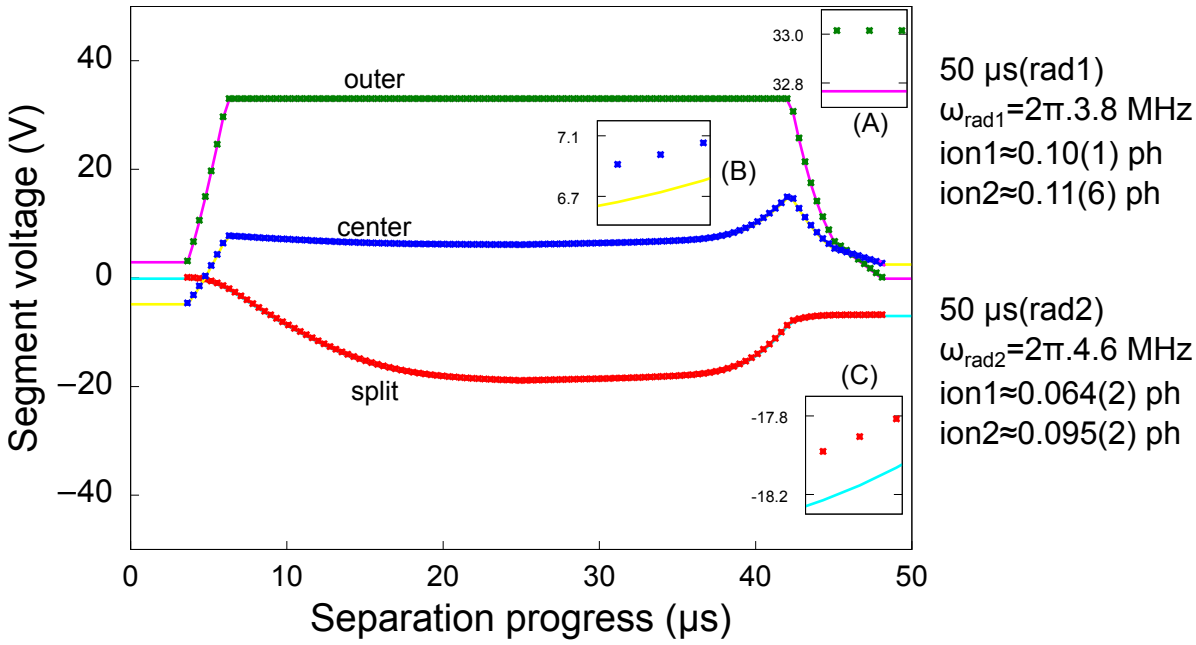
The motional excitation during the separation of two-ion crystal on axial and both transverse modes are investigated with varying separation duration. Tilt field (γ), and critical point offset $\delta U^{(CP)}$ at C segment are two major factors that have large affects over excitation for same trap duration. Distinct γ and $\delta U^{(CP)}$ calibration needs to be done for search of right tilt and $\delta U^{(CP)}$ so that final measurement result in minimal motional excitation for either axial or transverse mode for that specific separation duration. The measurement methods remains largely same as discussed in [Rus+14]. The tilt field (γ) is scanned for ΔU_O and mid value of this scan is selected as it has been found that energy increase of both ions is minimum for a tilt field if the energy increase in both ions are similar. After this, $\delta U^{(CP)}$ is calibrated by using R2 beam for the axial and R4 beam for the transverse motional modes. The π pulse of the respective carrier (R1/R2 and R1/R4) transition are used to probe the spin excitation on axial and transverse modes respectively, where large spin excitation refers an offset ($\delta U^{(CP)}$) value for lower motional excitation. Thereafter, a new measurement is conducted for these specific configuration using respective transition to probe axial or transverse excitation as mentioned earlier (see Sec. 1)[Wal+12; Rus+14; Lei+03a].

Static voltage set for separation

For the transverse modes, the shortest separation duration with minimal excitation achieved for the separating the 2-ion crystal is 50 µs. It was performed with central electrode 19 (18, 19 as split and 17, 20 as outer electrode). During separation, the time dependent progress of voltage on the segments C,S,O has been shown in Fig. 5.7a. The set of static voltages for this ramp $U^{i}_{C,S,O}$={-6.000, 0, 2.871} V at the beginning of the separation, $U^{CP}_{C,S,O}$={0.22115, -19, 33} at the critical point and finally $U^{f}_{C,S,O}$={2.6, .9, 0} at after the separation is completed. Using this static voltage set, a time dependent voltage ramp (see Fig. 5.7a)was designed using eq. 5.7 and reverse mapping of alpha [Kau+14; Rus+14]. The latest mean excitation measurement results for transverse modes are discussed (see Sec. 5.2.2).

The ramp shown in Fig. 5.7b corresponds to 60 µs separation duration (see Fig. 5.10 for motional heating measurements), relevant for minimal excitation on axial mode. The static set of initial voltages are $U^{i}_{C,S,O}$={-6.000,0,0} V at *rc*=0,$U^{cp}_{C,S,O}$={0.221,-18,33} V at *rc*=1,and finally $U^{f}_{C,S,O}$={2.6,-6.9,0} at *rc*=2.

(a) Transverse:Optimized voltage ramp for minimum transverse excitation



(b) Axial:Optimized voltage ramp for minimum axial excitation

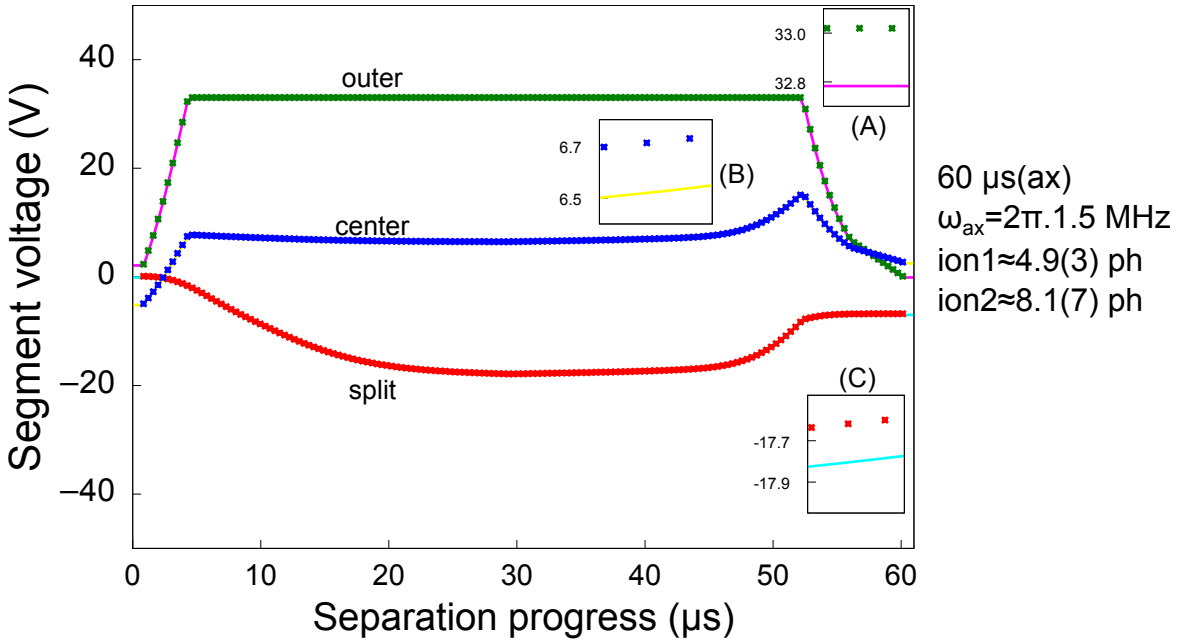


Fig. 5.7 The real-time voltage ramp for least excitation on axial and transverse mode. **(a)** The variation of voltage on center, split, outer electrodes for separation of two-ion crystal in 50 μs least motional excitation on transverse direction. Similarly, **(b)** is voltage ramp for least axial excitation ($<$10 ph) in 60 μs. The differential variation of different segments are as: center segments (top:solid-line(yellow), bottom:asterisk-points(indigo)), split segments(top:solid-line(aqua), bottom:asterisk-points(red)), outer segments (top:solid-line(pink), bottom:asterisk-points(green)). The plots in insets(A,B,C) highlights the small voltage difference between top, bottom segments of center, split and outer segments of the trap. **(a)** and **(b)** follow pre-sequence of 9.347 ms and 5.347 ms respectively for (Doppler and sub-Doppler cooling (transverse)) and (Doppler and sub-Doppler cooling (axial)) as well.

The axial mode is most sensitive and δU offset [Rus+14] achieved for minimal excitation on axial and transverse mode are always different. So, a single configuration that could fit well with axial and transverse modes has not been achieved for smaller duration. Although, there is still some scope for the improvement as upper voltage limit to bias the outer segments is still not well exploited. The measured mean motional excitation on the axial mode has been shown in Fig. 5.9a, Fig. 5.9b and Fig. 5.10 in (see Sec. 5.2.2).

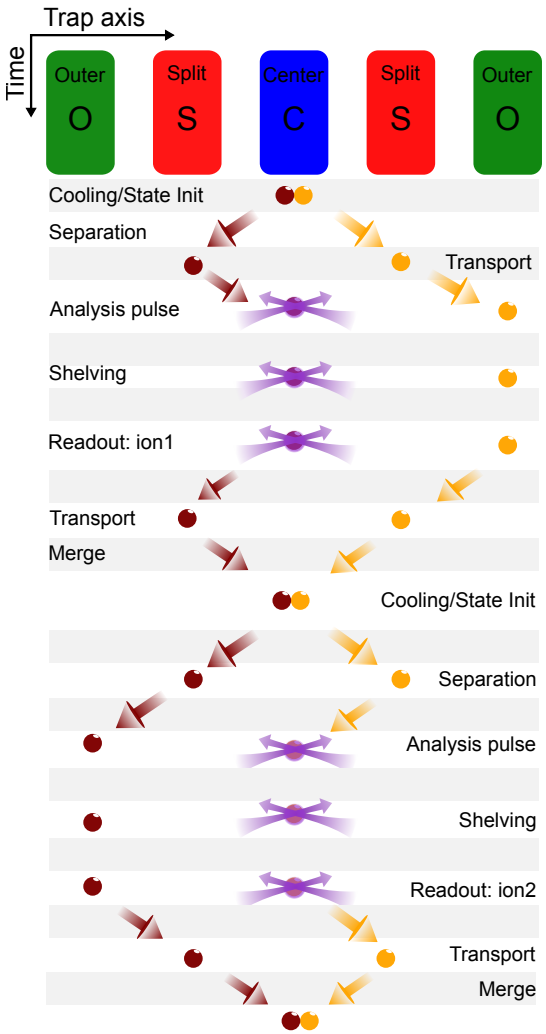


Fig. 5.8 Experimental sequence used for measuring separation induced motional excitation. Two-ion crystal is trapped then Doopler, sideband cooled followed by state initialization. Then, a separation ramp separate them out from two-ion crystal into individual ions. Thereafter, an analysis pulse, followed by shelving and read out process is performed for ion 1. Both the ions are then merged to reinstate the initial situation. Again, the measurement is mirrored to repeat this process on ion 2. The segments used during these measurements are Center (Seg. 19), Split (Seg. 20 and Seg. 18), and Outer (Seg. 17 and Seg. 21).

Axial mode

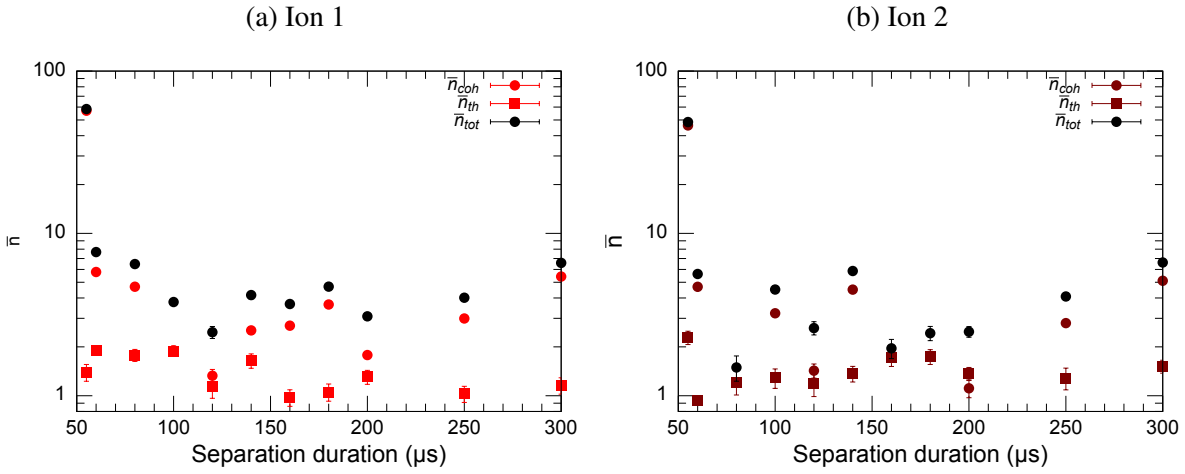


Fig. 5.9 Mean motional excitation on the axial mode of **(a)** ion 1 and **(b)** ion 2 during separation of two-ion crystal. The values shown in **(a)** by red-circle and red-square shows coherent and thermal excitation of ion 1, respectively. Similarly, in **(b)** brown-circle and brown-square represents for ion 2, respectively. The black-circles in both the plots represent mean phonon excitation for the respective ion.

The figure shown in Fig. 5.10 shows the variation of mean motional excitation of each ion for multiple separation duration. The experimental sequence follows as: Two Doppler-cooled $^{40}ca^{+}$ ions are trapped in the harmonic confinement and subjected to sideband cooling for motional ground state ($\bar{n}_{str}$<0.196(28),$\bar{n}_{com}$<0.103(30)), followed by optical pumping which initialize both ions in $|\uparrow\rangle$. Both the separation sequence is executed such that both ions separate out at harmonic confinement created at the split segments. Second ion is transported to remote segments adiabatically and first ion is then, transported back to the processing zone, where separation (and transport) induced energy increase is measured by driving stimulated Raman transition(R1/R2) and subsequent measurement of the spin state.

In the latest probe of axial motional mode excitation with current experimental controls and the latest report shows improvement over the previous presented results [Rus+14]. The best measured value in previous result was 4.16(16) ph at separation duration of 80 μs [Rus+14], while currently 6.64(17) ph/s at 60 μs, 3.98(36) ph at 80 μs, 2.5(3) at 100 μs are some of the recent measured value. Although, so far we have not observed a colder separation below 1 ph, nevertheless excitation in the range of 2-3 ph have been constantly observed for several separation duration (>80 μs). I am still hopeful that colder separation can be achieved by using right $\delta U^{(CP)}$ value.

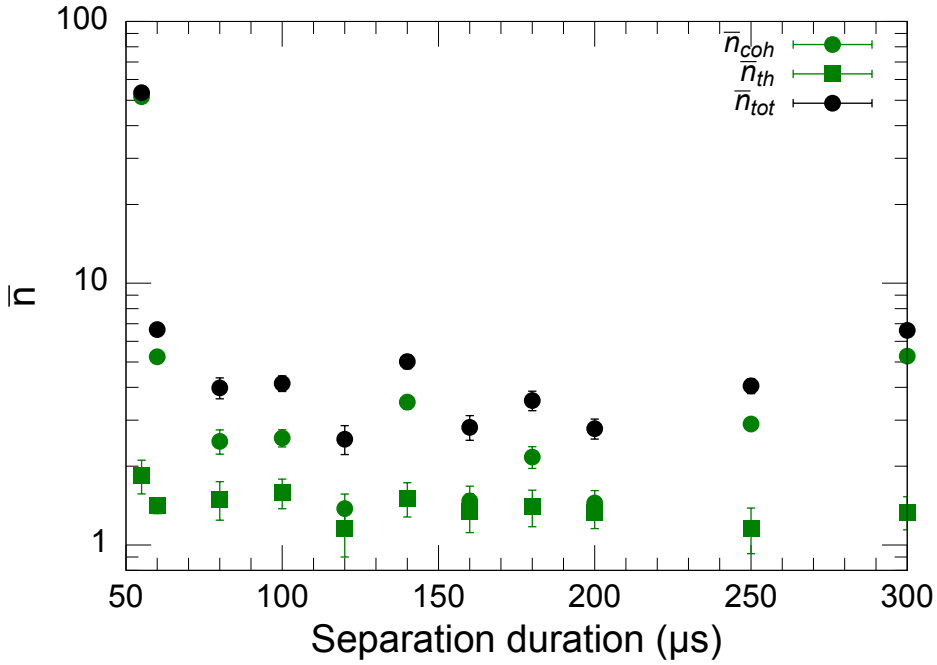


Fig. 5.10 Mean motional excitation on axial mode averaged over both separating ions during their separation from a two-ion crystal. The values represented by the green-circles and green-squares are the fraction of coherent and thermal excitation respectively, while the black-circles show mean phonon excitation average over both ions.

old measurement		new measurement			
separation duration (µs)	$\bar{n}^{old}_{50\,\mathrm{kHz}}$	separation duration(µs)	$\bar{n}^{new}_{100\,\mathrm{kHz}}$	γ	$\delta \mathrm{U}^{(CP)}$
55	98(19)	55	53.4(8)	-0.10694	0.05
60	11(2)	60	6.64(17)	-0.10304	0.06
80	4(2)	80	3.98(36)	-0.09827	-0.01
100	13(2)	100	2.53(32)	-0.0975	-0.01
120	7.5(2)	120	4.14(28)	0.1335	-0.02
216	17(2)	140	5.01(30)	0.1380	-0.12
324	25(2)	160	2.81(30)	0.1410	-0.14
432	26(2)	180	3.56(30)	0.1440	-0.16
540	39(2)	200	2.78(24)	0.1520	-0.16

Table 5.2 Mean motional excitation for different separation duration.The numbers for $\bar{n}^{old}_{50\,\mathrm{kHz}}$ has been taken from [Rus+14] (approx.), $\bar{n}^{new}_{100\,\mathrm{kHz}}$ are recently measured values. The static voltage set used for the measurements are same as presented in Fig. 5.7b. The respective recorded Rabi-flop data are shown in Appendix.

Transverse modes

The transverse motional modes have been characterized in the similar ways as of axial modes. The shuttling operation in the experimental sequence remain largely same as discussed in

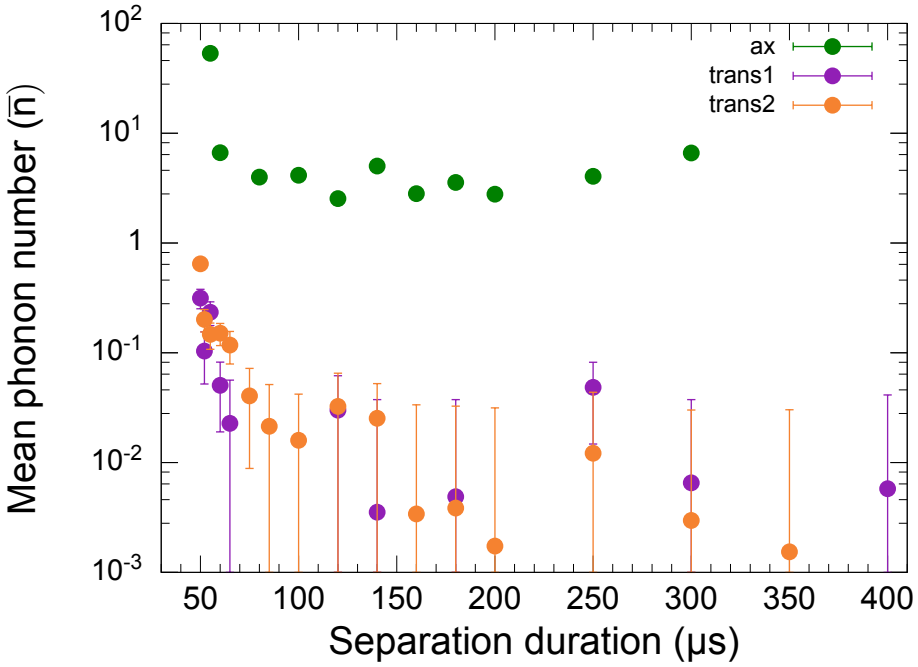


Fig. 5.11 Mean motional excitation during separation averaged over both ions on all mode (ax (green), trans1 (purple), trans2 (orange)). The transverse secular frequencies are (ω_y=2π×3.8 MHz and ω_z=2π×4.6 MHz), while axial is ω_x=2π×1.5 MHz. The mean motional excitation on any transverse mode is always less than 0.1 ph for separation above 60 μs, however for duration <60 μs marginal rise on trans1 mode is observed. The highest excitation measured on lower (purple) and higher (orange) frequency transverse modes are 0.28(6) ph and 0.64(7) ph at 50 μs respectively. However, for slower separation (<60 μs), no excitation has been measured. No excitation refers to value equivalent to baseline measurement, which is mean phonon corresponding to ground state cooled ion on the day of measurement. Some missing points in the plots are zero, highlighting absolutely no induced excitation in separation, hence only measurement error offsets are visible. Axial mode (green) measurement value are same from presented earlier, it is merely included here for sake of completeness and comparison of different modes on same scale.

above (see sec.5.2.2), however, the crystal is cooled to the motional ground state on both the transverse modes (mean phonon occupation, trans1 $\bar{n}^{COM}_{3.8\,\mathrm{MHz}} \approx 0.179(18)$, trans2 $\bar{n}^{COM}_{4.6\,\mathrm{MHz}} \approx 0.179(18)$) for the measurement of separation induced energy rise on either of the transverse vibrational modes, Raman beam pair of (R1/R4) are used. Also, after separation when either of the ions are brought at the laser interaction zone, relatively larger shift (20 kHz) in their respective transverse (both trans1 and trans2) frequencies have been observed. Therefore, for probing subsequent energy rise in their respective modes R1/R4 beam with newly calibrated center frequency of their sideband (rsb/bsb) shall be used, otherwise the sequence will just record excitation data from off-resonant rsb/bsb beams. This stark shift has been observed on

the axial modes also, but on the axial mode frequency shift is relatively rather small (1-2 kHz), hence it is not visible on the axial mode however re-calibration will further improve the contrast.

The separation barely causes any excitation on the transverse modes (see Fig. 5.11). For the separation duration (in between 60 µs to 100 µs), the lowest motional-heating has been observed, beyond this very small rise in the mean excitation has been observed on all secular mode. However, for the transverse mode this fraction is too small. The mean phonon excitation of 0.15(16) ph and 0.11(12) ph has been observed at trans1 and trans2 secular modes respectively at 50µs. The rise in the excitation below 60 µs is largely due to distortion caused by intermediate low pass 100 kHz between trap and voltage supply. Therefore, use of an algorithm that could largely speculate waveform by considering the distortion caused by these low pass filter shall improve the lower limit of separation duration threshold and also check the any coherent excitation caused due to filtering of voltages.

In conclusion, we have demonstrated faster crystal separation of as low as 50 µs (previous duration was 80 µs) and less induced excitation on all the modes. This was possible due to the upgrade mAWG and resulting larger voltage range which has allowed for stronger confinement during the separation at the critical point. As the entangling gate operation are performed on transverse mode, excitation from faster separation performed in 50 µs can be used. However, if many separations steps is to be performed a slightly slower process time of 60 µs is more suitable and will be used as standard separation duration in the quantum algorithms from now on.

5.2.3 Fast swapping of a two-ion crystal

Trapped-ions technology provides a path towards scalable quantum computer technology either by using large processing units with numerous qubits [Ste07; Lek+17] or deploying a modular based nodal architecture with photonic-interconnectivity [Mon+14]. When using dedicated laser interaction zones and shuttling to achieve individual addressing of ions, deterministic reordering of the ion-crystal are required. However, commonly suggested complicated junctions (T [Hen+06], X [Bla+09; Wri+13], and Y [Shu+14]) require multiple shuttling operations through the junction center, which is challenging performing without fast and with low motional excitation. Deterministic swapping offers a faster more efficient solution to this problem as it re-orders two-qubit crystals within without additional shuttling operations and leading to minimal excitation.

The successful experimental realization of swap gates by physically rotating the two-ion crystal on was demonstrated in [Kau+16]. Single-site rotation of two-ion crystals in 42 µs with motional excitation below 0.05(1) ph on all six normal modes was shown and also the successful rearrangement of a three ions crystal (register reconfiguration) using multiple shuttling operation. I discuss the recent results of crystal rotation on a faster timescale and also present some additional results including the reconfiguration of larger ion crystal (3 and 4-ion crystal) without further shuttling operation. The list of the latest measurements includes:

- Faster rotation of two-ion crystal (28 µs) at standard operational transverse trap frequencies (ω_y=2$\pi\times$3.8 MHz,ω_z=2$\pi\times$4.6 MHz).
- Remote swapping of two-ion crystal at any arbitrary electrodes.
- Simultaneous swapping of double two-ion crystal at two distinct remote electrodes.
- Segment independent parallel swapping.
- Swapping of a three-ion crystal
- Swapping of a four-ion crystal

Experimental method and results

Voltage ramp

The classical process of swapping is shown in Fig. 5.12, where a two-ion crystals is rotated and ions interchange their position ((AB)$\rightarrow$(BA)). This is done by simultaneously updating voltages on three electrodes of the ion-trap (see Fig. 5.12). The detailed discussion of methods and principles of tailoring the harmonic confinement is discussed in [Spl+09; Kau+16]. The transverse trap frequencies remain static in our ion-trap system, therefore physical swapping of two-ion crystals is achieved by increasing axial trap frequency with respect to lower transverse trap-frequencies. This is done by lowering the voltage on the trapping electrodes as show in Fig. 5.13.

During this experiment the secular frequencies remain as normal trapping conditions and shows a much faster (28 µ) two-ion crystal rotation at higher transverse secular frequencies ($\omega_{y,z}$=2$\pi\times$3.8 MHz, 2$\pi\times$4.2 MHz). Earlier results showed swapping at transverse frequencies of $\omega_{x,y}$ = {1.97, 3.248} MHz in 42µs. The lower transverse frequency is 1.63 MHz larger while the crystal rotation is 58% faster than previous results [Kau+16]. Due to the large transverse potential, the voltage levels required to the central segment are also larger, which has been

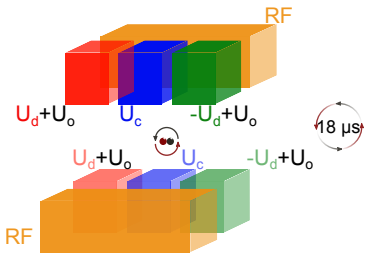


Fig. 5.12 Voltage mapping on trap-electrodes involved in swapping of a two-ion crystal in segmented ion-trap. Three electrodes and the respective voltage needed for controlled rotation of crystal are shown in respective color. The notation U_c and U_d represents voltage at trapping and diagonal segment while U_o is additional needed offset voltage which is to be applied to diagonal segments. The voltages on global RF electrodes (orange) remain unchanged. The newer time-scale for swapping of ion position by rotation of two-ion crystal is 18 µs (excluding filter delay of 10 µ).

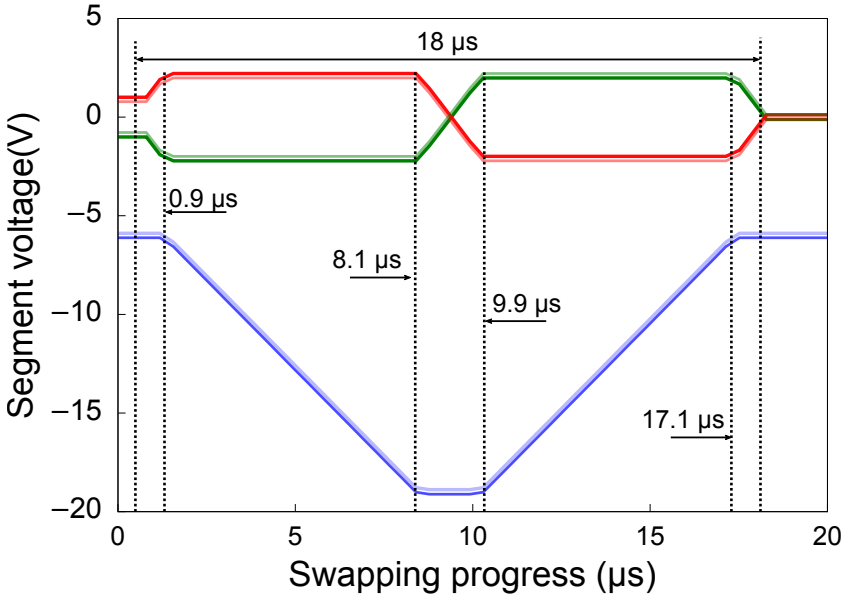


Fig. 5.13 The voltage ramps that are used to program the trap segments which are involved (see Fig. 5.12) in the swapping of two-ion crystal. It is followed in main sequence by a initial presequence of (5.346 ms), which include Doppler and sideband cooling followed by optical pumping for state initialization. Voltage at all six segments are simultaneously configured during swapping process. This voltage ramp has been used for all variant of two-ion crystal swapping discussed in this thesis. The relevant experimental parameter which constitute different laps of dimensionless timeline (t) [Kau+16] during ramping of voltage in swapping are t1 = 0.05, t2=0.45, t3= 0.55, t4= 0.95, U_c=-18.7 V, U_a=2.2 V.

possible only due to the extended voltage range of the mAWG. The sequence of crystal rotation is described using normalized time t, where rotation starts at t=0 and ends at t=1. At t=0, the diagonal electrodes, starts ramping up and reaches 2.1 V in t1=0.05, subsequently U_c starts to

ramp down to reach -19 V in t2=0.45, this leads to vertical alignment of the crystal. Then, diagonal segments start changing their polarity which breaks the symmetry, it completes at t3= 0.55, and finally U_c is ramped down to initial voltage -6 V at t4= 0.95, thereafter, diagonal segments are ramped down to 0 V in rest of 0.9 µs at t=1, thus completing the 360° rotation in 18 µs.

The smooth ramping of voltages is essentially required otherwise it will result in large coherent excitation as has been noticed during the experiment. This optimal voltage configuration for least motional excitation has been achieved by probing lower frequency transverse and axial SB on respective vibrational modes (COM/ROCK) and (COM/STR) with respect to offset voltages (U_o) [Kau+16].

Results: Motional excitation in swapping

Motional modes		$(\omega/2\pi)$(MHz)	η	swapping excitation ($\bar{n}$) (ph)		increase
				Before	After	
Axial	ω_x (COM)	1.49	0.16(1)	0.26(2)	0.36(2)	0.10(3)
	ω_x (STR)	2.58	0.11(1)	0.20(2)	0.28(2)	0.08(2)
trans1	ω_y(COM)	3.81	0.06(1)	0.33(2)	0.34(2)	0.01(3)
	ω_y (ROCK)	3.49	0.06(1)	0.25(2)	0.37(2)	0.12(3)
trans2	ω_z(COM)	4.63	0.065(3)	0.21(1)	0.25(2)	0.04(2)
	ω_z(ROCK)	4.37	0.065(3)	0.022(1)	0.23(2)	0.01(2)

Table 5.3 Rise in mean motional excitation on all the secular modes during fast swapping (18 µs) of two-ion crystal by physically rotating it.

The motional excitation caused due to swapping of crystal was probed using a stimulated Raman transition on the respective motional modes. Before excitation measurements, the sequence is tested using a tomography method for different input states to confirm the success of crystal rotation [Kau+16]. After this a swap sequence is executed, which follows the two-ion crystal pre-sequence of Doppler and sideband cooling and spin state initialization followed by swapping. Then, a Raman beam is used to probe and record the spectroscopy data for different normal of two-ion crystal. Then, the crystal is separated into individual ions for final readout. For the readout, the first ion is brought to the LIZ, then the process is executed in reverse to do a similar analysis on the second ion. This way we collect the Rabi-oscillation records to measure the rise in motional excitation. The recorded data is fitted assuming oscillatory and the mean phonon number is extracted as explained earlier.

The higher frequency transverse mode remains resilient to motional heating during swapping since only the axial and lower frequency transverse modes are part of this process. The increase in mean phonon number on COM ($2\pi\times4.63$ MHz)/ROCK ($2\pi\times4.37$ MHz) modes of trans2 secular frequencies after swapping are 0.04(3) ph and 0.01(2) ph respectively. The increase in mean motional excitation on COM modes of axial ($2\pi\times1.49$ MHz) and trans1 ($2\pi\times3.81$ MHz) secular modes are 0.01(3) and 0.10(3) ph respectively, while STR ($2\pi\times2.58$ MHz) and ROCK ($2\pi\times3.49$ MHz) modes undergo increase of 0.08(2) and 0.12(3) phonon respectively.

The results are summarized in Tab. 5.3. The results presented earlier also have very low mean excitation due to swapping, however, the real success of this measurement is a demonstration of swapping at larger transverse trap frequencies. This means with any ongoing shuttling based experiment SWAP operation can be included without lowering the transverse trap frequency. Also in the current experiment, it has been achieved with higher-filter cutoff frequency (τ_{rc}=10 µs) and smaller duration 18 µs, which makes the swap operations 14 µs faster than previously reported result (42 µs). These inclusive experimental achievement provide more effective swap operation in conjugation with other shuttling operations.

5.2.4 Advance swapping of two-ion crystals

In this section, two types of SWAP operations have been discussed. It includes

1. Remote swapping of two-ion crystal
2. Simultaneous swapping of two-ion crystals

Remote swapping of two-ion crystal

During these experiments standard shuttling duration have been used, duration of separation/merge operation, segment-wise transport (for single ion or two-ion crystal), swap operations are 80 µs, 20 µs, and 18 µs, respectively.

Simultaneous remote swapping of two-ion crystals

The success of performing swapping of two-ion crystal at arbitrarily remote segments has been extended to two crystals, where a simultaneous swapping of both crystals confined by two potential wells at the different site of ion-trap has been successfully performed. For these experiments, two crystals of two-ion have been trapped using shuffle load techniques. It is a technique where single ion or ionic crystal is trapped in LIZ and then transported to nearby segment so that another ion or ionic crystal can be trapped at LIZ. Both of these trapping

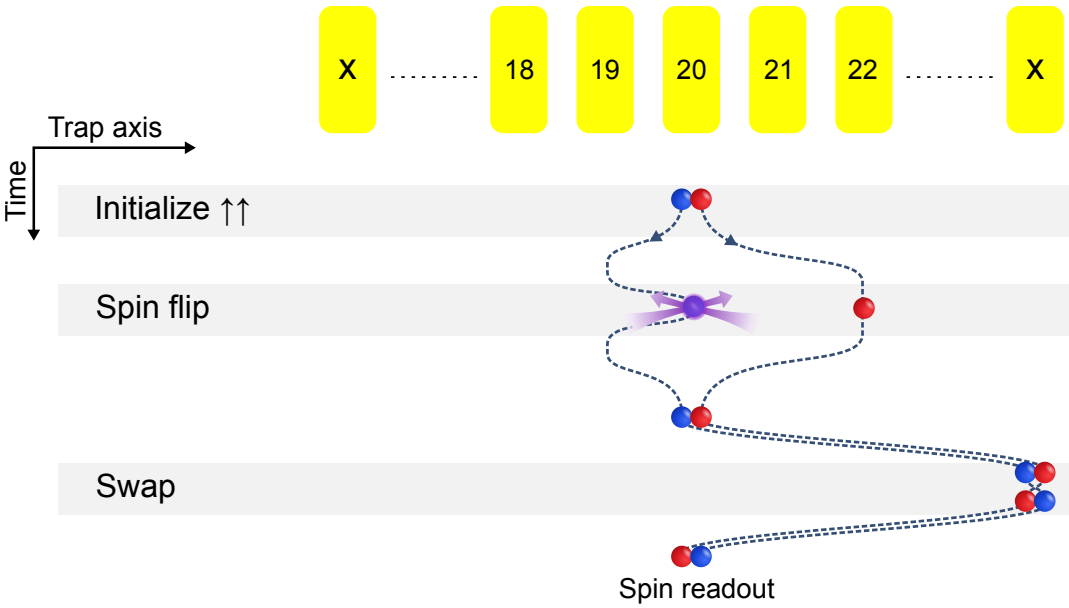


Fig. 5.14 Sequence for the implementation of SWAP operation inside ion-trap. Initially, two ions are initialized to same state, then separated in processing region (LIZ), then ion-A is brought back to LIZ for reversing the spin state, which is followed by merging of ion A and B subsequently at LIZ. The crystal is then transported to a remote segments, for it rotation ((AB) $\rightarrow$ (BA)). Finally, both ions are transported back at LIZ to verify the reversal of spin-state through state-detection. This experiment out-dates the re-positioning of ion crystal at LIZ for swapping (see Fig. 5.15 for success result).

potentials are periodically transported to LIZ for DC to inhibit the chance of losing ions. Both trapped crystals are disassembled into two separate ions, and then first ion from each group is initialized in a different state so that rotation of crystal can be detected. This initialization is sequential. Then, both the ions of same crystal are again merged sequentially and transported to remote segments, where simultaneous rotation with the same parameter as discussed in Sec. 5.2.3, are employed over both the crystal. After rotation, each of the ions is detected sequentially in the same way as it has been initializing. The short description of the sequence is shown in Fig. 5.16, however complete sequence has been presented in Fig. B.1.

For the verification of success of simultaneous swapping multiple test case has been employed. Each point has contained an average of bright probability from 100 test cases.

1. No Swapping
2. Swapping of only first ion crystal (S(AB))
3. Swapping of only second ion crystal (S(CD))

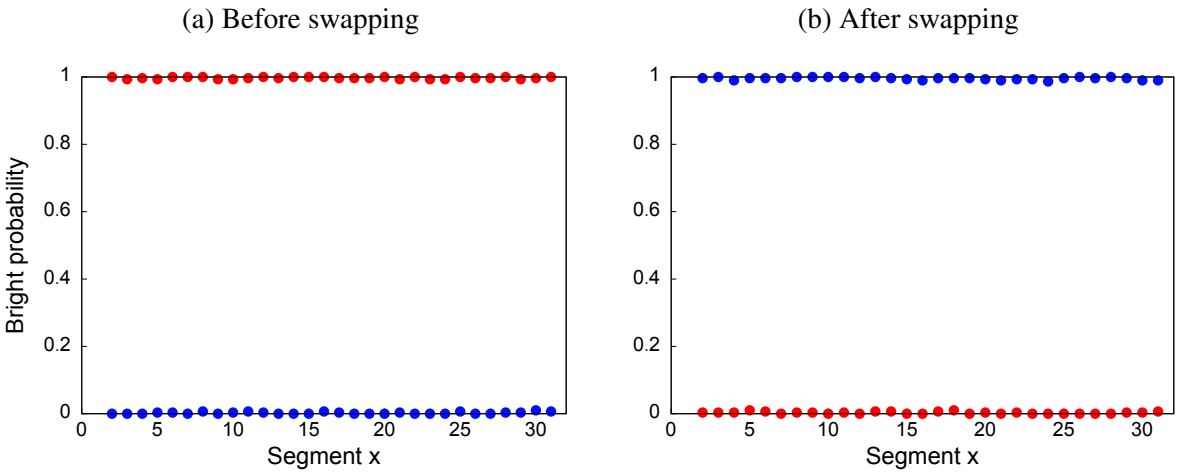


Fig. 5.15 Bright probability of both ions. **(a)** Before swapping, first ion, (green), (initialized in $|\uparrow\rangle$) is detected dark, and second ion(red) ((initialized $|\downarrow\rangle$) is detected bright. **(b)** After swapping, ions interchanges their physical position, so first ion is now detected bright while second ion is dark now. SWAP operation needs three segments, so, it is has been successfully demonstrated from Seg. (2 to 31) (x represents trapping segments).

4. Swapping of both ions crystal (S(AB, CD))

The average of probability measured in all four experiments has been shown in Fig. 5.17.

The ion initialized in the state $|\uparrow\rangle$ shall be detected dark, while the state initialized to $|\downarrow\rangle$ shall be detected bright. In the sequence, ion A (red, ion-A) has been initialized in $|\downarrow\rangle$ state while B (green, ion-B) has been initialized in $|\uparrow\rangle$, while ion C (blue, ion-C) has been initialized in $|\downarrow\rangle$ and ion D (purple, ion-D) has been initialized in $|\uparrow\rangle$. Therefore, in first case, where there was no swapping, red and purple ions are detected bright while green and blue ions are detected dark. While in second case, where swapping is performed over AB only S(AB), green and purple ions are detected bright, while red and blue ions are detected dark. As ion A and ion B have been interchanged. Similarly, when swapping is executed only over CD (S(CD)), ions red and blue ions are detected bright while green and purple are detected dark. Similarly, where swapping sequence is executed over both AB and CD (S(AB and CD)), red andpurple ions are detected dark while other ions are detected bright. Each of the measurement points is result of 100 successful repetition in one row. Which means crystal has been successfully deterministically rotated (or not rotated) for each measurement points.

After the success of simultaneous swap operation, incremental steps to it, two additional experiments have been conducted, first, this operation was tested over a different group of trap

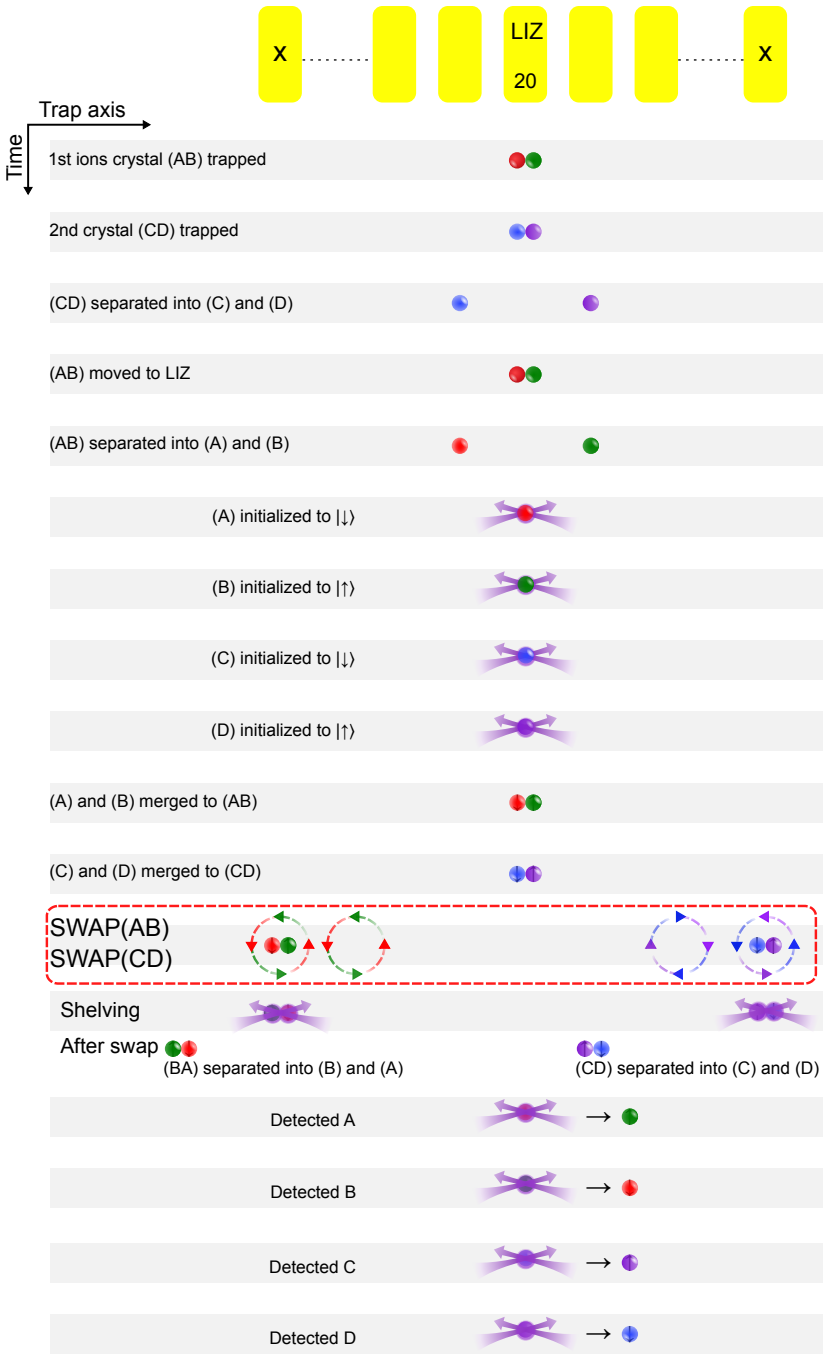


Fig. 5.16 Experimental sequence for simultaneous swapping of two-ion crystal at two remote segments. The segment (shown as x) has been varied across the trap from [2:31], also swapping in either directions (clockwise/anticlockwise) are equally possible. Therefore, it provides a gateway for swapping multiple ionic crystal simultaneously (This image is for illustration purpose, for more detail on sequence see Sec. B.1).

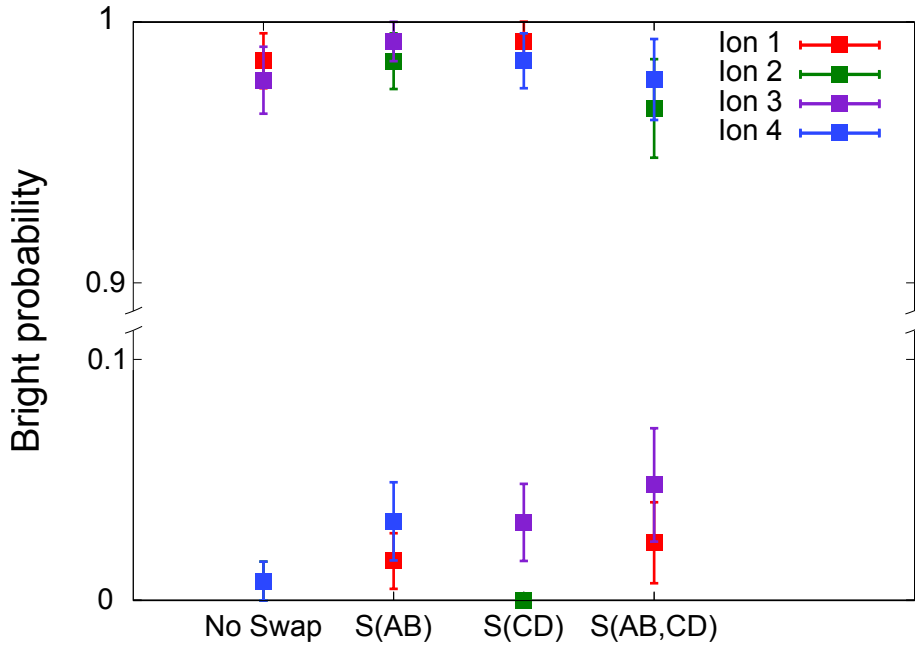


Fig. 5.17 The bright probability after simultaneous remote swapping for two crystals. Multiple test condition (S(AB), S(CD), S(AB, CD)) has been used to ensure that simultaneous swapping of both crystal. In case of no swapping, ion 1 (red) and ion 3 (purple) are detected bright , while ion 2 (green) and ion 4 (blue) are detected dark. For the case when only one crystal is rotated (S(AB)), position A and B interchanges, hence ion 1 (red) and ion 2 (green) are detected dark and bright, respectively. Similarly, for S(CD), only crystal CD rotates hence, ion 3 (purple) and ion 4 (blue) are detected dark and bright, while AB remain as it. And finally when both crystals are rotated (S(AB,CD)), ion 1 (red) and ion 2 (green) are detected dark and bright and ion 3 (purple) and ion 4 (blue) are detected dark and bright simultaneously, respectively. This experiment has been repeated for 100 time for each case and their bright probability are plotted here.

segments (three electrodes are required) and second, rotation of crystal has been tested for all combination of clockwise, anti-clockwise test cases as well.

During multi-segment simultaneous swapping, crystal (AB) has been moved from Seg. 20 to Seg. 2, while other crystal (CD) has been moved from Seg. 21 to Seg. 30, where in all cases the swap operation at any combination of electrode choice with two crystals remain successful. As three segments are needed for the swapping, therefore, a gap of two electrodes has always been maintained during this scan, for example when one of the crystal was at Seg. 20, other crystal stayed at Seg. 23.

The symmetric potential plays an important role in the trap, as while dealing with the multi-ions system, it is needed to balance the electrical potential at the trapping site of static

ions, during the shuttling operation of other ions. Therefore, in more test cases the direction of rotation of crystals has been reversed with respect to each other. The final results, however, remain the same (similar to Fig. 5.17) and also no loss of ions has been observed. The counter rotation of the crystal has been also scanned with segments, showing no change in the final result. However, during the counter rotation of crystal, the voltage ramp on two nearest electrodes (between two crystals) are same, therefore attempt to rotate the crystal using common voltage has been also tried which could not succeed so far. However, I still hope that with fine calibration this shall be possible to do it. The main advantage of counter-rotation of ions crystal is that the minimal number of required segments during the rotation will be reduced to 1, that will be an additional feature added to the quantum processor for scaling of the qubit and its operations.

The total duration of the experimental sequence used to demonstrate simultaneous swapping at remote segments is 34.786 ms, which includes presequence (Doppler, sideband cooling and optical pumping as well for state initialization), the shuttling operations which includes 4 separations, 4 merges, one swap (simultaneous) and multiple transports and post sequence which is readout, similar to as explained in [Kau+16]. More details on exact time spacing have been included in Appendix. B. The time-scale for all the shuttling operations discussed remain same as: Transport (segment-wise) 20 µs, Separation 80 µs and Swapping 18 µs.

Swapping of a larger ionic crystal

After successful demonstration of two-ion swapping in versatile way, another dedicated effort has been tried to realize the swapping of larger ion (three and four) crystal. The major advantage of full reconfiguration of ion crystal by rotation is a reduction of hefty load of unwanted separation and transport operation [Kau+16]from the main sequence, that causes large excitation (especially separation) even though engineered carefully. The recent preliminary result of the success of rotation of larger ion-crystal has been demonstrated.

Trapping of larger ion-crystal in segmented ion-trap is done in two ways. 1.) applying a bath potential i.e by applying -6 V to the neighboring segments (Seg. 20 and 19) such that a wide large harmonic confinement is created that can be used to confine the crystal of more ions along the axial direction. 2.) Using shuffle load, which uses advance shuttling capabilities, by generating two harmonic confinement as explained in the last section. The highlight of shuffle load (ions) can also be used to trap an asymmetric number of ions in similar trapping confinements. Once ion/crystal of both confinements is Doppler cooled, subsequently they are merged to form the larger crystal. Trapping larger crystal using bath potential however possible

but rather proves not so successful. As general methodology adapt to trap ion or ion-crystal is by creating a low depth harmonic bath potential, which is retracted back to normal trapping potential upon trapping. However, while retracting back to normal trapping potential at $-6.0\,\mathrm{V}$, due to background collision or insufficient cooling, it was impossible to get the linear crystal. The zigzag crystal [Ulm+13] was more common during trapping of larger ion crystal.

During the rotation, three-ion crystal (ABC) reconfigure itself as (BCA). For experimentally determining the deterministic rotation of it three different experiments has been performed. In first experiment, ion A of crystal (ABC) is initialized into $|\downarrow\rangle$ while other ions in $|\uparrow\rangle$ state. Similarly, for other two experiments ion B and c are $|\downarrow\rangle$ and others into $|\uparrow\rangle$ respectively. And subsequently each of the three sets has been test with and without implementation of swap-sequence.

Swapping of a three-ion crystal

The exact experimental sequence follows as: In two distinct potential well single and double ions are trapped (Shuffle load). Thereafter, a separation sequence is applied over double ions which separate out two-ion crystal into a single ion. Now, during the first test condition ion, A is initialized to spin down state while initializing other ions in the spin-up state as said. Then merge sequence is implemented which leads to merging of two ions initially and subsequently third ions is added to it in using the same sequence. This allows it to accommodate three-ion crystal in well initialized state $|\downarrow\uparrow\uparrow\rangle$ then swap sequence is applied that rearranges the crystal in $|\uparrow\uparrow\downarrow\rangle$. After rotation, three-ion crystal is fragmented into two-ion crystal and single ion and then into an individual ion. Each ion is shelved and then final spin readout is conducted in the same sequential order has been followed during initialization. The experiment is repeated for the other two cases in which one of the ions is initialized differently and spin readout follows the order of initialization. All three experiments confirm that no crystal re-arrangement is taking place two between ion with identical spins.

The successful rotation of three-ion crystal has been observed with similar voltage ramp as of two-ion crystal rotation (See Fig. 5.13) at Seg. 20 with swap-duration of 18 µs, but the short duration was causing large heating of the crystal that even the read-out was compromised to 50-60%. However, with larger swap-duration of 200 µs, heating of crystal can be attenuated, the contrast improved to ~095%. Spin-flip of ion A yielded contrast of 0.95% after swapping, while that of ion B and C yielded to ~0.85 and ~0.75, respectively. The experimental parameter are t1 = 0.05, t2=0.45, t3= 0.55, t4= 0.95, U_c=-18.7 V, U_d=2.2 V and U_d=0 V. Spin of each ion in three-ion crystal has been flipped sequentially for testing swap and non-swap cases and

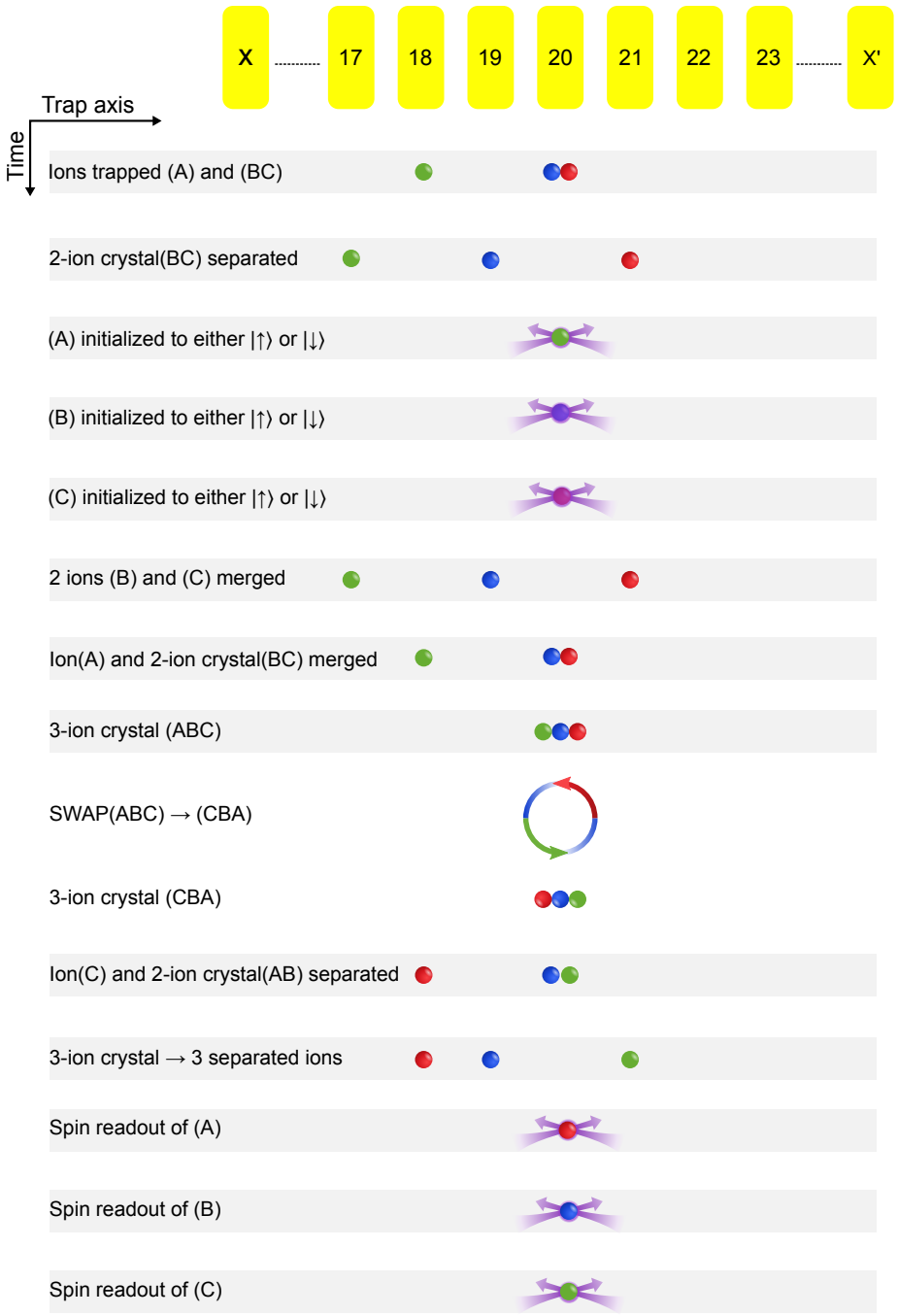


Fig. 5.18 Experimental sequence for swapping of a three-ion crystal

successful validating the rotation of crystal as single entity (see Fig. 5.20) without leading to any zigzag configuration [Ulm+13]. The results of bright probability for both cases has been shown in Fig. 5.20. Summary of final result has been shown in Fig. 5.19.

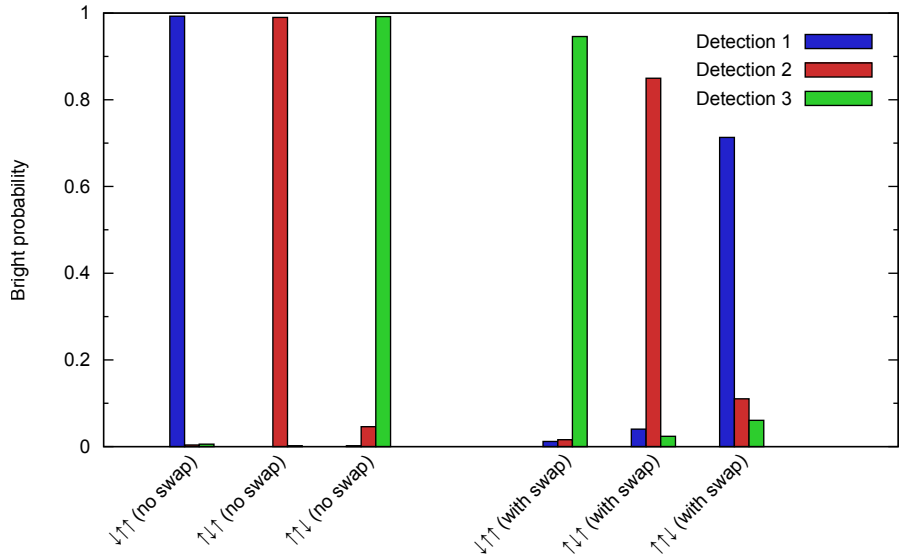


Fig. 5.19 Bright probability recorded before (first three from left) and after (others) swapping of the three-ion crystal. Ion initialized in state $|\downarrow\rangle$ is detected bright while $|\uparrow\rangle$ ions are dark. Each color blue, red, green represents ions at left,center,right position of a three-ion crystal. After swapping, position of ions are exchanged so blue become green(first and fourth from left in plot) and vice-versa, red remain unchanged (center ion). Three possible test cases ($|\downarrow\uparrow\uparrow\rangle$, $|\uparrow\downarrow\uparrow\rangle$,$|\uparrow\uparrow\downarrow\rangle$) have been verified by swapping and not swapping alternately during the experiments. The readout contrast of average bright probability is measured from successive 100 swapping on a three-ion crystal.

Swapping of a four-ion crystal

Swapping of four-ion crystal reconfigure crystal from configuration (ABCD) to (DCBA) or vice versa ((ABCD) $\leftrightarrow$ (CDBA)). It is an incremental step of three-ion crystal rotation. Like the previous sequence, in this case, also ions are trapped through shuffle load process, where each of potential well traps a two-ion crystal and then merge them to form a larger a four-ion crystal. The experimental parameter remains the same as of three ion crystal rotation. The spin of each ion in the four-ion crystal has been flipped sequentially for testing swap and non-swap cases for successful validation of crystal rotation as a single entity (see Fig. 5.20) without leading to any zigzag configuration [Ulm+13]. Results of bright probabilities for both cases has been shown in Fig. 5.20.

The general ion loss-rate observed during the measurements are 0.002% [Kau+19]. The figure of merit of this shuttling based quantum processor node has been summarized in see Tab. 5.4.

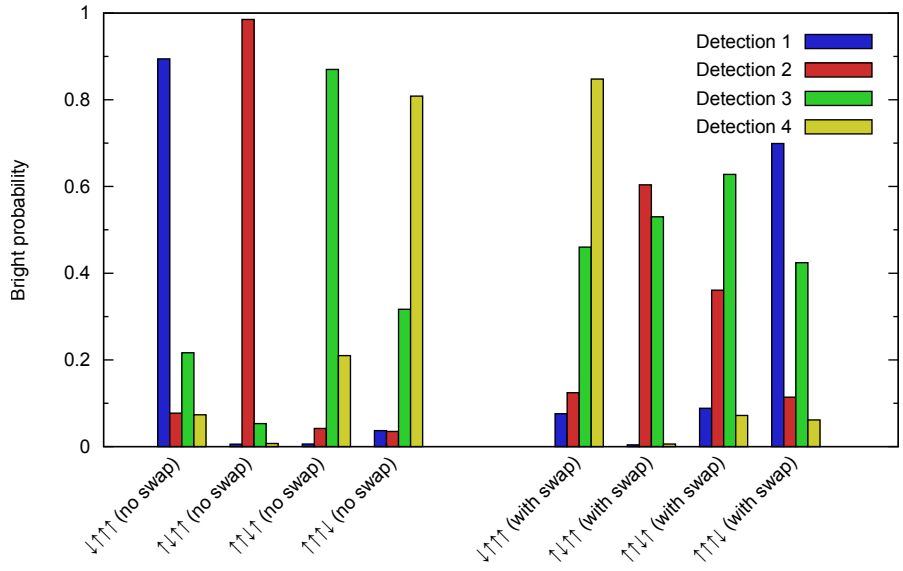


Fig. 5.20 Bright probability recorded before (first four from left) and after (other) swapping of a four-ion crystal. Measurement methods is an extension of three-ion crystal swapping (see Fig. 5.19), where relative placement of all ions are distinguished by different colors. Similarly, after swapping of four-ion crystal, ions positions (1(blue)↔4(yellow)) and (2(red)↔3(green)) are interchanged. In this case, four possible test cases ($|\downarrow\uparrow\uparrow\uparrow\rangle$, $|\uparrow\downarrow\uparrow\uparrow\rangle$,$|\uparrow\uparrow\downarrow\uparrow\rangle$, $|\uparrow\uparrow\uparrow\downarrow\rangle$) have been verified by swapping and not swapping alternately during the experiments. The readout contrast is average bright probability from successive 100 swap operation, as done in case of three-ion crystal. The readout contrast is limited as rotation of larger crystal causes large heating of crystal.

Table 5.4 The properties of shuttling based trapped-ion quantum processing node. The anticipated values are taken from [Ber+17].

Trap characteristic	ax ($\omega_x/2\pi$=1.48 MHz)	trans1 ($\omega_y/2\pi$=3.8 MHz)	trans2 ($\omega_z/2\pi$=4.6 MHz)		*status*
Heating rate (in ph/s with f_c=100 kHz)	9(1)	26.6(7)	9.2(3)	-	*experimental*
Motional coherence (in ms, with ac-line sync)	57(9)	11.6(5)	24(1)	-	*experimental*
Motional coherence (in ms, $\sim 1/\dot{\bar{n}}$)	111	37.5	108	-	*theoretical*
Shuttling operation	Motional excitation(in ph)			duration (μs)	
Transport (one segment)	~1 ~0.2	~0.1 ~0.01	~0.1 ~0.01	10 5	*experimental* *anticipated*
Separation/Merge of two-ion crystal	~6 ~1	~0.1 ~0.1	~0.1 ~0.1	60 (ax),50 (trans) 30	*experimental* *anticipated*
Swapping (or rotation) of two-ion crystal	~0.10(3) ~0.2	~0.01(3) ~0.1	~0.04(2) ~0.1	28 20	*experimental* *anticipated*
Multi-site swapping of multiple crystals (two-ion)	NA	NA	NA	28	NA

6

Conclusion and outlook

We have realized a small quantum processing node, capable of storing and rearranging up to about 10-12 trapped ion qubits and manipulating them at high fidelity. In order to realize a fully functional quantum processing node which can be integrated in a quantum network, some additional steps of demanding complexity have to be taken. However, the roadmap and details on how to proceed are already quite clear, and some of these steps have been already been successfully realized by other groups. We list the most important steps in the following:

1. **Fidelities**: In order to comfortably fall below a suitable fault-tolerance threshold, the entangling gate fidelities and their resilience against motional excitation needs to be improved. Increasing the available UV laser power for the gate drive, it is possible to remove the fidelity bottleneck given by spontaneous scattering. It is then crucial to identify the persisting bottlenecks and eventually mitigate these. In particular, we aim at designing composite pulse sequences for making the gate operations resilient against coherent excitation on gate and spectator modes. In order to allow for longer circuit depths, the qubit coherence time needs to be further extended. The remarkably long coherence times achieved using hyperfine qubits, e.g. $^{43}Ca^{+}$ [Har+14], together with ultra-stable magnetic fields [Rus+16], would essentially remove any limit imposed by magnetic field-induced qubit frequency drift.

2. **Multi-species**: At least one additional ion species is required to enable sympathetic cooling and scalable qubit readout. Both schemes are based on the fact that the auxiliary ion species allows for resonant driving with light which is far off-resonant to any relevant optical dipole transition of the qubit species. Sympathetic cooling refers to resolved sideband cooling on a mixed Coulomb crystal, where the qubit ions - although not being driven - are also cooled via energy exchange due to the strong Coulomb coupling to the

coolant species. A fast, efficient sympathetic cooling scheme has been realized by the NIST group [Lin+13]. On a single-species register, in-sequence readout of a subset of qubits, in particular for error detection purposes, is hardly possible. A single photon scattered by a remotely stored spectator qubit from laser light scattered from the trap leads to an undesired projective measurement on it. The solution is to perform the readout on an auxiliary species, after performing a hybrid SWAP-gate between the qubit to be read out and the auxiliary qubit. This has been successfully demonstrated by the groups at NIST, in Oxford and in Zurich [Tan+15; Bal+15; Neg+18]. However, adding an auxiliary species will lead to a substantial complexity increase in controlling the shuttling operations: Asymmetric masses for instance lead to excitation of the out-of-phase mode for linear transport of a two-ion crystal [Pal+14], center-of-mass shift upon swapping caused by the mass-dependence of the ponderomotive force, or arrangement-dependent ion position shifts due to residual axial ponderomotive forces [Hom13].

3. **Feed-forward**: Quantum error correction requires the capability of performing conditional branching of computational sequences based on the results of in-sequence measurement results. Basic demonstrations of quantum teleportation or error correction protocols have already demonstrated such operations [Rie+04; Sch+11; Neg+18]. In these demonstrations, the conditional operations consisted of performing or not performing single qubit rotations, including control of the phase. For the shuttling based approach, a suitable execution control hard- and software system would need to be able to conduct arbitrary branched sequences composed of shuttling and gate operations. This development is currently underway and requires complete restructuring of the sequence generation interface and software, the hardware sequence protocols and their storage, the execution control on the SoC, the photon detection hardware and data evaluation software, and the rf pulse generation for laser pulse control.

4. **Storage capacity**: The storage capacity of the currently employed trap will likely not be sufficient for applications beyond quantum repeater nodes. About a decade ago, surface electrode traps have been established [Sei+06]. These traps are based on fabrication methods adapted from the semiconductor industry, and therefore allow for arbitrary electrode structures [Ami+10] at small dimensions and excellent precision. While this technology has continuously improved, and elements such as X- [Wri+13] or Y-junctions [Moe+11; Shu+14], trap slits and island electrodes connected through vias are now available. This allows for decreasing the overall dimensions and increasing the number of trap electrodes. Still, due to the reduced symmetry, these traps are more challenging to operate as compared to their multilayer counterparts. The ion proximity to surfaces

is generally closer, which leads to increased heating [BKW18], and the more shallow potentials lead to increased loss rates. Therefore, surface electrode traps will likely require a cryogenic environment for proper operation.

5. **Cryogenic environment**: Cooling an ion trap to liquid Helium temperatures can offer a number of significant advantages. Freeze-out of residual background gas reduces collision induced ion losses or decrystallization events. Even more importantly, it has been shown that surface noise-induced anomalous heating can be significantly suppressed at cryogenic temperatures [Des+06; Lab+08; BSC15]. Furthermore, suitable cryogenic shielding around the ion trap can strongly suppress ac magnetic field fluctuations, which can drastically enhance the performance of magnetic field sensitive qubits [Bra+16]. In our group, efforts on setting up a Sandia HOA-2 surface electrode trap in a cryogenic environment are currently underway.

6. **Programmability**: Despite similar performance parameters as compared to static string-based architectures [Sch+13; Deb+16], our architecture currently lacks the capability of easy compilation of a given quantum circuit into a sequence of hardware instructions. This problem can be broken down into two problems, which can be solved sequentially: First, a quantum circuit needs to be translated into a schedule of register reconfiguration operations, i.e. it needs to be determined which ions should be placed into a LIZ in which temporal order. This problem is constrained by the presence of the spectator ions and the storage properties of the trap, and invariant against an initial and final permutation of the qubits. This represents a logistics problem, and it is currently unclear if it can be formulated such that its complexity class allows for efficiently obtaining solutions on classical computers. The second, more tractable problem consists of computing voltage waveforms for realizing a given shuttling sequence. This task can again broken down into two optimization problems: First, voltage sets realizing a given confinement configuration are obtained, and the shuttling sequence results from interpolation between these solutions. The next stage consists of mapping these interpolated voltage sets onto an actual time to obtain time-dependent voltage waveforms which comply with the available hardware resources and lead to minimized motional excitation of the ions. Efforts for realizing such a software framework are currently underway.

7. **Interfaces**: A conceivable realization of a full-blown trapped ion quantum computer *outperforming classical computers with useful tasks* could consist of an array of automated, identical processing / storage nodes each consisting of one ion trap, which is interconnected via photonic interfaces. Such interfaces could consist of free-space or cavity-enhanced coupling to optical radiation. In both cases, controllable high numer-

ical aperture access to trapped ions is ultimately required. The technical realization at sufficient coupling rates, fidelity and interoperability with the trap remains challenging. Several research groups pursue the quest for free-space [Str+11; Huc+14] or cavity-based [Bra+13; Pfi+16] optical interfaces. Note that segmented trap in conjunction with ion shuttling is a natural fit to such interfaces, as the shuttling allows for controlled coupling of selected ions to the photonic bus.

While the steps outline above and the integration into one platform are challenging, they currently seem to be feasible. An optically connected network of 10 quantum processing nodes each bearing 10-100 trapped-ion qubits is definitely within reach and could be realized within the next one or two decades. Such an apparatus would already allow for outperforming classical computing hardware on useful task such as computing molecular energy structures [Hem+18]. As the operational timescales of such are platform will be dominated by the shuttling-induced overhead, which is in turn tied to the timescales imposed by the secular trap frequencies, such an architecture will not be competitive to e.g. superconducting platforms in terms of operational speed. However, the performance advantage of a quantum computer is given by its intrinsic *quantum parallelism*, it is promising to keep on pursuing this approach.

List of scientific publications

- "A shuttling-based trapped-ion quantum processing node". V. Kaushal, D. von Lindenfels, C. T. Schmiegelow, J. Schulz, F. Schmidt-Kaler, and U. G. Poschinger. In: *Unpublished manuscript under preparation* (2019).

- "Cryogenic setup for trapped ion quantum computing". M. F. Brandl, M. W. van Mourik, L. Postler, A. Nolf, K. Lakhmanskiy, R. R. Paiva, S. Möller, N. Daniilidis, H. Häffner, V. Kaushal, T. Ruster, C. Warschburger, H. Kaufmann, U. G. Poschinger, F. Schmidt-Kaler, P. Schindler, T. Monz, and R. Blatt. In: *Review of Scientific Instruments* 87.11 (2016), p. 113103.

- "Fast ion swapping for quantum information processing". H Kaufmann, T Ruster, C T Schmiegelow, M A Luda, V Kaushal, J Schulz, D von Lindenfels, F Schmidt-Kaler, and U G Poschinger. In: *arXiv:1607.03734* (2016).

- "Scalable Creation of Long-Lived Multipartite Entanglement". H. Kaufmann, T. Ruster, C. T. Schmiegelow, M. A. Luda, V. Kaushal, J. Schulz, D. von Lindenfels, F. Schmidt-Kaler, and U. G. Poschinger. In: *Phys. Rev. Lett.* 119 (15 Oct. 2017), p. 150503.

- "Experimental realization of fast ion separation in segmented Paul traps". T. Ruster, C. Warschburger, H. Kaufmann, C. T. Schmiegelow, A. Walther, M. Hettrich, A. Pfister, V. Kaushal, F. Schmidt-Kaler, and U. G. Poschinger. In: *Phys. Rev. A* 90 (2014), p. 033410.

- "Entanglement-Based dc Magnetometry with Separated Ions". T. Ruster, H. Kaufmann, M. A. Luda, V. Kaushal, C. T. Schmiegelow, F. Schmidt-Kaler, and U. G. Poschinger. In: *Phys. Rev. X* 7 (3 Sept. 2017), p. 031050.

- "Phase-Stable Free-Space Optical Lattices for Trapped Ions". C. T. Schmiegelow, H. Kaufmann, T. Ruster, J. Schulz, V. Kaushal, M. Hettrich, F. Schmidt-Kaler, and U. G. Poschinger. In: *Phys. Rev. Lett.* 116 (3 Jan. 2016), p. 033002.

- "A spin heat engine coupled to a harmonic-oscillator flywheel". David Von Lindenfels, Oliver Gräb, Christian T. Schmiegelow, Vidyut Kaushal, Jonas Schulz, Ferdinand Schmidt-Kaler, and Ulrich G. Poschinger. In: *arXiv e-prints* (Aug. 2018).

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A

Experimental data

Motional coherence

Fit equation used in the mathematica for fit the data recorded during measurement of contrast decay for the spin-motion superposition state (motional coherence see Fig. 3.11).

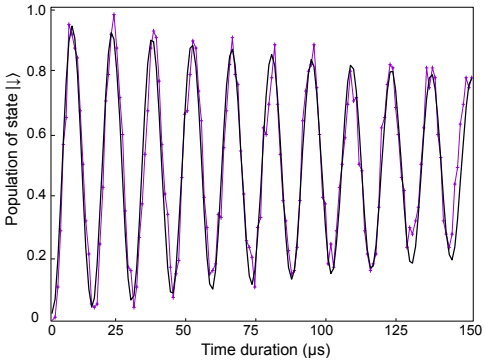
$$f(x) = a.\exp\left(bx + cx^2\right) \tag{A.1}$$

Motional modes	**LT**	**fit parameters**		
		a	b	c
Rad2	enabled	0.976524	-50.4697	401.705
Rad2	–	0.967792	-134.629	- 3408.32
Rad1	enabled	0.96148	-81.4483	- 370.852
Rad1	–	1.00728	-226.154	1545.13
ax	enabled	0.920217	-20.6212	52.9364
ax	–	0.950789	-22.8034	192.5512

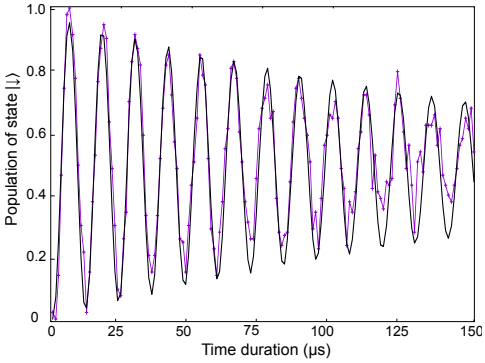
Separation of two-ions crystal:Recorded Rabi-flops

transverse (50 µs)

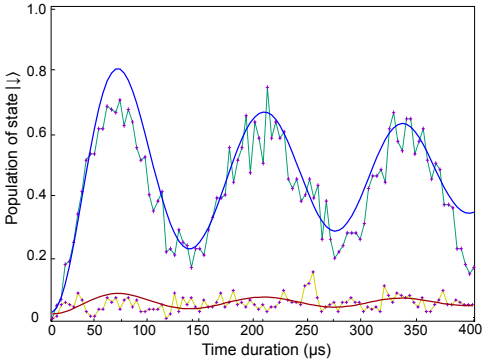
(a) trans2/trans1→ion1→car



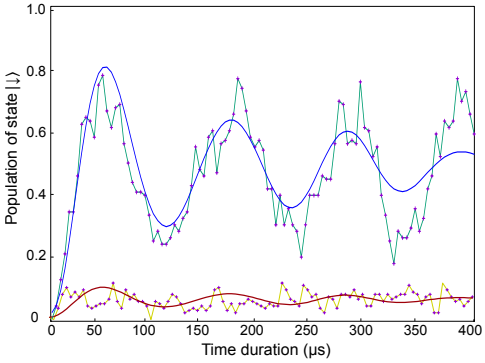
(b) trans2/trans1→ion2→car



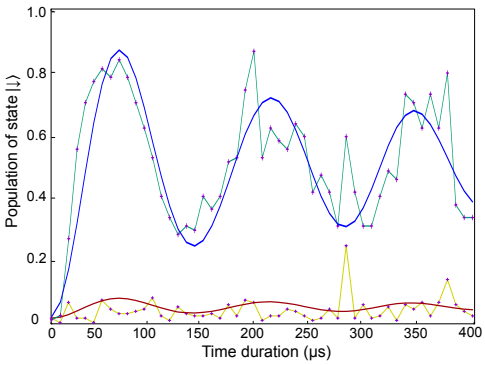
(c) trans2→ion1→rsb&bsb



(d) trans2→ion2→rsb&bsb



(e) trans1→ion1→car



(f) trans1→ion2→rsb&bsb

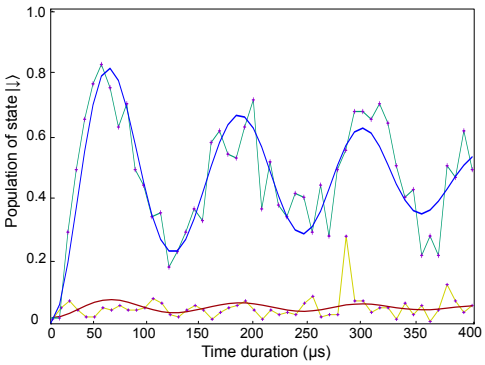
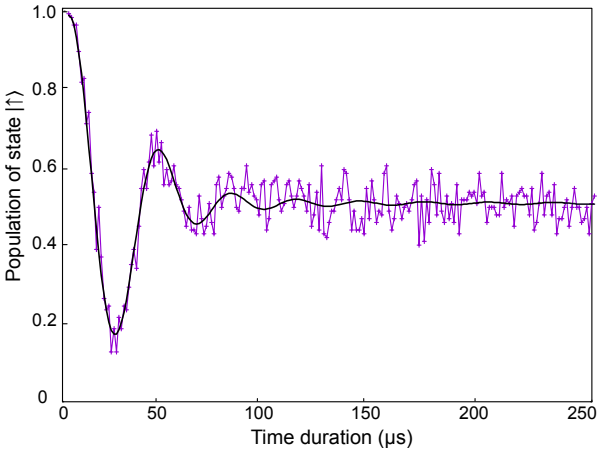


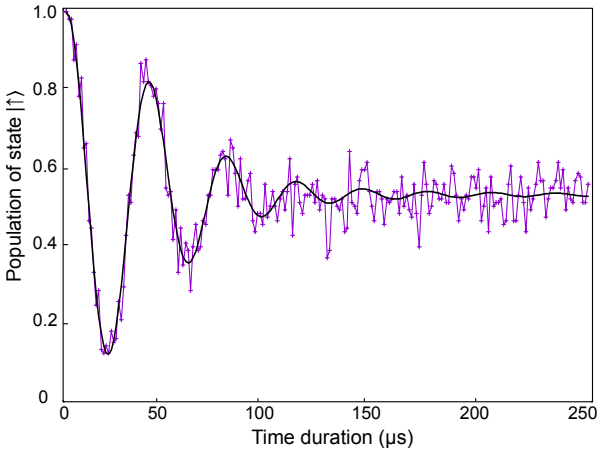
Fig. A.1 Rabi oscillation recorded at for both ions on both transverse modes (trans1 and trans2) during the separation of two-ion crystal in 45 µs. For both ion car frequency are same for their respective transverse modes, while rsb and bsb for both ions of both modes are distinct. Black is the fit to the recorded data (dark-violet) of car frequency in both top-most plots, while blue/red are fit to their respective bsb (green)/rsb (yellow) recorded data.

Axial (60 µs)

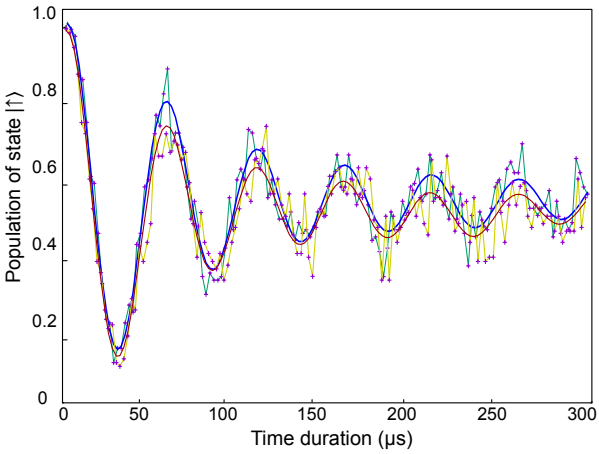
(a) ax→ion1→car



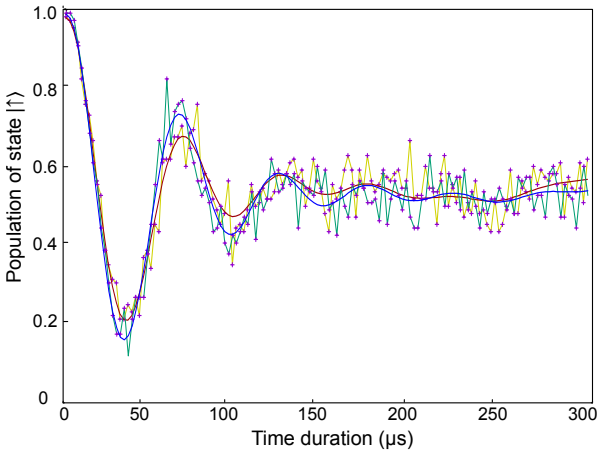
(b) ax→ion2→car



(a) ax→ion1→bsb&rsb



(b) ax→ion2→rsb&bsb



Swapping of two-ions crystal:Recorded Rabi-flops

Transverse

(18 µs)

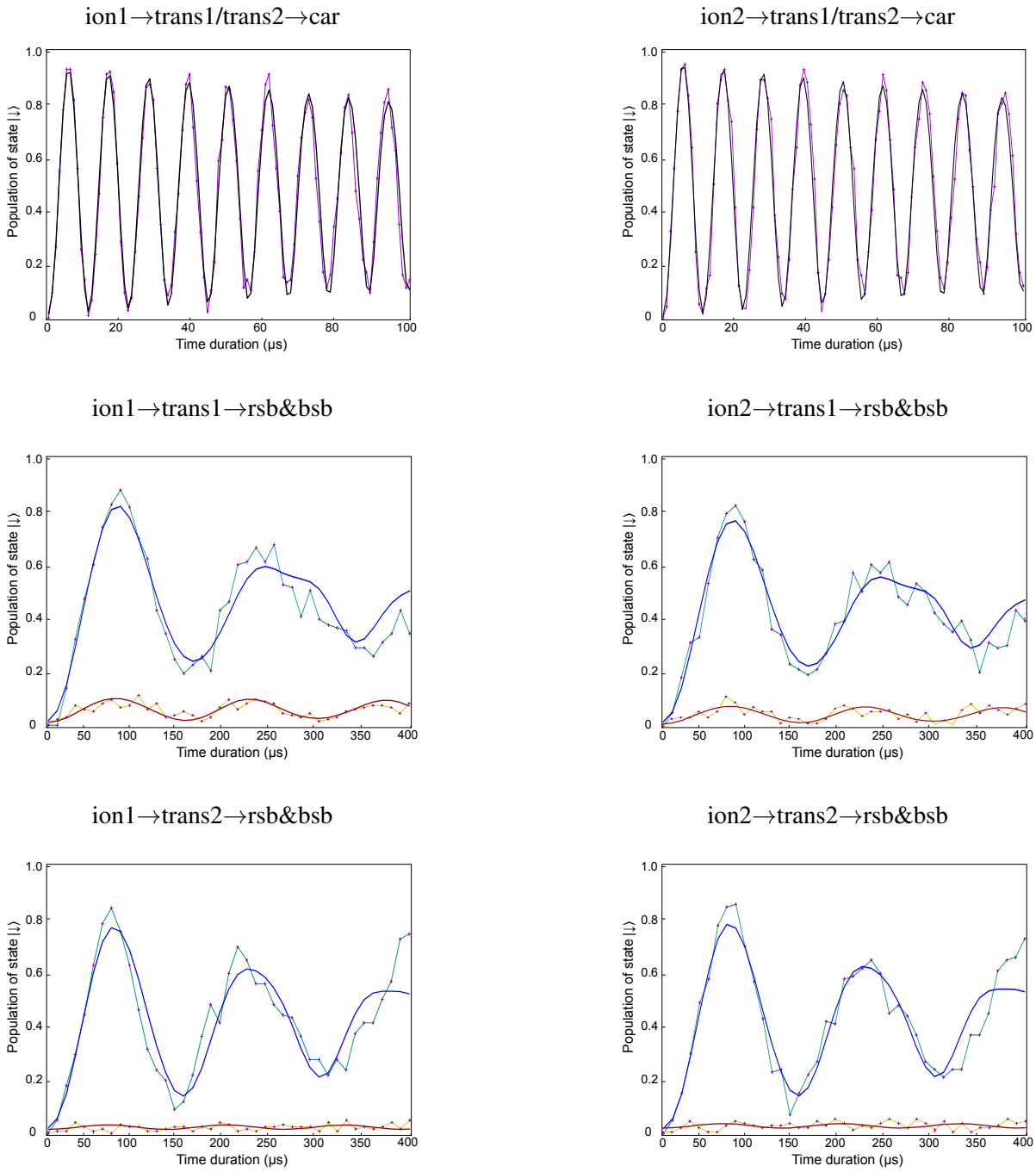
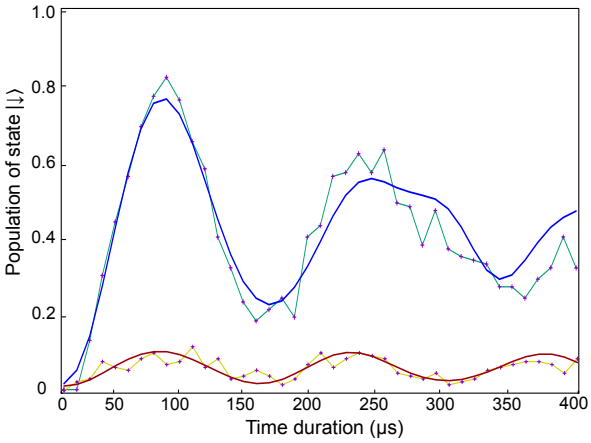
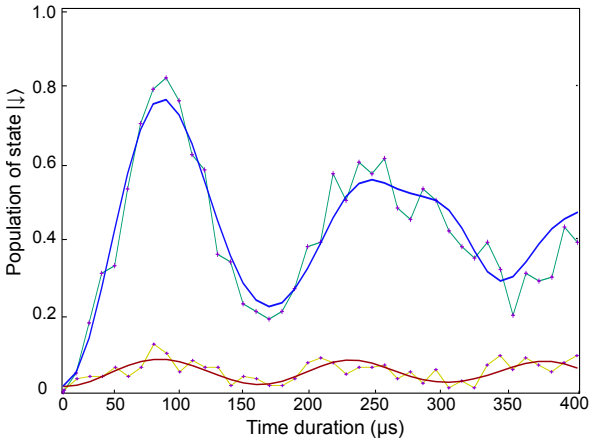


Fig. A.4 Rabi oscillation recorded on the transverse COM (center of mass) mode after swapping of two-ions crystal at 28 μs.This two ion-crystal swapping duration (28 μs) includes the low pass filter time-constant (τ_{RC}) of 10 μs, and actual swap duration of 18 μs.

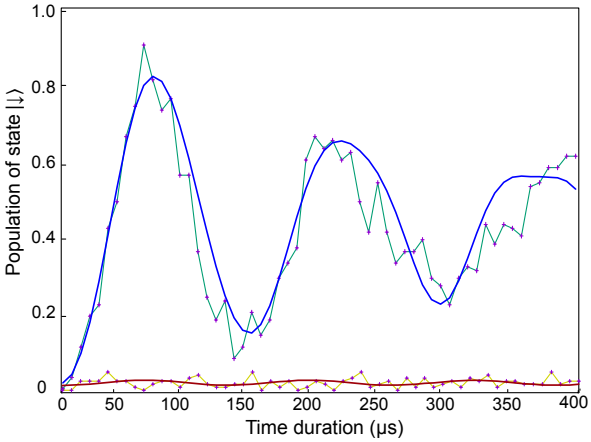
ion1→trans1rock→rsb&bsb



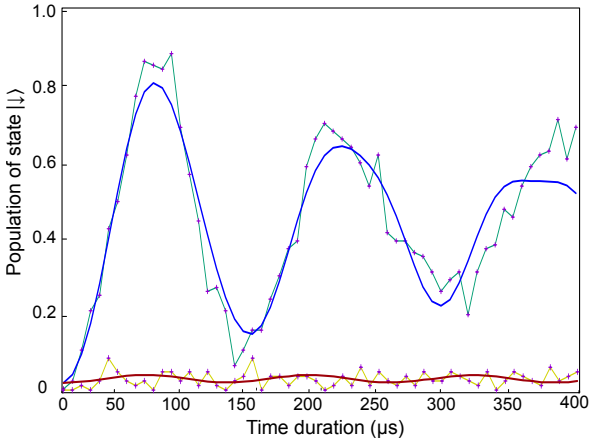
ion2→trans1rock→rsb&bsb



ion1→trans2rock→rsb&bsb

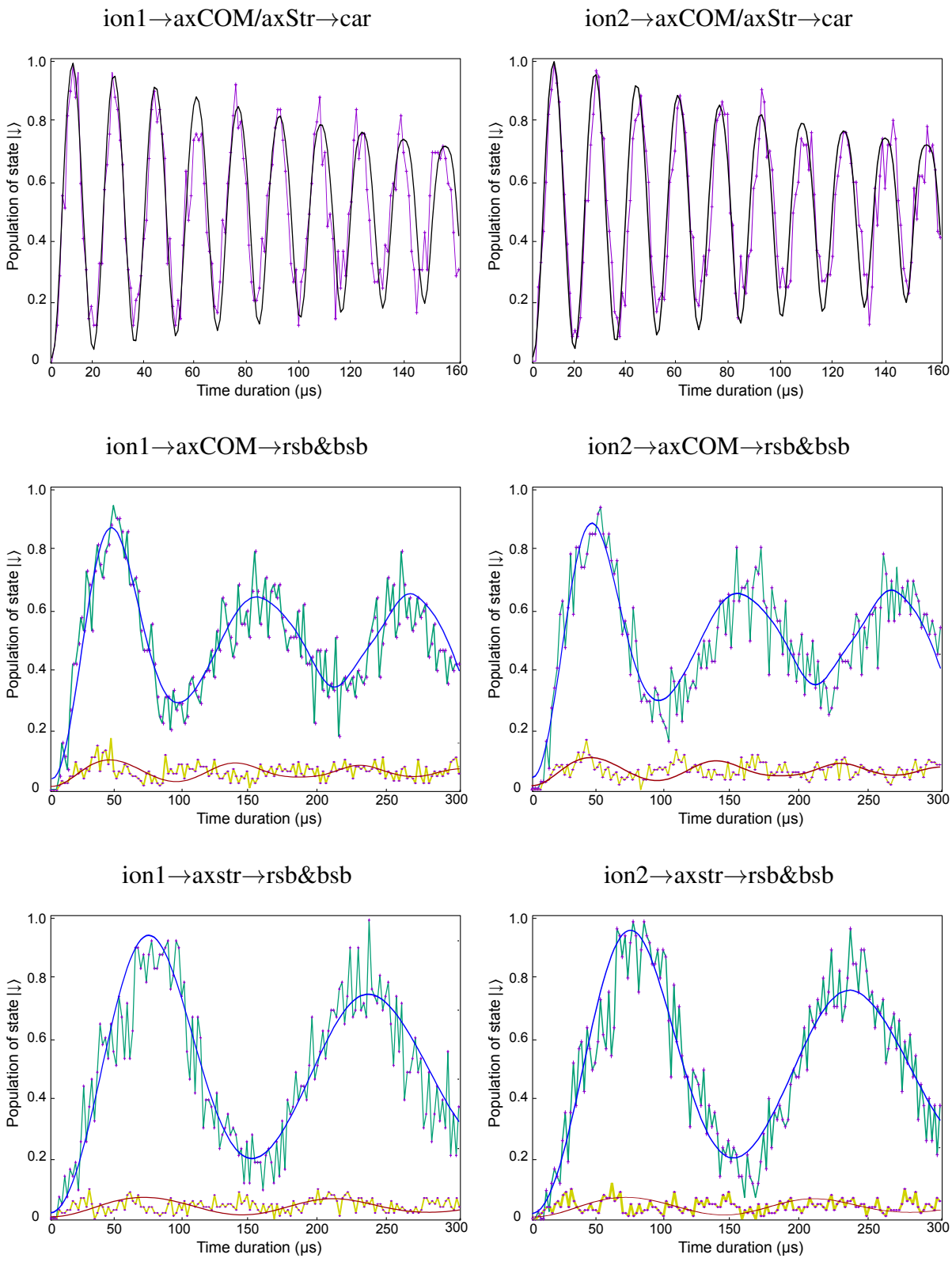


ion2→rad2rock→rsb&bsb



Rabi oscillation recorded on the transverse rock (rock mode) mode after the swapping of two ion crystal in 28 μs. This two ion-crystal swapping duration (28 μs) includes the low pass filter time-constant(τ_{RC}) of 10 μs, and actual swap duration of 18 μs.

Axial



Rabi oscillation recorded on the axial COM (center of mass)/str mode after swapping of two-ions crystal at 28 μs.This two ion-crystal swapping duration (28 μs) includes the low pass filter time-constant (τ_{RC}) of 10 μs, and actual swap duration of 18 μs.

B

Experimental sequence

Remote parallel swapping of two crystal

Total duration of experimental sequence: 34.78620 ms. Assuming that experimental sequence has started at t=0, the time-line for progress of it is as follows.

Sequence	Event	Time (ms)	Comment
Pre-sequence	Trapping and Doppler-cooling of two double ions(*Shuffle* load)	ends at 6.33	Crystal (AB) and (CD) trapped S1(see Sec. B.1)
Main-sequence	*first separation*	ends at 6.41	Crystal *(CD)* separating into C and D in 80 µs. Sub-sequence S2 and S3(see Sec. B.1)
	second separation	ends at 11.49	Crystal *(AB)* separating into A and B in 80 µs. Sub-sequence S4 and S5(see Sec. B.1)
	third merge (inverse separation)	ends at 13.87	ions A and B merged into (AB) in 80 µs. Sub-sequence S10 and S11(see Sec. B.1)
	fourth merge (inverse separation)	ends at 14.49	ions C and D merged into (CD) in 80 µs. Sub-sequence S12 and S13(see Sec. B.1)
Readout	*simultaneous swap* $(AB)\rightarrow(BA)$ and $(CD)\rightarrow(DC)$	starts at 14.743 ends 14.761	Crystal reconfiguration in 18 µs(see Sec. B.1)
	fifth separation	ends at 15.06	Crystal *(AB)* separating into A and B in 80 µs. Sub-sequence S2 and S3(see Sec. B.1)
	sixth separation	ends at 15.66	Crystal *(CD)* separating into C and D in 80 µs. Sub-sequence S2 and S3(see Sec. B.1)
	seventh merge (inverse separation)	ends at 27.76	ions C and D merged into (CD) in 80 µs. Sub-sequence S31 and S32(see Sec. B.1)
	eighth Merge (inverse separation)	ends at 31.36	ions C and D merged into (CD) in 80 µs. Sub-sequence S33 and S34(see Sec. B.1)
Readout	Trapping and Doppler-cooling of two double ions(*Shuffle* load)	6.33	–

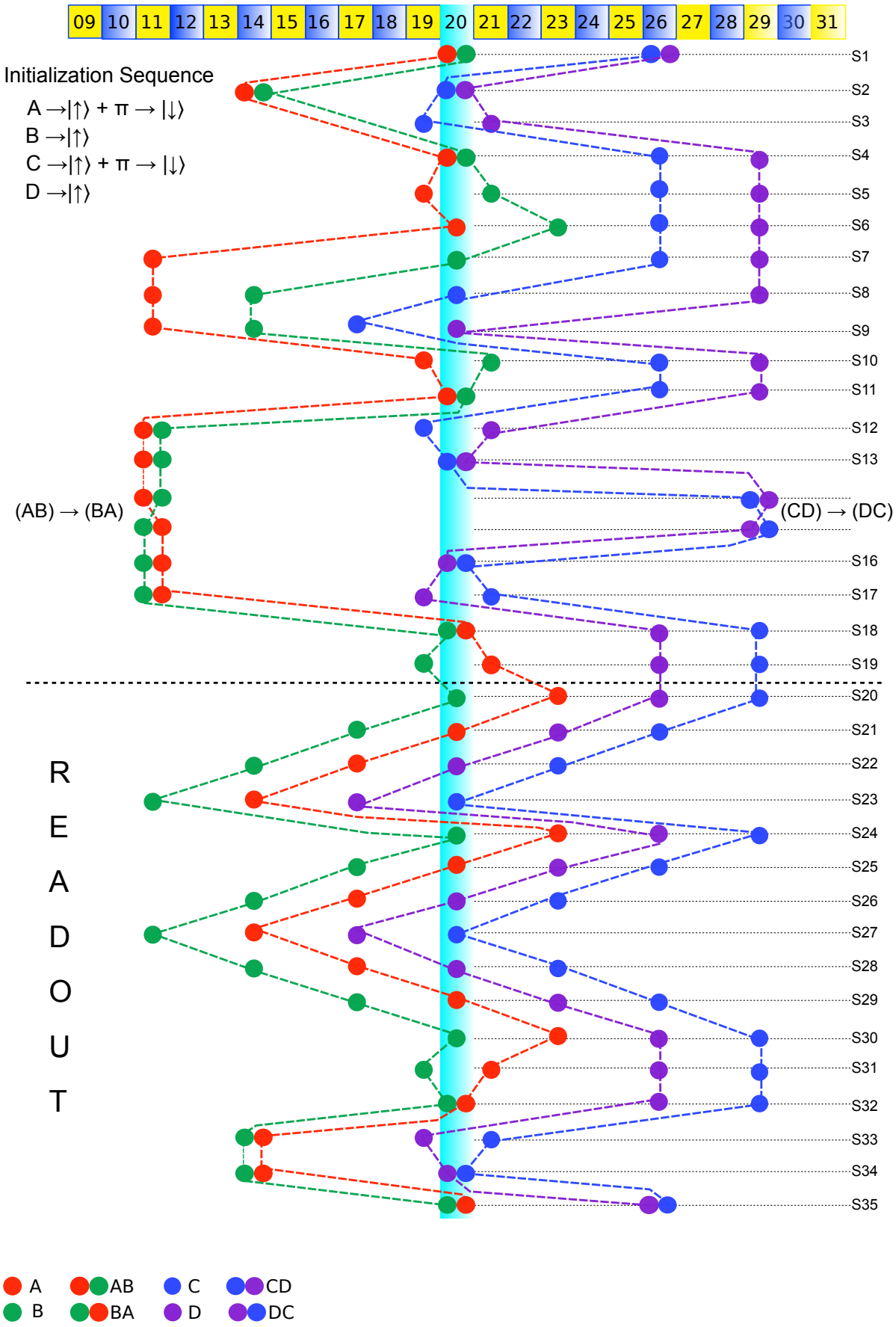


Fig. B.1 Sequence demonstrating simultaneous swapping of two-units of two-ions crystal. The reconfiguration of ions crystal, AB as BA (AB → BC),CD as DC (CD → DC) are done simultaneously.

C

FPGA based experimental control for scalable quantum operations in segmented ion-traps

Introduction

The experiments based on trapped ion quantum system is still challenging, although several milestones in the direction of scaling such systems [Haf+05; Kau+17; Mon+16] have been achieved in the last decade. The idea, to design a scalable segment controller is motivated to meet the demand of on-growing experimental resources and to scale up storage of trapped-ion qubits inside segmented ion-trap [Shu+14; Mau16]. Scaling of qubits in ion-trap requires many individual electrodes to control independent positioning of each qubit. The trapped-ion qubits inside segmented ion traps are controlled by changing time-dependent voltages on individual electrodes. I hope that current design (discussed in this thesis), can also be used with other trap architecture [Bla+09; Wri+13]. It is useful for supporting basic shuttling operations of trapped ions and also to shape laser pulse for implementation of necessary quantum logic gates with shuttling operations. The latest programmable System on Chip (SoC) architecture based on FPGA embedded technology has been used as heart of this experimental control system. Through systematic approach, multiple segments of the design have been developed separately and concatenated at the end, for its realization. It has also been tested as an advanced mAWG successfully and thus, addressed as New Bertha (N_Bertha) (see Fig. C.1) throughout this thesis. Multiple segments of N_Bertha can be divided into six sections as, Analog unit, Digital unit, Internal Power unit, Programmable Device unit, Mains power supply, and a digital line

distribution unit.

The primary function of N_Bertha is to provide independent and simultaneous control of 80 analog power supply channels, that can be connected to several trapping electrodes of any segmented ion-trap to support parallel shuttling operation, along with 24 digital channels (TTL pulses) to control laser pulse duration. The idea of managing digital and analog channels from the same device facilitates correlated control of laser-induced gate-operation and shuttling of ion(s) crystal. There is also a provision of synchronizing all analog channels and digital pulse sequencer with an external signal. Multiple units of N_Bertha can also be connected to support fully scalable architecture for large-scale quantum computing. The actual implementation for scaling it (N_Bertha), beyond the single entity (80 analog and 24 digital channels) is based on the master-slave configuration (see Sec. D.3). It can also be understood as a similar effort [Rya+17] in designing a complete hardware solution, especially for segmented ion-traps. Detail discussion of different units have been presented in subsequent sections.

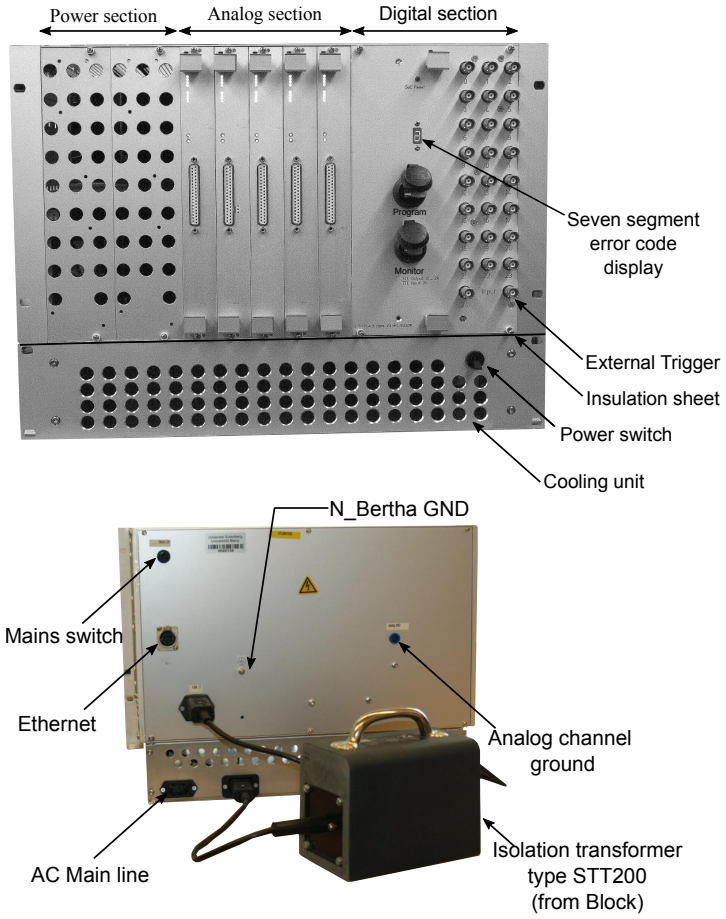


Fig. C.1 Overview of new generation waveform generator N_Bertha (or mAWG), the latest shuttling hardware.

Before moving ahead on the discussion, dealing with underlying intrinsic details of the segment controller, it would be better to have a brief description of hierarchical model of experimental control system from the N_Bertha perspective, which would help to understand the overall picture of it. The discussion ap-

proach is from top to the bottom, which is how current designs of N_Bertha has been implemented. Therefore, in Sec. C discussion and significance of N_Bertha as complex experimental control system has been presented. In the next section (see Sec. C.1), a brief discussion on basic principle of programmable technology, its availability in the market, reason for choosing this hardware-platform and motivation for using current firmware have been discussed. After that (Sec. C.2), workflow of the segment controller (N_Bertha), which is the structural pillar of N_Bertha has been discussed.Interplay of multiple units are also included in the discussion.

After that, for the sake of simplicity, we have divided the complete design into two main sections, Development of Digital Electronics (Sec. C.3). As the name suggests it discusses the detail of digital electronics of this design, more precisely, the central program running on the programmable device and Development of Analog Electronics (see Sec. C.4) presents a complete discussion on the analog electronics designed during this thesis. Moreover, these sections have multiple branched subsections which are needed to explain their respective divisions.

This chapter might appear more interesting for the physicists with electrical engineering background. It contains several technical and new terminology, which might be new to the reader. However, understanding this technology will help them to explore the new dimension in experimental physics as this is how we lay down foundations and build the experimental infrastructure which is used to investigate the ions and to do more exciting physics.

Hierarchy of the experimental control system

The diagram in Fig. C.2 shows a hierarchical model of the experimental control system from N_Bertha perspective. The lowest member in this model is the control computer, where the experiments are encoded in a higher level programming language (currently used CPP/C). Then coded and encrypted experimental information moves through a multiple level of compilation and generates a structure of binary data. This data is generally called as sequence which represents the experiment in binary format. After that, we need an instrument which can read this encrypted information and perform experimental as embedded in data. This decoding and experimenting is performed by N_Bertha.

The sequence information is transferred via Ethernet to next-level i.e. SoC-FPGA based Digital architecture. SoC-FPGA is the programmable device that has been discussed in Sec. C.3. For the sake of simplicity, it can be assumed as an advanced microprocessor, that is prepro-

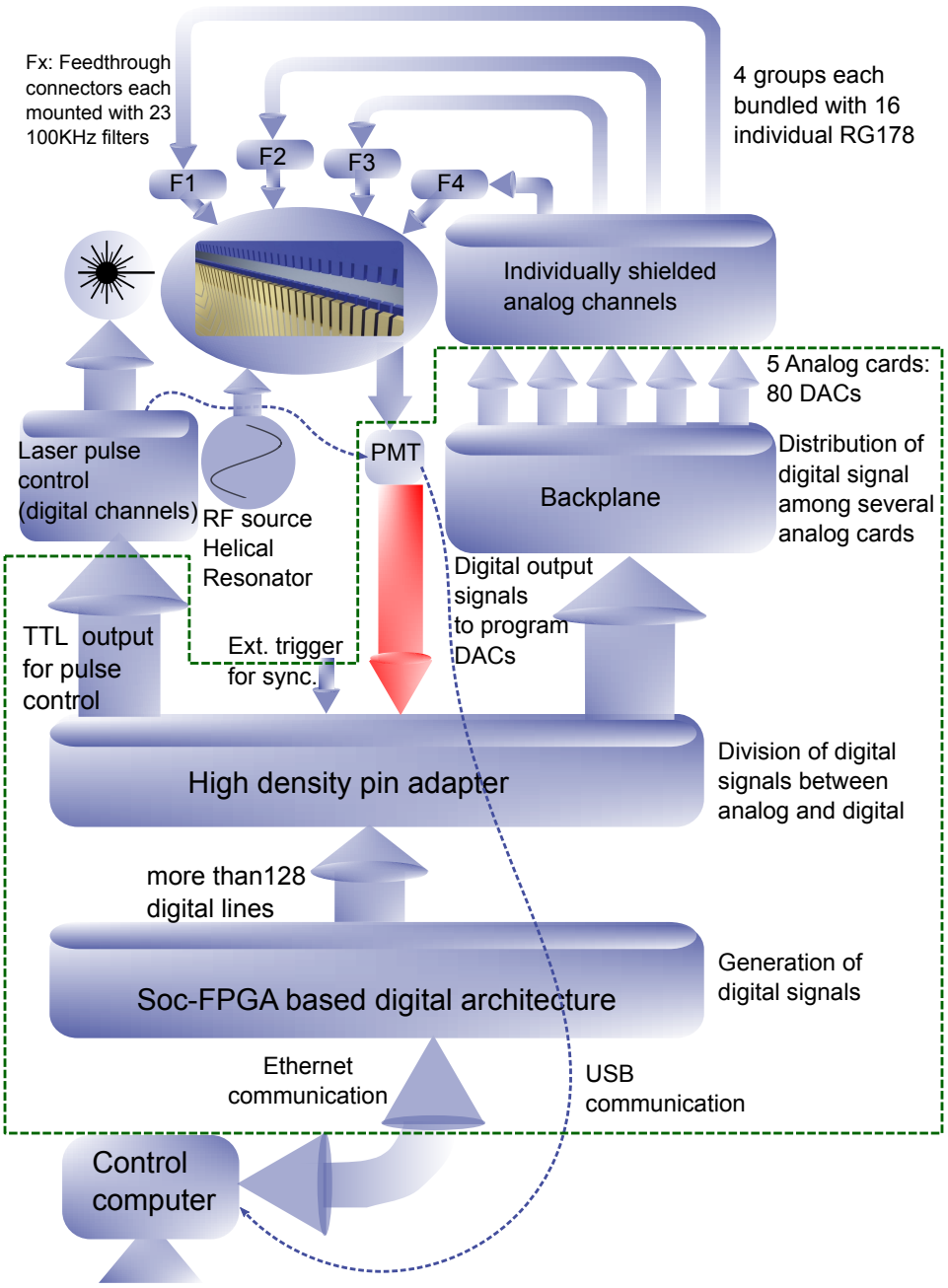


Fig. C.2 Detailed block level view of N_Bertha. The enclosed area by the dashed line (green) shows content of N_Bertha. The red line stands for missing functionality which is to be implemented. PMT with red-line indicates that PMT module will be counting incoming digital information from a PMT through FMC-adapter (High-density pin adapter), which is built inside SoC-FPGA. SoC-FPGA based digital architecture is the core for the digital control of time-critical and accurate control of experimental functioning. This is the handler for handling input and output of experiments. F1..Fn are the four sub-D 25 connector at feedthrough which is connected to trap electrodes. More details are discussed in text.

grammed to control the lab-equipment with nanosecond precision (∼10–20 ns). The encoded information of the experiments are then decoded by this digital architecture (SoC-FPGA), which then generates fast digital control signals with high precision. Each of these digital lines are responsible for managing different instrument (either optical or electrical) in the lab, including the electrodes of segmented ion-trap. Hence, this level in the hierarchy is responsible for experimenting what we wish to do. Once the encoded information from the control computer is sent to this instrument, it performs the experiments by controlling the essential devices and pass the information back to control-computer after successful completion of the experiments. Any change in the control scheme of the experiment has to be addressed at this level. This is the reason, why a precise and error-free development of this architecture is so important.

The digital lines are differentiated at this level and redirected to high-density pin adapters (see Sec. C.1). This high-density connector accepts the differential and single-ended digital lines from source and redirect it to Backplane. The backplane feeds the requirement of digital signal needed for programming each of the DACs (analog channel) in several analog cards (see Sec. 44). While high-density connector directly buffers digital signals to the digital front plate which is then used for fast switching of high impedance load. Due to special electronics (see Sec. 40) switching of 50 Ω loads is also possible. The voltage generated by the DAC system is then connected to flange via specially designed cable (see Sec. D.16) which is mounted with custom developed concatenated filters with sub-32 connectors (see Sec. D.6) to provide low pass filtering at the input of electrode-voltage of the ion-trap. The red-arrow (see Fig. C.2) is the data acquisition from PMT module that provides a statistical count of photons emitted by ions at the end of experiment which is then evaluated to identify the state of ions [Rus18]. This is a missing link and has not been implemented till date, although under the joint collaborative effort of Uni-Mainz and Gigatronics Inc., work is in progress to establish this missing link as soon as possible. Establishment of this missing link will mean that the digital architecture will be able to do more complex algorithm with minimum consultation to the control-computer. And, except for the generation of experimental sequence code by user, everything including controlling of electrical-instruments, electrodes of QCCD and recognition of ion-states will be done at the digital architecture level. This will decrease negotiation overhead between the control computer and FPGA digital architecture. Currently, the data acquisition is done by USB link (dashed line in see Fig. C.2) through the PIC micro-controller[1]. There is also a provision of synchronizing the experiments with external source within the resolution limit of 20 ns. This synchronization trigger directly interacts at the digital architecture level and synchronizes the

[1] PIC32mx250f128b

generation of digital control lines which in-turn sync the experiments.

Many pioneer ion-trapping research groups labs use National Instruments data acquisition (DAQ) cards to achieve the similar control of the experiments. But using a NI-DAQ analog source might not serve our purpose due to several high-end requirements for our experiments. In our case, quantum gate operations are followed by shuttling of ion(s) simultaneously. Therefore, an exact and fixed phase relationship between the control of analog voltages for positioning control of ion(s) and laser pulse used for quantum logic gate is needed. Besides the low noise, the precise voltage control and phase relationship are the critical requirements which cannot be compromised in our experiments. So far till date, I am unaware, if such device is available in the market, which can support as many as eighty analog channels and twenty-four digital channels for shaping laser duration with explicit low noise level (see Sec. 12) in the voltage supply, and if needed, can be scaled (see Sec. D.3) to support larger ion-traps or QCCD .

C.1 Selection of programmable device

The programmable device is a compact integrated circuit which can be custom programmed multiple times by the user. FPGA is a similar programmable technology that is designed using several arrays of programmable gates, where these programmable gates contain Lookup Table, D-flip-flops, and multiplexers. So, it is called as Field Programmable Gate Array (FPGA), where "Field" stands for its hardware programmability by the user, unlike microprocessor.

The basic usage principle of the SoC-FPGA based FPGA is similar to micro-controller. Both SoC and µC have an embedded processor, RAM, ROM, interrupt modules and other peripherals. But the main difference between an FPGA based architecture and µC or µP is the idea of field programming in their hardware. It means, in the second case, i.e., µC orµP cannot be rewired (reconfiguration) according to the user's need, while reprogramming is possible in the first case. In FPGA designs, one can design new hardware peripheral and can also execute custom software, if it contains an embedded processor. In other words, µC can be called as a minicomputer, where reconfiguration of preset hardwired peripherals is not feasible, however, execution of processor compatible software is possible.

An important question is to, why use FPGA , instead why not using µC with embedded µP, to generate pulse sequences and to program the DAC is also possible with such µP. A very straight answer to this question is that FPGA provides more flexibility in terms of improving and adding functionality to main core to run the experiments as required. Moreover, our

experimental control system needs precise digital resources as they will be one point contact to interact with shuttling based quantum processor and do data evaluation, so either μC or embedded μP based μC is not enough in terms of resources to support digital architecture (see Fig. C.2), as it is the fundamental basis of experimental control system. μP is fast, but they cannot be reprogrammed to design newer peripherals. Therefore, they are not flexible and hence would not fit well in requirement criteria.

Rise in the latest electronic technology in the last decade offers an extensive range of programmable resources in market. At the time of writing this thesis, 7 series FPGA (e.g., Virtex-7, Kintex-7, Ultrascale devices) and also Zynq based SoC-FPGA (e.g., Zc702 (see Fig. C.3b, Zc706 (see Fig. C.3c) and others) are dominating the programmable device market. I would suggest the reader for warming up their information on FPGA from different available online resources, as it will help in understanding various aspects of the design discussed in this thesis.

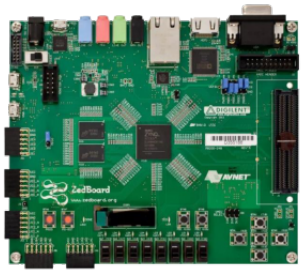
SoC-FPGA are FPGA in association with inbuilt fast embedded processor along with hardwired peripherals (that includes an Ethernet controller, memory interface controller, UART Controller, and many others) and FPGA can be used to design new peripheral and the embedded processor can be used to control input and output of the customized peripheral. For example, let's say that we need a precise counter with 2 ns resolution, that shall start/stop counting after interrupt by the user, in this case, the user will negotiate with embedded processor, that will initialize FPGA logic to start counting with ns resolution. An interrupt from the embedded processor or the completion of assigned task through FPGA logic shall be pause/stop it. An embedded processor cannot do such precise counting by using higher level programming language. This is how FPGA wins over μP concerning flexibility and μC regarding resources. There were several engineering aspects which have been taken into consideration before concluding the firmware advancement platform, like, available on-board device-resources (like memory resources, input-output channels), the dimension of board, availability of the supplementary parts (like connectors), software support, the number of targeted electrodes in segmented ion-trap. However, the most influential factor was "the number of ion-trap electrodes intended to be addressed simultaneously. But then unavailability of support for old FPGA resources (Virtex-5) for old DC segment controller [Wal+12; Rus+14; Kau+14; Kau+17] has added a requirement of making a design, which can address future problem also, i.e with an essence of forward compatibility. Hence, new design using Xilinx Soc Zynq-702 (Zc-702) evaluation board (see Fig. C.3b) as the heart of system has been developed for addressing maximum number of electrodes in ion-trap with its unique design technology that supports

futuristic compatibility also. Therefore, an essential feature of this design which separates it from its counterpart [Bai+13] [PK15] is its adaptive nature, in modern ever-growing field programming technology. The CIP developed for this segment controller uses AMBA® AXI4 protocol, which is the latest data bus protocol from the ARM (ARM Holding) and also the leading data bus protocol in the developed or newly developing the latest field-programmable technology from Xilinx. ARM holding is a British firm, which known for their the most successful designs of the embedded processing world (ARM processor) and their protocol (AMBA). Also no device/board specific dependency of (Zc-702) has been incorporated in it. So the CIP (intellectual property) developed for this, can be easily used in any new programmable platform for the embedded design which uses same bus protocol and relatively more or comparable device resources than SoC-FPGA Zc-702. Zc-702 evaluation board uses chip (ZC7Z020CLG-1) which is used in Zedboard also, the Zedboard are starting variant in Zynq series. The current design has also been tested with less advanced Zedboard and more advanced SoC-FPGA Zynq 706 (XC7Z045ffg900-2) which is next elder sibling of Zc-702 in Zynq series.

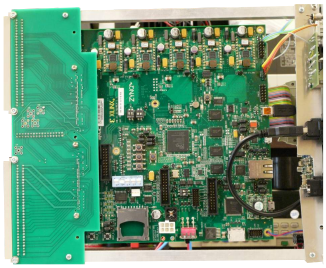
Zedboard, Zc-702 and Zc-706

Zedboard, Zc-702 and Zc-706 evaluation boards are the first three boards of SoC-FPGA variants from Xilinx, in growing order of the complexity. Zedboard and Zc-702 have the most basic SoC-FPGA chip of this series, but they differ in availability and access to different peripherals in the board. The peripheral which are in our design perspective is access to I/O ports of Zc-702. Zedboard provides access to the only limited feature of the Zc-702 chips. The resources of Zedboard and Zc-702 are same (except I/O); therefore any developed design which is synthesizable/implementable on Zedboard will be equally good for Zc-702. However, other way around implementation will not be a possible due to mismatch in available I/O resources. Therefore, when the initial course of development was accomplished on the Zedboard, and after the preliminary test were successful on Zedboard, resource-design were transferred to Zc-702 boards. Subsequently, it was tested on Zc-706 boards as well. A brief introductory comparison of these three variants in context of current design has been presented in Tab. C.1.

(a) Zedboard



(b) ZC702-evaluation-board



(c) ZC706-evaluation-board

Fig. C.3 Image of first three variants of the evaluation board from Zynq series of Xilinx Inc. The three boards are relevant to our N_Bertha as the design discussed in this thesis has been tested on all of these boards. The image Fig. C.3a and Fig. C.3c has been taken from available resources at the Internet (for introduction' sake only), while Fig. C.3b is an image that is currently in use. (a) Zedboard and (b) Zc-702-evaluation-board share same SoC chip but (b) is rich in available board resources, while (c) is more powerful than (a) and (b) concerning both on-chip and onboard resources.

Table C.1 Comparison of device resources in different variants of Zynq series

Features	Zedboard	ZC702	ZC706
BRAM	140	140	545
Flip-flops	106400	106400	437200
IO buffers	200	200	362
LUT	53200	53200	218600
RAM(MB)	512	1024	1024

There are two types of random access memory inside the FPGA which can be configured during design development. They are Distributed and BRAM . Both of these can be configured and used as local storage for immediate buffering of the data for e.g, during the image processing, and when the buffer memory resources are needed for direct access to data. BRAM can be understood as a block of programmable memory, which is available across FPGA chip while distributed RAM (LUT) is part of programmable gates of gate array (FPGA). Buffer memory storage (like FIFO) can be designed using either BRAM or Distributed RAM. They are necessary resources and hence shall be utilized correctly, as they may provide access to data without any delay. The number of BRAM in Zc-706 is much higher than Zc-702, which means a large amount of data can be buffered, and hence for memory related complex design Zc-706 will be a preferred choice.

Flip-flops are the basis of logical programming. Therefore, before using logic for either doing mathematics (like an addition/subtraction/comparison/multiplication) inside FPGA , the usage of it shall be tracked and optimizing the usage of embedded memory resources. For multiplication, DSP shall be used in association with flip-flops, otherwise larger resource from distributed RAM/BRAM will be synthesized by the Xilinx tool for usage. DDR3 RAM and access to I/Os buffers are board features, which means external memory resources and I/O connector are connected to memory controller pins and I/O buffers respectively. The DDR3 memory details are as: Zedboard (2 each 256 Mb $\times$8 SDRAM= 512 MB), Zc-702 (4 each 256 Mb $\times$8 SDRAM=1 GB) and Zc-702 (4 each 256 Mb $\times$8 SDRAM=1 GB), which means that multiple memory block-units of 256 MB[2] are mounted on the boards. These memories are accessible in our design at addresses from 0x0000_0000_h to 0x3FFF_FFFF_h.

I/Os of Zedboard and Zc-702 are accessible using FPGA Mezzanine Card (FMC) connectors. FMC connectors are I/O pin connector which are available only in advanced modern FPGA (Zynq series and other 7-series boards) boards. FMC connectors are available in two variants low pin counts (LPC) and high pin counts (HPC) . Zedboard and Zc-702 contains one and two LPC connector(s) respectively, while Zc-706 contains two HPC connectors.

The adapter devised for translating the board I/O signal to the back-plane is compatible with HPC (High Pin Count) type as well. LPC is used in lower variants while HPC is used in higher variants of these (Zc-706, Virtex-7 series, Kintex-7 series) to facilitate more I/O pins as the device resources. The custom adapter board administers the SoC-FPGA digital signals to 2$\times$32 male pins[3] for analog and to 32 pins dual row standard connector for digital sections of the boards.

The presence of two LPC connectors on Zc-702 evaluation boards has reduced the effort of redesigning a new adapter board for this SoC-FPGA chip. Currently, several latest available boards in the market are using this connector, so high density pin-adapter (Sec. 4.2.2) has been designed to translate digital signals generating from Zc-702 boards to analog and digital modules (see Sec. 4.2.3 and Sec. 4.2.2 or (see Sec. 44 and Sec. 40). The high density pin-adapter is compatible for both LPC and HPC connectors. This feature is added to with the idea of forwarding compatibility in long run.

[2] **Micron MT41J256M8HX-15E**.
[3] **DIN 41612**.

The explanation of several terminologies presented above is based on my understanding of different elements associated with either FPGA or SoC-FPGA . The expert might have a different opinion or way of explanations. However, detail presented for multiple boards are relevant concerning the design discussed in the thesis and shall not be considered as main reference. The documents are available at the website of Xilinx and hence shall be considered as main references.

C.2 Design overview of N_Bertha

The block diagram (see Fig. C.4) shows the physical placements of different modules (analog cards, SoC-FPGA , digital channels, power supplies) inside 19" compatible box-cabinet. Digital signals generated by SoC-FPGA is passed to backplane via FMC connectors (Sec. C.1). Analog cards (see Sec. 44) has two group of analog channels, which is distinguished as North or South group. Each group of analog channels contains eight single channels DACs and its associated parts. LPC -1 (FMC1) is medium to control the northern channels while LPC -2 (FMC2) is used for south section. Standard dual pin insulation displacement connector (IDC) (1.54 mm) of 34-pins is used for the digital section (discussed in 40). This also shows that the relative placement of the different power modules used within the design. The power units (see Sec. 32, Sec. 39, Sec. 33) that powers analog cards are situated at the left extreme as shows in the design, while support for the digital sections which includes power supply for SoC-FPGA also are provided from the right side (see Sec. 39). This way we tried to establish complete isolation of the digital and analog section to avoid any noise interference coupling to analog section from the digital side. This is done to maintain the integrity and isolation of analog channels.

The diagram shown in Fig. C.5 shows the simplified picture of the data flow for execution of our sequences in the experiment. The experiment sequences that are executable in N_Bertha are converted into binary format by C++ program written by Thomas Ruster and me. This C++ program is used under wrapper of custom home-grown software, MCP developed by Kilian Singer. Although, I have discussed the format of data structure needed for this device in sectionC.3, the complete C++ outfit can be found in Thomas thesis [Rus12]. This binary sequence is transferred to the server running on ARM processor of ZC702, via raw Ethernet TCP/IP protocol. ARM receives the binary data and performs initial data validation. This connection validation is the first check to validate if established connection belongs to the experimental control computer, as it is the only computer which is authorized to send data to the server hosted by the arm processor of the SoC-FPGA . If it fails to resolve or recognize the host computer, it will refuse to execute the requested sequence. So the host connection must be pre-configured in accordance to match the specification of this device (Sec. C.3).

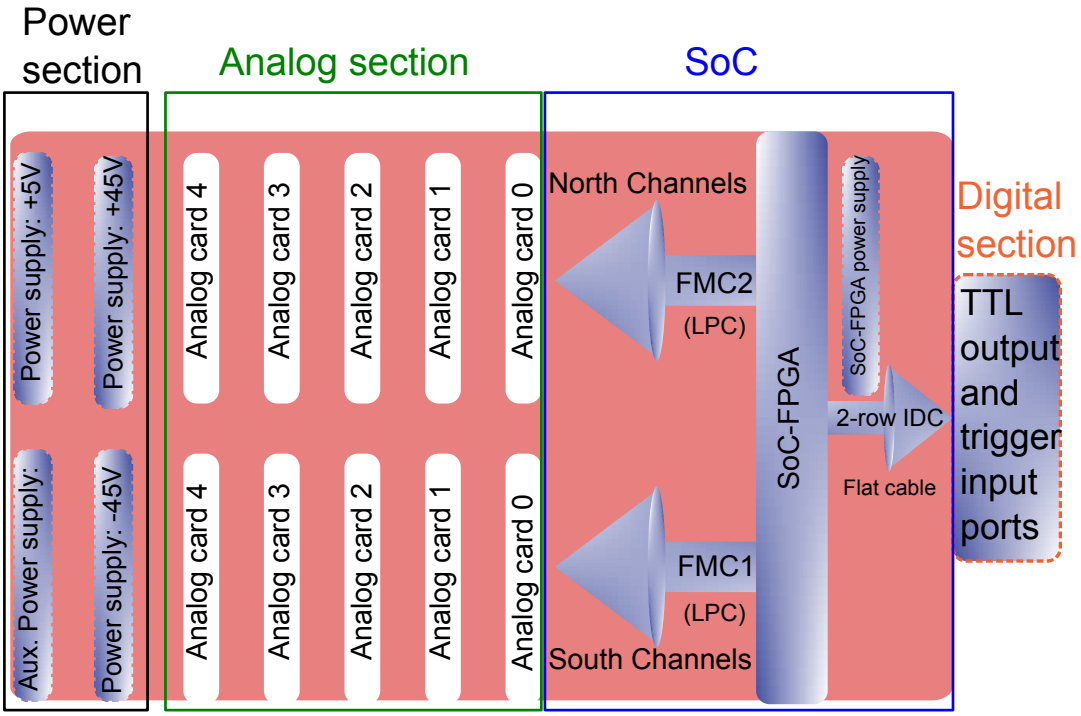


Fig. C.4 Physical placement of SoC-FPGA , analog-cards units, power-supply units, laser pulse-shaping units inside the N_Bertha housing. There four power supply units (extreme left), five analog-card units (center), one pulse-shaping unit (right). Right units are completely isolated (no GND connection) from left side units. Power-supply for SoC-FPGA units (SoC-FPGA power supply) is used to power the right units (digital section), all the analog power supplies powers central unit (analog cards) only.

After connection validation, it checks for data format integrity, before writing it into DDR3 memory. Data format as mentioned in C.3 must be maintained for successful execution of the sequences. After initial data validation, the custom designed program (in C) running on the arm processor separate all the necessary information and write it into the different initialization register and DDR3 memory. The info (see Sec. C.3) are recorded on the digital-register while sequence is written into DDR3 memory. ARM processor then informs CIP that it has finished the necessary pre-processing of the data and execution of the sequence may be started. CIP checks the status report through its status register and takes over the initialization command from the processor and pass it to the Master modules (M0 and M1) and synq these modules. These master modules are equipped with intelligent state machines which starts independent processes wherever is necessary and also they can negotiate for synchronization whenever needed. All the state machines (info on M00 and M01 also) have been explained in Sec. C.3. In the currently installed system in the lab, simple sync module is in use for the synchronization, however it not of much importance for the single unit of N_Bertha . Sync module is mainly

implemented to support multi-unit configurations, that means synchronous control of electrodes of the ion-traps, that needs support for more than 80 segments (see Sec. D.3). After successfully executing the received sequence, both the modules (M0 and M1) pass this information to the sync module, which in turn uses a high priority interrupt line to pass this information to the arm processor. After that, the ARM processor builds up an Ethernet packet and immediately transfer this information back to the control computer.

The modules (M00 and M01) is in synchronous with each other, they are together work for streaming 128-bits data, with an individual contribution of 64-bits digital lines at the resolution of 20 ns. Therefore, N_Bertha appears as 128-bits device from outside. There are multiple clocks used in it for synchronization (see Sec. C.3). However, output clock is 50 MHz that is used for programming the analog cards and also resolution limit of pulse-shaper. Nevertheless, internally both the modules (M00 and M01) are in sync with 5 ns resolution. A total of 100-pins are dedicated for the analog channels while 12-pins from both module data-bus are reserved for the laser pulse sequencing. 4-bits have been kept optional to keep the hardware architecture ready for the future course of the development as we will discuss in the chapter: 5 (Outlook). Hardware descriptive language for designing this digital logic is VHDL (VHSIC Hardware Description Language). Beside digital logic development, it has also been used for configuration of ARM-bus (AMBA AXI bus protocol).

We have divided the development process broadly into two sections.

- Development of Digital Electronics: It contains the description of process-based sequential and concurrent digital logic including state machines, that is currently running on SoC-FPGA . It based design methodology relevant for our experimental control has been discussed in detail.
- Development of Analog Electronics: This section mainly discusses the development of multi-channels analog cards, power-supply units and digital TTL buffers for laser pulse-shaping.

C.3 Development of digital electronics

This section contains a discussion of SoC-FPGA based digital architecture (see Fig. C.2). It is subdivided into three different parts for the sake of presenting whole design in structured way. The Sec. C.3 discusses embedded firmware development at the block level, which means an illustration of how block level has been put together to facilitate the necessary data transfer

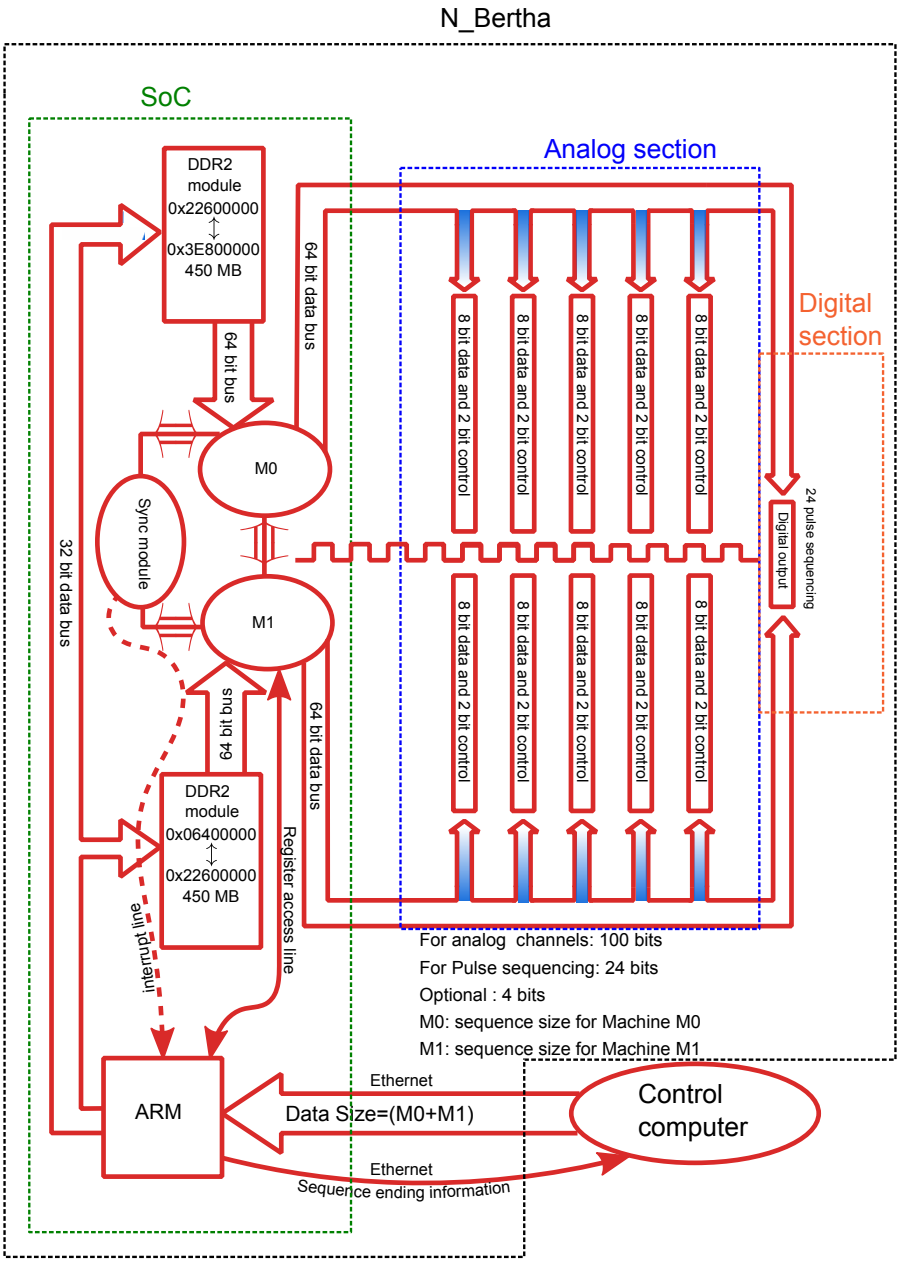


Fig. C.5 Illustration of 128-bits data flows inside N_Bertha framework (black dashed-block) from SoC to Analog modules. In control computer digital data is encapsulated in two-block (for M0 and M1, each 64-bits), and sent through Ethernet TCP/IP. The ARM processor of SoC-FPGA handles this data, and write it into two different locations of DDR3-modules. Then, a sync module (SoC-module, green dashed-block) synchronize two DMA transaction to buffer synchronously to Analog (blue dashed-block) and Digital module (orange dashed-block). And finally, end of successful buffering is reported back to control computer. More information is provided in text.

as illustrated in Fig. C.5. It is achieved by establishing a Master-Slave relation between the different available interface of the digital block level entity. It is followed by the introduction of CIP (see Sec. C.3). It explains in detail different state machine (SM) that are acting together at the most basic level to support the sequence execution. Lastly, there is a brief discussion on the data transfer methods (see Sec. C.3), there I have tried to explain the methods of data transfer tried during developmental phase. The significance of used method and the performance report has also been discussed.

SoC based embedded design

N_Bertha utilizes the resources from programming logic (PL) as well as processing system (PS) . The ARM processor is PS unit while FPGA is a PL unit of the SoC-FPGA . PS unit can take care of the interrupt, Ethernet handling, managing general purpose, and the control register of all controllable IP of design. While PL unit is the central configurable unit of the device that can be used to implement the decision-based algorithm with digital logic, we will discuss the configurable PL and other core of PL used in the design to achieve desired data flow as shown in Fig. C.5.

There are two aspects of general embedded design, first is the implementation of an accurate clock and reset signal as they are responsible for successful initialization of the digital logic, which is represented as a block (Fig. C.6 or Fig. C.7), then comes successful transfer of data from one block to its neighborhood. Data transfer generally happens with the collective effort of several signals. Hence, it has to be a interface in nature while reset and clock are significant nevertheless they are continuous and bear a time critical relation before the start of any process. Therefore, clock and signal, although mutually related for design perspective, but are independent individual signals. Once all the process has successfully started, we can stop worrying about the clock and reset signals. Hence, any discrepancy in their behavior will seize whole design, irrespective of design perfection. This is the reason why a hardware board developer makes sure the fundamental properties of the clock and reset signals are largely preserved.

Other structured layers associated with design includes software management, associated structured clock and reset design, a full understanding of the data flow, generation of one or more custom IP (s), scaling and assembling all the IP (s) in the IP -integrator and lastly but not the least a well regulated and thorough testing protocols. Differentiating the development stage used during this project precisely is difficult. So, I would instead try to build a course overview of the main structure for the future development of this project. Before proceeding

ahead, I would like to emphasize this point that for some user development of this project may be very straightforward, but the most challenging part of this project is to get the design fully functioning in the lab conditions.

Software management for hardware development

Software management is one of the most crucial aspects of this design development as even with revision control system access of the old working project might not be possible. Therefore, it is always recommended maintaining a separate copy of the basic structure of the project. Also, the software has to be robust enough to handle design demand during embedded project development. As any small mismanagement in design understanding or software knowledge will be like an infinite loop around the error. And it will be difficult to figure out the exact source of the error. There may be large number of such errors. I have discussed a few of them in the upcoming section. Several unsuccessful efforts have been tried with the older version of embedded design software, which is still used by many of the developers. In the older versions, it was challenging managing continuity of ongoing development of whole design.Before Vivado evolved as a complete solution for hardware designing and software developments, PlanAhead, ISE Navigator, EDK (Embedded development tools) were some of the embedded processor development tools which were extensively used during the project development.

Fig. C.6 and C.7 have been designed in Vivado 2016.4 IP - Integrator. Our old FPGA firmware which contains Virtex-5 has been developed in EDK only. By that time EDK use to contain software development kit (SDK) also. But shortly after that, Xilinx Inc. deprecated this architecture of the supporting SDK inside EDK. Even today, if someone wants to modify the current working software of old firmware which is still in use, will have to use EDK-2012 version.

Vivado is the latest embedded firmware development platform from Xilinx Inc. Evolution of Vivado and its IP Integrator has reduced the effort of software management substantially. Otherwise, development of embedded processor-based design was challenging. I consider Vivado as a more advance well-managed version of integration idea of EDK tool, ISE and plan tool. The current project has seen phases of EDK, ISE, and Planahead before reaching finally to the current format in Vivado. Also managing the project using any revision control (like GIT) is not recommended, it is advised to keep a separate copy of working project as it is. However, entire project can be placed under revision control but do-not rely on complete restoration of a working project if lost for some reason.

Constructing the Embedded design

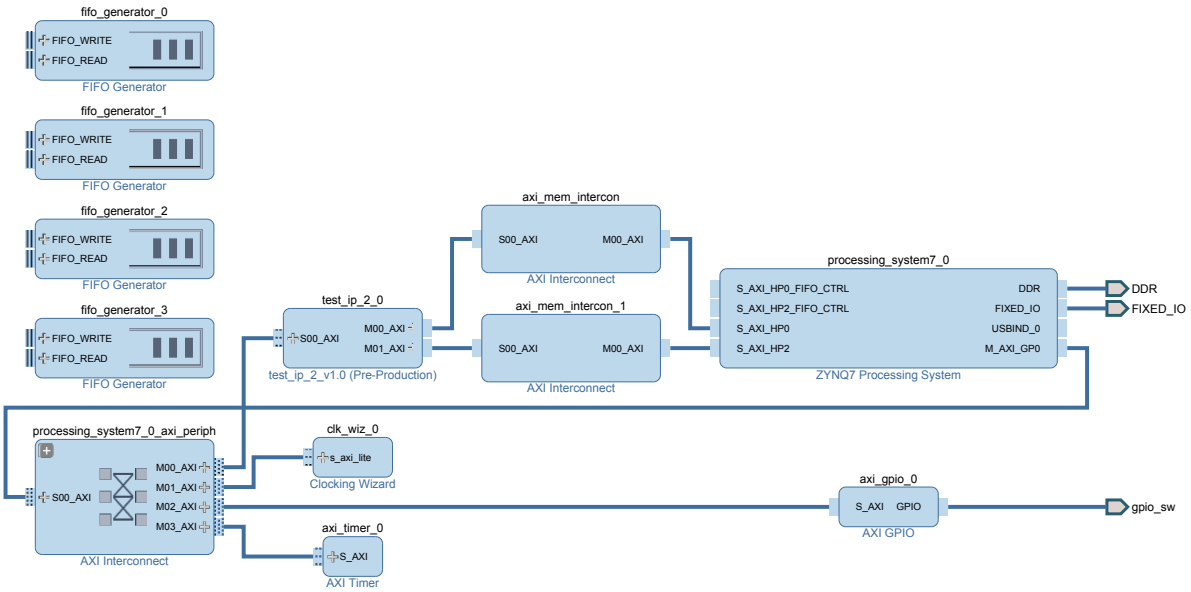


Fig. C.6 Master-Slave type embedded architecture based on AMBA® AXI4 protocol in Zynq, (interface designed in Vivado 2016.3). It shows flow direction of data and commands between master and slave. The interface which is on the right side and starts with 'M' are Master module and those specified on the left side and starts with 'S' are the slave interfaces. Master has to be connected to the slave which it desires to control.

Zynq®-7000 AP SoC of ZC-702 evaluation board contains rich dual core ARM® Cortex™-A9 MPCore™ based processing system (PS) and Xilinx programmable logic (PL). Beside ARM embedded processor, there is a total 19 IP core used in this design. Some IP core used can also be replaced by simple gate logic. Nevertheless, it is being used outside of IP core to maintain overall integrity, and the logical structure of the custom is simple. Table:C.2 contains the list of IPs currently used in the design.

The diagram shown in Fig. C.6 has been designed in the IP Integrator of Vivado release (later than or Vivado 2016.3 release is recommended for any upgrade). Custom IP (test_ip_2_0) of the Tab. C.2 shall be added to the repository of default IP directory in the working Vivado. Then, a tool command language format **(.tcl)** file (**project_1_Mains.tcl**) can be invoked to build up the project. Due to infinitely large content in the .tcl file, it is part of the digital submission along with this thesis. This .tcl file can be executed in the Vivado-Tcl console to re-produce an exact copy of main design.

Table C.2 List of the IPs used in embedded design on N_Bertha

S.N.	IP name	IP version	Number of units
1.	**processing_system7_0**	ZYNQ7 Processing System:5.5	1
2.	**test_ip_2_0**	test_ip_2_v1.0:1.0	1
3.	**clk_wiz_0**	clk_wiz:5.3	1
4.	**axi_timer_0**	axi_timer:2.0	1
5.	**axi_gpio_0**	axi_gpio:2.0	1
6.	**xlconcat_0**	xlconcat:2.1	1
7.	**fifo_generator_0** **fifo_generator_1** **fifo_generator_2** **fifo_generator_3**	FIFO generator:13.1	4
8.	**axi_mem_intercon** **axi_mem_intercon_1** **processing_system7_0_axi_periph**	axi_interconnect:2.1	3
9.	**util_vector_logic_0** **util_vector_logic_1** **util_vector_logic_2**	util_vector_logic:2.0	3
10.	**rst_processing_system7_0_50M** **rst_processing_system7_0_50M1** **rst_processing_system7_0_50M2**	proc_sys_reset 5.0	3

The IPs listed in the Tab. C.2 are added by using the add-button on the IP - Integrator panel in the software. We can execute a simple c-program on the embedded arm processor, which allow us to read and write data to/from any of the IP interfaces connected to the processor as a slave. Fig. C.6 shows Master-Slave type design, in which some IPs, including (ARM Processor, Custom IP) are acting as the commanding Master and also being slave on the interconnecting bus, while the rest of IP (s) are only Slaves, to either processor or CIP. One of the Master GPIO ports of ARM processor (ZYNQ processing system) is acting as Master on the AXI Interconnects in-turn controls like a Master on the Clocking Wizards, software controlled GPIO ports, timers, and CIP. So CIP is acting as a slave for the ARM Processor. CIP is connected as Master to HPC of the ARM processor memory interface controller. So, ARM controller is situated on the bus as slave to the custom designed IP , CIP. This design interface fulfills the necessary data flow of our experiments as shown in Fig. C.5. Master IPs can read information from Slaves IP and also can perform write operation on the respective register of the Slave IPs. This is how ARM processing unit writes down the data to the DDR3 and hence inform CIP about the completion of its respective processes. When CIP is performing the data transaction as master from the DDR3 memory, none of the IPs core including even processing unit (ARM PS) can interrupt. The CIP is designed to get priority on its data bus while performing the data streaming.

Clock Scheme and Resetn Signals

There are three clock system (clock and reset) (see Fig. C.7) used in this design. The PS is generating main clock **FCLK_CLK0**, which is optimally configured to drive connected systems at 100 MHz. While other two clocks (**clk_out1** and **clk_out2**) are generated by the other **IP:Clocking Wizard** (see Fig. C.6). These output clocks from clocking wizards are driving the respectively connected modules at 200 MHz and 50 MHz receptively. It takes the main clock of PS and locks the phase relation to the output clock with main clock (400 MHz).

All read and write operation are done by the PS unit, which is synchronized and controlled by the standard processor clock, **FCLK_CLK0**. PS reset module FCLK_RESET0_N and its clock FCLK_CLK0 are used to drive the Processor reset unit (**rst_processing _system7_0_50M**) Tab. C.2, which subsequently generate synchronous and asynchronous reset bus signal with respect to FCLK_CLK0, altogether these asynchronous/synchronous reset signals and its synchronous clock (**FCLK_CLK0**) are used to perform read/write operation at all the slave IPs (slaves to PS units). These slaves include AXI interconnect (**processing_system7 _0_axi_periph**), AXI Timer (**axi_timer_0**),Clocking Wizard (**clk _wiz_0**) and respective associated clock and reset port of project_1 _1_0 (**project _1_v1.0**). These resets are active high or active low in nature, so depending upon the driving slave IPs and its respective port requirement, they need to be connected. The software tool will start complaining if there is a mismatch between their polarity. Also, most of the reset signals are of the bus type, so if the users are willing to generate their reset system, the generated signals shall be a single bit bus type. The connection details of the main clock, and its reset modules has been shown in the Tab. C.2.

The clocking wizard is like a phase looped lock (PLL) unit, which generates the clocks at configured frequency, whose phase and signals are related to **FCLK_CLK0**. The LogiCORE^{TM} IP Clocking Wizard core [PG015] generates the HDL source code wrapper for fulfilling the requirement of customized clock circuit. The IP can be customized using the IP Wizard, or it can also be implemented using the direct primitive HDL wrapper, Advanced Mixed Mode Clock Manager (MMCME2_ADV) [UG912]. These HDL wrappers can also be directly integrated inside the CIP using standard VHDL/Verilog depending upon used programming language. However, we have decided to use wizard oriented block level design to keep the CIP clean and easy enough to configure. Implementation of more HDL based wrappers inside will complicate the internal structure CIP.

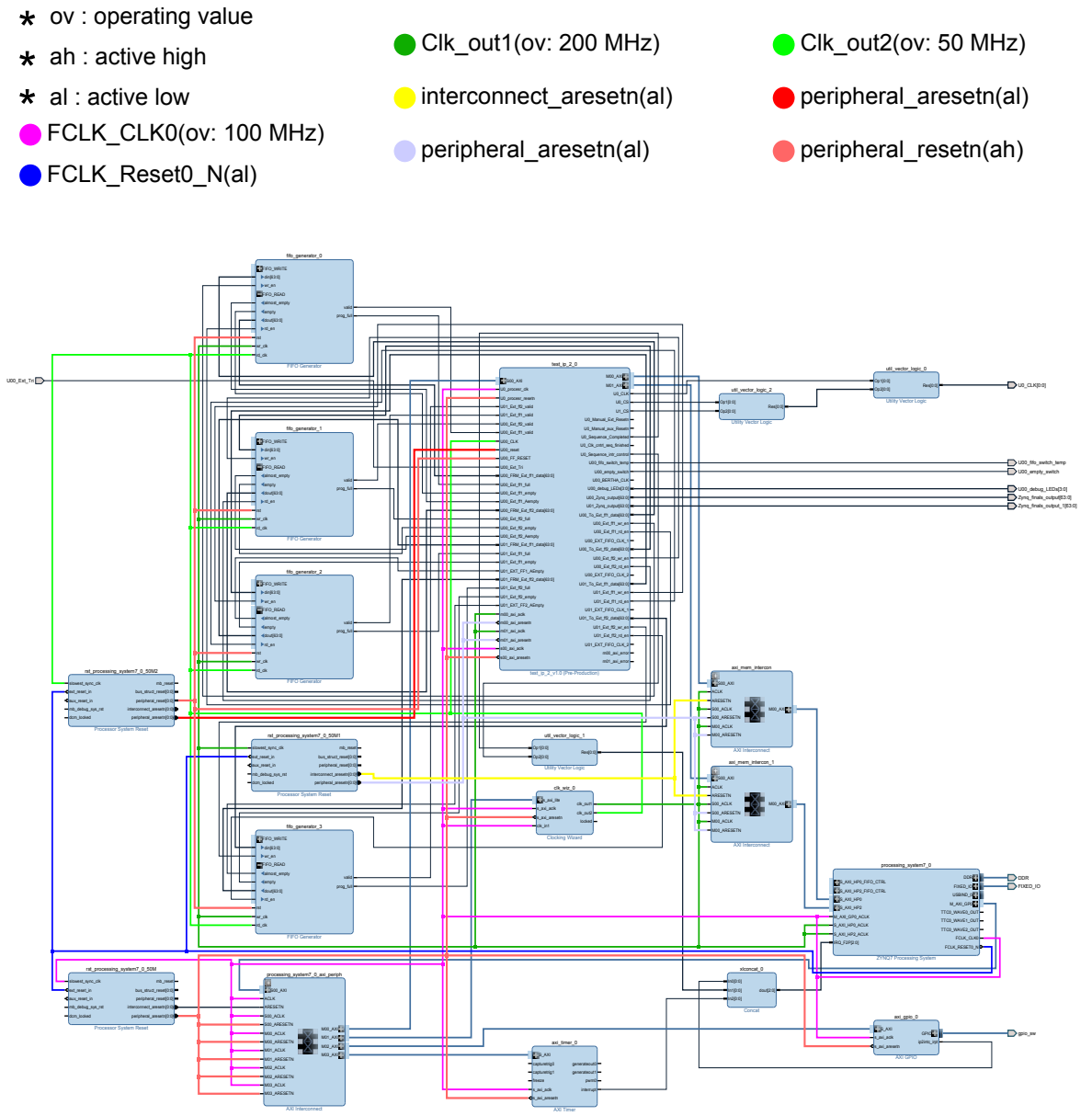


Fig. C.7 Embedded design of N_Bertha based on AMBA® AXI4 for Zynq architecture in Vivado 2016.3. It highlights three variants of clocks (FCLK_CLK0 (100 MHz), Clk_out1 (200 MHz), Clk_out2 (50 MHz)) with operating value (ov) and their respective active high/low (ah/al) reset signals used in this design. These1 clocking and reset signals have been discussed in Sec. C.3.

This IP connects as a slave to the PS, and its control registers can be accessed from PS to control the output frequency of the clock. A master clock of 400 MHz is initialized using the PLL logic and then subsequently 200 MHz, and 50 MHz clocks are derived from this master clock. This master clock and its derived clock has the locked phase relation

Table C.3 Connection configuration of **FCLK_CLK0** and its associated reset signals

Clock Signals			**Port**	**IP name**
FCLCK_FCLK0			s_axi_aclk	**axi_gpio_0**
			s_axi_aclk	**axi_timer_0**
			M_AXI_GP0_ACLK	**PS ***
			slowest_sync_clk	**RST_PS #**
			s_axi_aclk U0_procesr_clk	**test_ip_2_v1.0**
			s_axi_aclk clk_in1	**clk_wiz_0**
			ACLK S00_ACLK M01_ACLK M02_ACLK M03_ACLK	**PS_AP ~**
associated Reset Signal rst_processing_system7_0_50M				
Reset name	Type	State		
interconnect_arestn	async	active low	ARESETN	**PS_AP ~**
peripheral_aresetn	async	active low	S00_ARESETN	
peripheral_aresetn	async	active low	M00_ARESETN	
peripheral_aresetn	async	active low	M01_ARESETN	
peripheral_aresetn	async	active low	M02_ARESETN	
peripheral_aresetn	async	active low	M03_ARESETN	
peripheral_aresetn	async	active low	s_axi_aresetn	**axi_timer_0**
peripheral_aresetn	async	active low	s_axi_aresetn	**clk_wiz_0**
peripheral_aresetn	async	active low	s_axi_aresetn	**axi_gpio_0**
peripheral_aresetn	async	active low	s_axi_aresetn	**test_ip_2_v1.0**
peripheral_aresetn	async	active low	U0_procesr_aresetn	

* **processing_system7_0**
\# **rst_processing_system7_0_50M**
~ **processing_system7_0_axi_periph**

with PS clock of 100 MHz. Each of these clocks has been given a dedicated reset module (**rst_processing_system7_0_50M1** for the 200 MHz and **rst_processing_system7_0_50M2** for 50 MHz) which generates synchronous and asynchronous reset signals for respective clocks. (associated IP and reset signal of 200 MHz and 50 MHz are not shown). The connection details of both clocks are presented in the Tab. C.3.

This lower frequency clock is used to synchronize final streaming output. This structure of design can also be used to stream the final output at a wide range of the clock frequency. Tab. C.4 shows the recommended value of the clock frequency which can be tuned via the control register of the clocking wizards to vary the streaming frequency for driving DAC channels with clock frequency.

For more information on the reset IP modules, it is recommended to look into the product guide of this IP [PG115].

Custom IP (CIP) and used State Machines (SM)

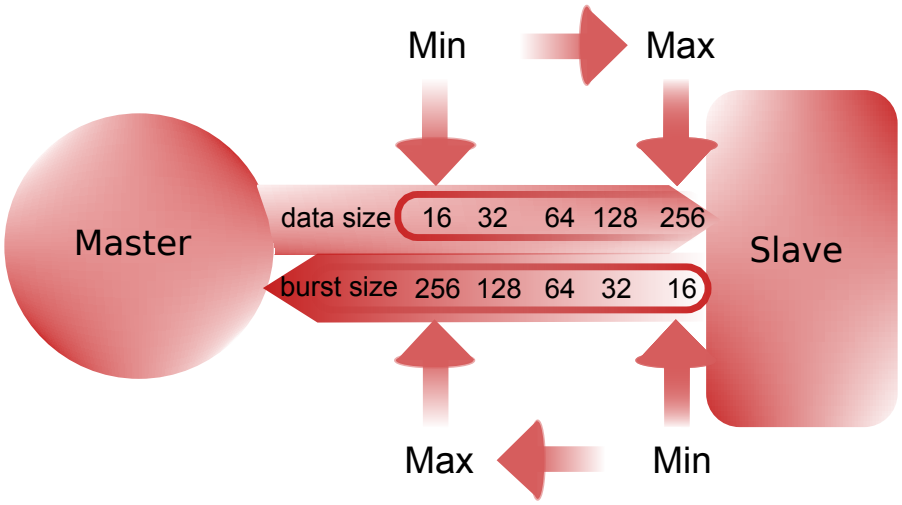


Fig. C.8 Possible burst size and respective data size during the transaction of data from master to slave. This transaction shall not cross max. bandwidth of 4 KB (4096 Kbits). This means if data-width (size) is 16, then largest possible burst size is 256 and so on. In current design we are using burst size of 16 (BS16) (Appendix. F) with data-width of 64 bits for each master slaves full transaction).

Customs IP is the general master-slave based intellectual property developed during the development of this project, that manages the data traffic flow during the continuous data streaming process. There are one slaves and two master interface(s) associated with this IP . Slave IP has lite interface type (S00) with 10 (32-bit) user-accessible registers. Both the master modules (M00 and M01) is full type interface. We use slave lite register to write the relevant information which is used as a reference for both the master interface for determining the amount of data to be processed during the direct memory transfer (DMA) transaction.

We will focus only the interface structure and function of different SM used along with this IP.

There is a total of 11 SM used in the current functional design. These SM are responsible for reading the data from the memory, writing into the FIFOs, streaming it to the output pins, detecting any timing information in the sequence, pausing the running sequence, starting the counter, waiting for the counter to count the request delay in the real time, and re-assuming the data flow, and detecting the error.

The central theme of CIP has been designed to perform two simultaneous DMA transactions to read the data from DDR3 memory and write it into available FIFO and then channelize the output of FIFO in the form of continuous data streaming. The user controls the size of the data by writing it into the registers of using slave interface (S00), which can be infinitely long duration. The long-term here imply to an upper limit of the memory size available on the boards, which is 450 MB for each DMA transaction, that includes 900 MB against the available memory of 1 GB in the currently used evaluation board. Remaining 100 MB of memory resource is reserved for Ethernet buffers, where onboard received data through Ethernet is directed through the ring-buffers (discussed in C.3). This IP can also be used directly with any other memory interface which is supported by AXI bus protocol to read the memory resources of more than 1 GB. The figure shown in Fig. C.8 symbolically shows the possible burst configuration that can be used to read the data from memory. For example, if the data width size is 64 bits, then the only available burst size is 64 or less. 4 Kb is the upper boundary of memory which can be read in one burst transaction for more information on the burst size, and its properties can be referred from the technical documents of the AXI transaction[4]. In our system, we are using the data size of 64-bit and burst size of 16. Nevertheless, burst size (BS) of 64 and 32 works equally well and is also well tested. Higher burst Size (BS) value can be useful if one wants to DAC system with higher clock frequency.

The size of the general generated experiment sequence shall be the factor of the burst size. It is an additional condition imposed by fixed BS (16,32 or 64) size otherwise some redundant information will be read during the completion of the DMA transaction. Due to this addition condition either we copy the previous 64 bit of data of the sequence and add to it on the software side at the host computer (or on FPGA side), or we design an interrupt to disengage the ongoing burst transaction so that only valid data is read from memory. Experimental sequence needs not necessarily have to comply and be the multiple of 16 as the requirement by burst size. So,

[4] ARM11.

after receiving the experimental sequence data through the Ethernet, we use the first option and copy the last 64 bit of data (on the FPGA side) into the subsequent memory. Although, the exact data size can also be read by ignoring the data in the last burst or disengaging the burst transaction in the previous ongoing data transaction.

Nevertheless, we have decided to use the first approach, as using the first option makes handling of the streaming control (discussed later in this section) secure and deterministic. While we have also tried including some mechanism to disengage the ongoing burst transaction which does work but fails to synchronize while channelizing the output from the FIFO for few cases. Implementation of a disengaging mechanism will improve that performance for small size data processing. Although our first attempt was to implement this method and a lot of effort has been tried for its optimization, but at the end when it failed to perform for the tested sequences, hence second approach has been adopted.

The DMA transaction is burst type (see Fig. C.8) of memory read and write transaction, which means master and slave modules performs initial handshakes and master gets exclusive access for either reading from the memory or writing to memory of slave modules. Burst size of 16 and 64-bit data-width reads 1024 bit (1 Kb) of data in 105ns, with currently used 200 MHz read the clock from DDR3 memory. Both of the master (M00/M01, see Fig. C.9) get exclusive access to two different memory address through two different high performance (HP) [UG517] interfaces available in Zynq. It takes five clock cycles, i.e., 5×5=25 ns for handshaking and then subsequently continuous stream of data is available at the port for subsequent 16 clocks cycles (16×5=80 ns). Table:C.4 the maximum possible frequency for streaming the output data. This data is stored in FIFOs buffers for further processing.

Custom IP contains four files, top file in the hierarchy comprises instantiating hierarchy and a reset SM which is responsible for issuing a reset signal to all the clocking and reset module in the design. Beside this, slave lite interface register and master interface types (as mentioned earlier in the section) are well organized and initialized in particular HDL description files. There is a total of ten state machines used in the current functional design. These state machines are primarily responsible for following operations: 1. Reading the data from memory, 2. Writing into the FIFOs, 3. Streaming it to the output pins, and also detecting any timing information in the sequence, pausing the running sequence, 4. Starting the counter, 5. waiting for the counter to count the request delay in the real-time, 6. Re-assuming the data flow, 7. detect the error, and 8. Repeating the entire sequence. More information has been discussed in upcoming sections.Since it is designed to be a scalable system, so both the masters

Table C.4 Recommended main clocking frequency and the burst size for different streaming frequency

Desired streaming freq.(MHz)	Master Clock (MHz)	DDR3 read clock	BS
1-150	**400**	**200**	**16**
150-215	600	250	32
215-230	600	250	64

of a full type interface are symmetrical to each other. Each of these masters interface contains five SM handling the 64 bits data-width (the standard data width) altogether making it 128-bits machine.

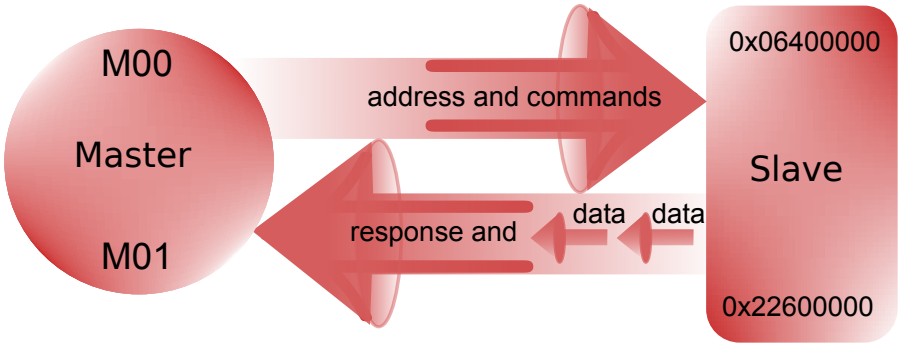


Fig. C.9 Illustration of burst data-transaction using master-slave interface. The Master and slave interact using handshake signals (address and command) followed by actual transfer of data through data-signals of the interface. In current design, M00 and M01 are the two such full master modules built in CIP and the DDR3 memory module is being used as slave to read the data.

The pictorial representation (see Fig. C.10) presents an elaborated picture for the traffic involved in the flow of data from DDR3 memory to the output port. The process management of reading the requested data (requested by the user through ARM) size of the DDR3 memory and assessing the traffic condition of data inflow from DDR3 and outflow into the FIFOs buffer to continue reading or to pause is decided by the SM: Fig. C.11. Fig. C.12 shows the logical SM that is responsible for channelizing the right FIFOs buffer for storing the data. Similarly, Fig. C.13 does the works for utilizing the already written or filled FIFO for available for the reading, while the last state machine which is a mealy type and is responsible for outputting the good time bounded streaming of data at the output port. All the state machine is equally important, and logic used in all of these SMs are mainly optimized to work for an unlimited amount of data with infinitely long multiple delays in between.

Figures C.10 to C.14 shows all the indispensable SMs used in the data processing, although besides this decision-making SM there are multiple processes in the design which helps the SMs to decide for acting and allowing the constant outflow of the data to the output pins. The non-SM type processes are also sequential clock sensitive logic which uses flip-flops to assign value depending upon conditional logic. These processes help in handshaking of master and slave modules before exchange of data for successful data transfer. There is a total of twenty-nine such methods in this design (apart from SM type processes) (refer to a behavioral modeling master interface (M00/M01) of the IP HDL files). These non-SM type processes are also identical for both the master interface modeling. Some of these processes are driven from the standard template of master-slave handshaking modules provided by the Xilinx Vivado tool used to create custom IPs specifically. While, the rest of the operations have been written during the development of this project. It can be broadly divided mainly into two groups: Read and Write section, which means that some of these are helping during the read transaction while others during write transaction. In this design, there is a predominately reading process which reads the data from memory so actively read transaction signals are being updated here.

Nevertheless, the processes which update the signals of write processes are also being updated due to the inherited behavior of hardware modeling in VHDL. I did not remove this logic as these might be useful in due course while implementing write transaction as explained in the final Outlook. All the processes sensitive to the clock are being updated with the clock transition, while the logic inside is like flip-flop which updates at the rising edge of the clock. In this thesis, while explaining any HDL-logic, I am presumably assuming that the reader has prior basic understanding of behavior modeling of hardware using VHDL. The underlying idea of each these processes, followed by an explanation of individual SM has been explained in the subsequent subsection.

Internal slave-master communication

ARM processor or the master modules uses the IP internal register to communicate with the peripheral-modules. The list of the information shared by the master and ARM processor through the slave modules. The slave module of the CIP is situated at offset base-address of $0\times43c1\_0000$ Range of 64KB and High address $0\times43c1\_FFFF$. All the register of the CIP are 32 bits registers.

- Disabling the master's interface write channelize

  - Both the master interface are disabled to process any write transaction at the start of the sequence execution by writing '1' at register offset of 0×0 at bit position:'30'.

- Total number of the bursts transaction masters have been requested to process (sequence data size)

  - PS system calculates the number of burst transaction by dividing the number of lines of 64 bits of data by the BS currently employed in design (16). This information is written at register offset of 0x4 at bit position:'0..31' (32 bit) is reserved for this information. For example, if the data size is 10 MB= $10 \times 1024 \times 1024 \times 8$ bits=83886080 bits=1310720 lines of 64 bit data = 81920(0×14000_h) transaction master interface will be done to read up the entire sequence.
  - Register 0x4 and bit position:'0..31' for master interface (M00), while register offset of 0x24 bit position: '0..31' for master interface (M01) are reserved. This enables the feature of driving sequence of different sequence length on M00 and M01.
  - currently both M00 and M01 are configured through their first register (0×4) to run equal sequence lengths on both the master interface (M00 and M01)

- Number of the line (if the sequence-length is not exactly multiple of BS)

  - if the sequence length is not exactly a factor of the BS then the remaining number of lines (<16) is written to the address offset of 0×8_h at the bit position: 7..0 (8 bits)
  - This feature is not used currently. Although, it is still enabled from the hardware side. This function might be used if the user does not want to copy the last lines to make is exact multiple of 16. This feature works deterministically for the most cases, but still, it may not work in some case as explained earlier in this section. So it is recommended not to use it unless you are running out of space (max. 120 B for copying 15 lines and 8 B for copying one lines).

- Number of repetitions for sequence

  - The sequence has to be repeated for multiple time to determine the photon count during the experiments statistically. This information of sequence repetitions is written at the offset of 0×C_h at the bit position: 31..0 (32-bit register space). Max.

Possible repetitions are 0×FFFFFFFF_h times, which means that even smallest possible sequence of 10µs can keep device busy for (2^{32}-1)×10 µs=12 hours long measurement for a single measurement point!. Currently out PMT detection time is ≈ .5 ms. So this device can do infinitely long measurements in all cases.

- There is provision to repeat the last sequence with new loop number without really transfer the sequence for the second times. This register can be reset to the new value and a new request to initialize the sequence can be launched.
- More information on the Ethernet request protocol for requesting to invoke the last running sequence with updated new loop number without actual data transfer is explained in sectionC.3.

- Start sequence command
  - Sequence starts only at the transition of '0' to '1'. The register offset of 0×10 at the bit position:'0' can be used to launch a sequence. '1' has to be written for this position to start the sequence and them immediately '0' shall be written in the same position to make sure that the master interfaces capture a transition. It can be done the other way around also by simply writing '0' in the beginning and subsequently writing '1' in the next clock. I prefer the first method as it faster to initialize a sequence by writing '1' (single times) rather than doing two write operations.

  - The register offset of 0× ten at the bit position:'0' is inheritable dedicated for M00 interface initialization. While the bit position:'8' is reserved for the initialization of the M01 master interface. Currently, these register possible are internally interconnected to invoke the initialization of both master module (M00/M01) simultaneous.

  - This hardware design has been modeled to drive master modules M00 and M01 independently. But there is a hardware limitation that there is only one clock for both groups of channels North (top 40 channels) and South (bottom 40 analog channels). This hardware limitation sometime may lead to timing failure in one of the channels. So it is not deterministic always, however, implementation of other dedicated clocks for both the channels may lead the device to add on more freedom in the control of the channels (discussed in details in the outlook section).

  - More information on the Ethernet request protocol for requesting to invoke the last running sequence without actual data transfer is explained in sectionC.3.

- Interrupt info for stopping the sequence
  - An interrupt from the host computer can be issued by writing '1' register offset of 0×14 at bit position:'0'. This interrupt can be issued to reset any running sequence, probably resulted due to wrong sequence request.
  - More information on the Ethernet request protocol for requesting interrupt is explained in sectionC.3.

- Tracking the difference between real-time interval requested and executed
  - Sequences have several embedded timing gaps/interval in them. This embedded timing information is recorded in registers at an offset of 0×20_h at bit position:'31..0' for the M00 interface master module. While at an offset of 0×2C_h at bit position:'31..0' is reserved for M01 interface module. In case if there are multiple embedded modules, these registers are updated with the latest timing information that the master module has executed.
  - This information can be used to compare the requested time interval and the time gap between the sequence executed by the master modules
  - Both the master modules can execute embedded timing gap with 20 ns resolution. It is recommended to an embedded gap of more than (or equal to) 60 ns. More information on the time is available in the table.
  - These registers are write protected for the PS system (ARM processor). Although these registers can be assessed by the PS to read their content as intended. These registers are open for write process to only master modules (M00/M01) respectively.

- Sequence ending information
  - Sequence completion is written to the 0×24_h at the bit position:'0'. This register bit position is written to '1' as soon as the sequence execution is successful.
  - This register is also write protected for the PS.

- Final interrupts for successful completion of the true sequence
  - Receipt of every successful sequence is reported and recorded at register offset of 0×28_h. This offset address is updated by writing 0×FFFFFFFF_h on the 32 bits

address by the ARM after successful receipt exact sequence as the promised by Ethernet headers.

- This register is reset to 0x00000000_h by the arm when the PS system receives the Ethernet header. As soon as exact data are received this register is updated to said value.
- On the information of update of register 0×24_h at bit position:'0' and 0×28 at bit position:'0', an interrupt is issued which informs the host computer about the successful completion of a true sequence. Both the position has to have '1' for an interrupt to be issued.

SM and other process inside master module

There are total 29 general processes which co-ordinate with 5 SM to process the data streaming. The diagram shown in Fig. C.10 has tried to show the position of different SM in the traffic of data streaming management. This general and SM based processes are symmetrically present for both the master module (M00/M01). One of these processes is dedicated to synchronizing both the modules. These processes do the assigned task for the input signals of the CIP.

ARM processor extracted sequence-information and writes in the respective control registers according to the set protocol as mentioned in the last section. Then, It invokes the master modules (M00 and M01) to start reading the data from the DDR3 from their preassigned memory location.

M00: SM_A is responsible for reading the data from the memory location of 0×64000000_h while M00: SM_B does the same task of reading the data but from different memory location 0×22600000_h. The difference of their predefined memory address is 450 MB, which is upper limit defined during the customization of the CIP. It is defined to stop the interference between the two master modules. As one master module may try to access the memory location where another module might active for reading the data. Such conflict can happen if either of experimental sequence (for M00/M01) is larger than 450 MB (max. 500 MB). In the next step, this available data has to be written into the FIFO, the stacked memory resources. The FIFO are designed using the BRAM memory resource of the device. BRAM is also a kind of memory resources which are generally used as local storage in the embedded designs. Distributed RAM can also be used for designing FIFOs, however performance of BRAM is better and also designing FIFOs with distributed RAM needs more resources.

In this design, I have used BRAM resources to design FIFO as local storage for continuous streaming. These RAMs acts as stacked memory resources for the data, where the depth and width of it are configurable. So, the depth is multiple of BS in depth and standard width size is 64-bits, i.e., data-bus width. The configuration of BRAM as embedded local storage used in this design is not straightforward. I will try to discuss this idea in detail in the upcoming section as the focus of this section to quantify multiple pillars of the master modules.

M00: SM_B and M01: SM_B are assigned to monitor the status of the FIFO. SM_A cannot for-see the amount of data written into the FIFO. So SM_B of the respective modules track the amount of data written into the FIFO and as soon as one the FIFO is full it switches the empty FIFO which is supported in the design to continue to write process by SM_A without actively wasting any time. This switching of the FIFO for the writing purpose is so accurate that even single bit of data is not lost during this process. The design supports only two such FIFO so it may eventually happen that both of the FIFO is full then in that circumstance it provides a busy signal and asks for interrupting the ongoing read process by SM_A. As soon as SM_A gets this interrupt signal, it pauses the read process and subsequent write process to the FIFO as well. It resumes writing process again once the interrupt is set to low by SM_B. SM_A resumes the read process from the same memory location where it has paused after an interrupt is set to low by SM_B. Hence SM_B controls the data traffic flow of reading data from DDR3. Both M00: SM_B and M01: SM_B are initially designed to fill the first stacked FIFO memory, as soon as a sequence is requested. In case, if the size of the course is larger than the size both FIFO, first interrupt is delivered to SM_A after both the FIFO (for M00/M01) stakes are full.

As soon as first FIFO of both master modules is entirely written, SM_B negotiates with its counterpart of other master module and to get similar acknowledgment. After, successful handshaking SM_B of both the modules issue ready to read signal which is subsequently captured by the another SM module to continue the further processing of the sequence data.

M00: SM_C and M01: SM_C are reading counterpart of M00: SM_B and M01: SM_B, although functional control of M00: SM_C and M01_C are much more difficult to control against its counterpart. Its counterpart takes the benefit of handshaking interval between the two consecutive BS read transaction and force it to pause their next transaction until one of the FIFO is completely read out and is ready to be refilled again. While M00: SM_C and M01: M_C are challenging controlling as they don't get such handshaking opportunity where they can deterministically switch between the FIFO. As the streaming of the sequence data has to be continuous and precisely following the resolution of 20 ns (currently used!), it has to switch

deterministically between both the FIFO, one running out of data to another FIFO which is full and has a continuous line of the data. Deterministic switching of the FIFO happens within the resolution period of 20 ns, this ensures continuous streaming of data as if the data is being read from the DDR3 memory in constant mode at a frequency of 50 MHz.

Nevertheless, the hardware modeling is independent of reading clock frequency so in case if the requirements of the output ports are more than 50 MHz, it will adapt to it and is capable of deterministic switching the FIFO with own resolution. I am writing 20 ns and 50 MHz as an example only as this is our value in use. The Intrinsic details of the response signals resulting this process has been discussed with the help of their respective state machine in the upcoming section.

- M00: SM_A and M01: SM_A : These SM can read and write from/to any memory address for their respective master modules. Currently, we are reading data from DDR3 memory resource, although this SM can do a transaction with any other memory resources like BRAM generator i.e. which supports the AXI interface. A pulse trigger generated by one of the master (M00/M01) module process on the low to high transition in the state register. This pulse is (5 ns)longer so it can be captured by the master clock which is also running at 200 MHz. As this pulse is recognized in this SM and subsequently it presets some values and loads the relevant requested amount from the control register. This includes a number of the burst and number of repetitions required from the user, number of extra lines it needs to read if the requested sequence is not an integral multiple of the burst, make the DMA engine as busy using ff_done type signals and setting all debug signal to active-low in set it to active-high to the respective state to enable debug if an error occurs.

  This SM is Moore type which is also synchronous to the master clock of 200 MHz (currently configured). The signal (init_axi_pulse) is captured in the idle state of the SM_A and forwarded ahead to the next state (init_write) to perform the writing process. But this state is not used in current design as high to signal (u_read_only) makes it write protected. Although all write process which are currently there are in the program but not used. Disabling write protected signal will lead to undefined behavior in entire data flow structure, as the SM will start writing some incremental data initialized in its process. And since, the writing process is neither optimized and nor tested for the amount of data it will write or the number of the time it will overwrite, the already written sequence in the memory will be overwritten. Although this state has been ignored in the currently

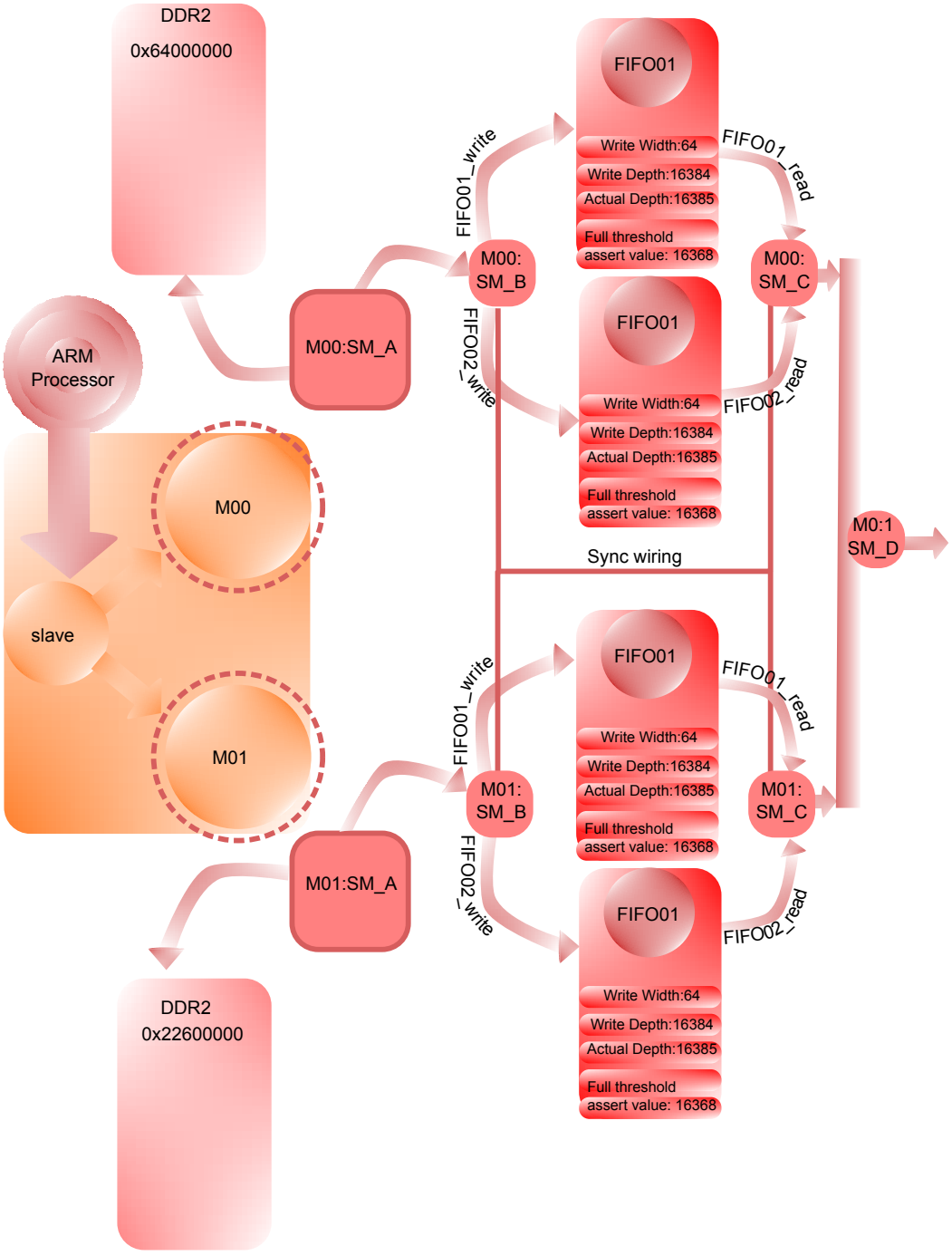


Fig. C.10 Block diagram representation of CIP functioning, where M00 and M01 is handling two stacked memory FIFO buffers and streaming the final synchronized data at the output port. SM_A, SM_B, SM_C, SM_D are the state-machines type which are used by both the master for streaming respective share of data (64-bit) in the CIP. The description of the state-machine types are available in the respective sections.

nevertheless it is essential to restructure this state if branching of the sequence has to be implemented.

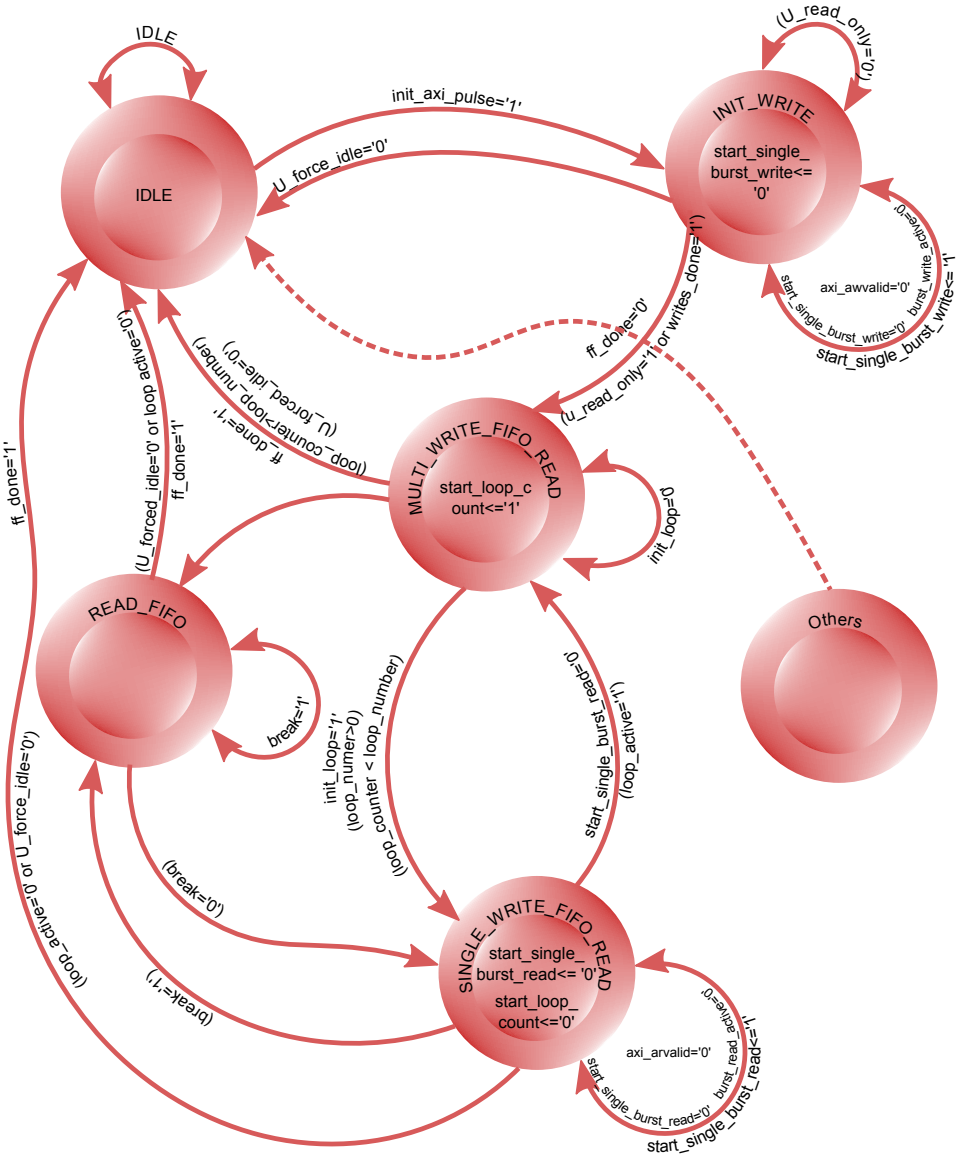


Fig. C.11 SM_A:SM for the reading the data from DDR3 memory

This SM is also Moore type, which is also synchronous to the master clock of 200 MHz (currently configured). The signal (init_axi_pulse) is captured in the idle state of either of the SM_A process and forwarded ahead in the next state (init_write) to perform the writing process. Although, this state has been ignored currently. I find it relevant to discus the importance of this state.

This state is not used in current design as active-high of the signal (u_read_only) makes it write protected. Although all write processes which are currently available in the program but not used. Disabling write protected signal will lead to undefined behavior of entire data flow structure, as the SM will start writing incremental data initialized in its process. And as the writing process is neither optimized and nor tested for the amount of data it will write or the number of the times it will overwrite, the experimental sequence stored in the memory will be overwritten by garbage data. Although this state has been ignored currently nevertheless it is essential to restructure this state if there is a requirement of changing the real-time executing data. For eg. Some predefined advance sequence can be hardwired in using several math functions in the combinatorial process, and a general wrapper can be used to transfer it to the memory and perform the standard experimental sequence execution. During the implementation of the sequence if the tailgater SMs gets trigger from the PMT section to change the currently programmed sequence then this state (init_write) can be requested to overwrite the programmed sequence. In this way actively running sequences can be altered during real-time execution. This will improve the current working style of all the sequence based programmable quantum algorithms and also enable the implementation of several complex algorithms.

After recognizing that the design is configured as write protected the SM_A moves ahead to the next state (MULTI_WRITE_FIFO_READ), where it notices the amount of the data that been written into memory and the number of time data has to be read repeatedly i.e looping of the sequence. It recognizes the amount of the data in term of a number of the burst transaction and number of the times it will redo this transaction. There are two counters configured to track the real-time progress of the amount of the data read and repetition number. It starts the repetition monitoring counter by invoking the signal (start_loop_count='1') from low, this is captured by one of the running processes that convert the active-low to high transition to 5 ns pulse. This pulse then triggers the repetition counter to increment by one and subsequently start the burst transaction by pushing the SM to the next state (SINGLE_WRITE_FIFO_READ). The repetition counter can count from 1 to 0x7FFFFFFF so request for 0 loops is not entertained while the request of a negative number is flushed by ARM PS while preprocessing the Ethernet data. Each time as repeat counter increments, the read address reset itself to the base-read address, the base-read address is the starting address of the sequence. The ending of the sequence has to be also properly synchronized using the pulse generator so that the exact time of ending of the burst the last transaction is well recognized and subsequently the ending of the sequence looping. A loop counter is actively counting

the number of the repetition there is another signal (loop_active) starts monitoring this counter, which begins (loop_counter) from 0 and continues up to requested loop number (loop_number). As loop_counter reaches the requested loop_number, loop_active set to low, this transition from high to low enables the generation of a short pulse generation equivalent to the master clock duration, which is captured by this state and subsequently this SM_A announces that successful completion of the requested size of data has been read and also requested looping has been completed successfully.

As the repetition counter increments, state of SM_A starts moving backward from (MULTI_WRITE_FIFO_READ) to SINGLE_WRITE_FIFO_READ to read the sequence and repeatedly repeat it as long as the requested number of the repetition is reached. This state cares for the regulating each burst transaction deterministically. The burst transaction starts by setting the signal (start_single_burst_read) to high that initialize the handshaking process with the respective slave and assert the modified current modified address to its slave to initialize the read process. As this handshaking process finishes this signal successfully is set to low again, and a counter starts which counts the read data as the master is also reading its read bus. It counts up to the preset number of the burst size(16,32...254) (BS16) and as it approaches the last data in the bus stream a signal called _rlast rise to inform the slave that it the last read data by the master and then slave pulls down the respective handshaking signals and waits for the next request from the master. This process is repeated each time a new burst transaction is started. The information presented in Tab. C.5 shows that handshaking and burst transaction duration during active data transfer. The first data during the burst transaction stay longer by one clock cycle (i.e. total duration: (BSxClock duration+5) ns) on the data line in the reading data bus. READ_FIFO is acting like a buffer state it neither care of the

Table C.5 Hand shaking and duration for reading data

BS	Handshake duration (ns)	duration (ns) for actual data reading
16	30	85
32	30	165
64	30	325

number of the loop nor cares for data reading from memory. The only goal of this state is pushing SM (SM_A) into a buffer mode where it remains as it is. It neither cares for tracking the current status of burst transaction nor the current repetition status. As explained earlier, that SM_A read the data from memory and writes into the available FIFOs from where the data is streamed at the lower pre-configured requested frequency.

As the write clock frequency is much higher against the reading frequency of the FIFOs, during this process, the FIFOs are no more available to write any more data although the sequence is still in middle course of it entirely. This pushes the need of a buffer state where write SM does not continue further while read SM are again reading the data commanding the requirement to empty the filled FIFOs for the writing machine to maintain. Ths READ_FIFO is the state where SM_A is pushed into for pausing the ongoing write processes. This information is generated by the read SM (SM_C) which is synchronous to the low running clock frequency. It reaches SM_A within 10 ns after its initialization. As once the burst transaction has started, it will continue to till the last data in the burst transaction is read. So this break signal is not issued when the FIFOs are full rather than issue when there is at least one empty stack still available in the FIFOs to accommodate the data of the ongoing burst transaction. This enables a quick response from SM_A and eliminated the chances of an error caused due to the fact the FIFOs are full, and the discrepancy can occur during this time. Write SM pauses here and usually continue once this signal is set to low by SM_C and informs SM_A to proceed again for the completion of the sequence.

In case of emergency stop request from ARM PS, master wrapper sets an emergency signal (U_force_idle) to low and which immediately revokes all requests in process and resetting it to preset values.

Table C.6 SM_A: SM states (mst_exec_state) and respective error codes

SM_A : State	Error
IDLE	0xF
INIT_WRITE	0xE
READ_FIFO	0xD
SINGLE_WRITE_FIFO_READ	0xB
MULTI_WRITE_FIFO_READ	0xA

The error code shown in Tab. C.6 for M00 master will appear at base-address of CIP at an offset of 0x1c at bit position[4..0]. While for M01 master corresponding error code for this state will look at location [4..0] at the same base and offset address of CIP slave register. As SM_A captures the generated start sequence pulse trigger, all ebug registers value are set to 0, so if all the value happens to be zero for long duration (more than 20 ns), this means SM is forced to redirect to others state. Much may find it uneasy to see the usage of others as a state in SM_A, but at the time of the designing, this SM

synthesizing and simulating this specific SM was showing error and complaining about missing state in SM_A although it this complaint was not confirmed with other SM(s).

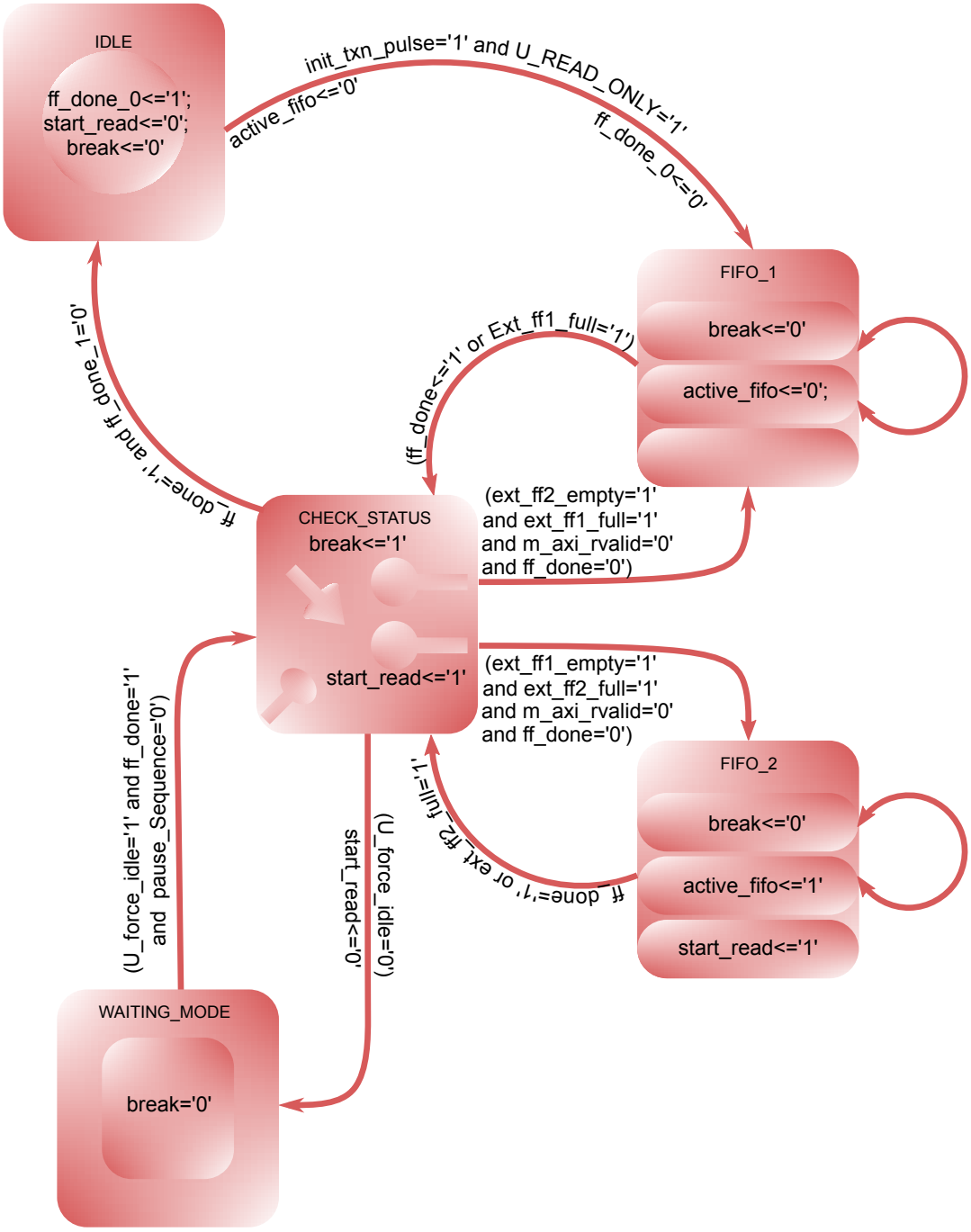


Fig. C.12 SM_B:SM for tracking and switching the FIFO. This state machine is responsible for writing into one FIFO and tracking to prevent any loss of data if it is full (i.e during wait time of the sequence).

- SM_B: This SM has been assigned to decide for the changing FIFOs based ongoing data traffic situation during the streaming. It keeps track of the situation of the data traffic flow and the status of each FIFO in advance to redirect the empty FIFO toward the incoming data bus from DDR3 and detach the FIFOs which has been filled. This can be interpreted as an intelligent switch which circumvent around the decision of connecting and disconnecting between two FIFOs. It is essential to know which FIFO is currently used for reading the stored data because the ongoing read process from the FIFO shall be able to rule out the writing process on same FIFO. As simultaneous read and write on the corresponding FIFOs may lead to undefined state within the FIFO SM (inbuilt SM of the FIFO) which will result in the data error. So this option must be ruled out during the design process, as nowhere in design one would like to add up some issue which might lead to corruption of data with even far off probability.

  Simultaneous read and write of the FIFOs might appear a tempting idea with less work around, but problem with such design will occur when FIFO will about to be empty, and a write process will be attempted, this will lead to undefined situation as FIFO might not be able to distinguish if the FIFO is empty or not. Due to simultaneous read and write with different clocks and the defined SM inside the FIFOs might not be equipped to handle such conditions. Subsequently, it will lead to either failure of all the other inter-connected SM or data error during the execution of the sequence. So it suggested not to avoid simultaneous read and write to the FIFOs. IDLE, FIFO_1, FIFO_2, CHECK_STATUS, WAITING_MODE are the five states of this SM, that are altogether executing the switching process between FIFOs successfully while avoiding the simultaneous read and write at any of the FIFO.

  The most relevant signal which is controlled through this SM is active_fifo, ff_done_0 and break and Start_read. active_fifo='0' means that currently read bus is attached to the first FIFO while '1' switches for the second FIFO. Another signal break='0' employ that one of the FIFO is currently available to continue the writing process into the available FIFO, while break='1' alarms the ongoing read process from the DDR3 that the no more FIFO is available for writing so SM_A must pause the ongoing read process from the DDR3. While **ff_done_0 ='0'** informs, it's status that this SM is actively working and any further request to process any other sequence shall be ignored. Such information does initialize from all the SM so that CIP can inform (on behalf of all the SM) to ARM PS that CIP is busy and further request for sequence launching will be ignored. **Start_read** is the signal which invokes the read process from the FIFOs. This information is passed

from SM_B to SM_C. SM_C receives this information and uses it's SM to subsequently read out all the sequence information stored into the FIFO.

In IDLE state (as similar to SM_A) it captures the standard sequence starting pulse (init_axi_pulse) and also checks if it work in write protected mode (u_read_only). As both conditions hold, it assigns the starting values to its control signals assuming that it is the start of the sequence. It allows the default FIFO (i.e., FIFO:01) to be written first with the data which is available on the read bus controlled by SM_A. The SM_B switch its state (FF_SWITCH)to next state which is FIFO_1, it stays in this state till first FIFO is filled. It also handles the situation that if the size of the sequence is smaller than the size of the FIFO and sequence is finished before the FIFO can be filled. It assesses the situation and issues Start_read commands accordingly which is recognized by SM_C to continue the read process from the FIFOs and subsequently redirects its current state from FIFO_1 to the CHECK_STATUS to analyze the current status of the easy data traffic management. This state (CHECK_STATUS) is dedicated to translating the status of the ongoing data traffic flow into the signals and redirects into the respective state to handle the current situation. If the data in the sequence is lower than the size of the first FIFO, then it waits until it receives the successful completion status from SM_C. After that, it redirects itself toward the IDLE state and be ready to receive a new sequence.

Nevertheless, in most of the sequence, the sequence size is bigger than the size of the FIFOs and SM_B does want to take the support of another available buffer FIFOs. In this case, it waits until the first FIFO is filled and invokes the read process which is captured by SM_C as stated. It detaches the first FIFOs and redirects the writing process toward the second FIFOs by changing its state towards CHECK_STATUS. CHECK_STATUS does recognize current situation redirects toward FIFO_2.

Meanwhile, the read process from the first FIFO has started while the writing process has been directed toward second buffer FIFO. FIFO_2 also assess the situation of ongoing traffic and follow up similar logic like FIFO_1. Second FIFO might be fully or partially occupied depending on the size of the data. In case if the second FIFO is partially filled then SM can safely wait until SM_C can declare its completion status, but in case if the sequence is bigger and the second FIFO is filled then it has to wait until the first FIFO is fully readout, and SM_C switches itself to the second FIFO to read out its data. This condition must be carefully managed as any overlap here might lead to mismatch or error

requested sequence data.

Another important aspect that has been carefully considered, as the burst once DMA transaction has started it can be paused (as recommended) only at the end of the completion of the burst transaction, so information for the available space in the FIFO has to be extracted before it really runs out to the limit. A different full offset parameter has been set into FIFOs which allows the FIFOs to issue a signal stating that FIFOs is full during the writing before it full. This idea helps the SM_A to complete the transaction without worrying that data might be overwritten or will be ignored by the FIFOs. The **Full Threshold Assert value** for all the FIFOs is **16368** while **Full Threshold Next value** for all the FIFOs is **16367**. While, the upper limit of 64-bit lines that can be accommodated is 16384. This means it has sufficient storage left when it informs the respective SM so that even if a burst transaction has been initialized after the full signal has been asserted it will be able to accommodate the ongoing transaction. It is recommended to use the different offsets if the BS has changed from 16 to some other value. Recommended offset for BS-32 and 64 are16352 and 16320 respectively. Although this offset has been set in which rules out any conflict or rewriting the data at the FIFO write port nevertheless it has been taken care on the SM_A side that once FIFO full has been asserted in the middle of DMA burst transaction handshake, it interrupts the building up transaction. In this way, we make sure that FIFOs is not fully occupied till its maximum upper limit.

Currently, 112 BRAM (according to the synthesized report) out of the available 140 in the ZC7Z02 based evaluation board is being used. Nevertheless, this number can be minimized if BRAM resources are needed for the other purpose for implementation of more features in the current design. The minimal amount can be as small as one as long as output streaming is being processed at 50 MHz. Configured FIFO is of the FIFO36E1 type which is 64-bit wide and 512 line deep. It seems that the Vivado tool optimizes the use of BRAM usage and use 4 BRAMs for 2048 lines as expected but needs only 7 BRAMs for 4096 lines. Similarly, it requires only 28 BRAMs for 16384 line. Again it will need 57 BRAMs for 32768 lines. This means the use of the FIFO generator to use BRAMs for designing the FIFO stacked memory seems to more optimized rather than using individual FIFO36E1 BRAMs instantiating to develop more FIFO depth by cascading these particular FIFO as has been done in the old design which was designed in Virtex-5.

Table C.7 SM_B states (FF_SWITCH) and respective error codes

SM_A : State	Error
IDLE	0xF0
FIFO_1	0xE0
FIFO_2	0xD0
CHECK_STATUS	0xC0
WAITING_MODE	0xB0

All the conditional HDL logic has been chosen meticulously in order avoid any conflict that can happen during processing of the data. This discussed algorithm works equally well irrespective of the size of the requested sequence. It has been successfully implemented in the current design and has been tested over months with infinitely many conditions to exclude any error chances.

- SM_C:

  This SM routes the filled FIFO toward the SM_D so that SM_D can read the data from the FIFO. This SM is one of most critical SM among all the SMs designed during the development of this design. As like other SMs, it does not get relaxation time like handshaking duration to prepare its suitable logic and synchronize itself to switch the FIFO right on time. Data has to synchronously to the reading clock and streaming continuously to the output port with a resolution period (as configured 20 ns currently). This needs very tight time bound (one clock cycle) conditions on the logic as within this duration the FIFOs has to changed and also data at the output port of the newer FIFO has to be ready enough to read in the next consecutive cycle. This means that the reading SM should be able to figure out that in advance the exact clock duration in which the last data of the currently read FIFO will be read out. This is critical because even single clock extra stay at the exhausted FIFO will result in reading last data multiple time. This will ultimately lead to a repetition of the data, resulting in a sequence data error. So, to avoid such a failure, this SM has been designed to track down the exact clock cycle when it will read the last data and starts the switching process. This is done so that by the time it reads the last data from the FIFO, and SM would prepare other logic to start read process from other FIFO without any need of extra clock duration. This process we call as deterministic switching between reading FIFOs. Currently, we are doing this for 20 ns resolution clock, but the design permits it to do at any frequency. As stated in the Table:C.7, the maximum clock that can be used to drive this logic is 230 MHz, and this condition is imposed by the FIFO logic as these BRAM FIFOs cannot be read for more

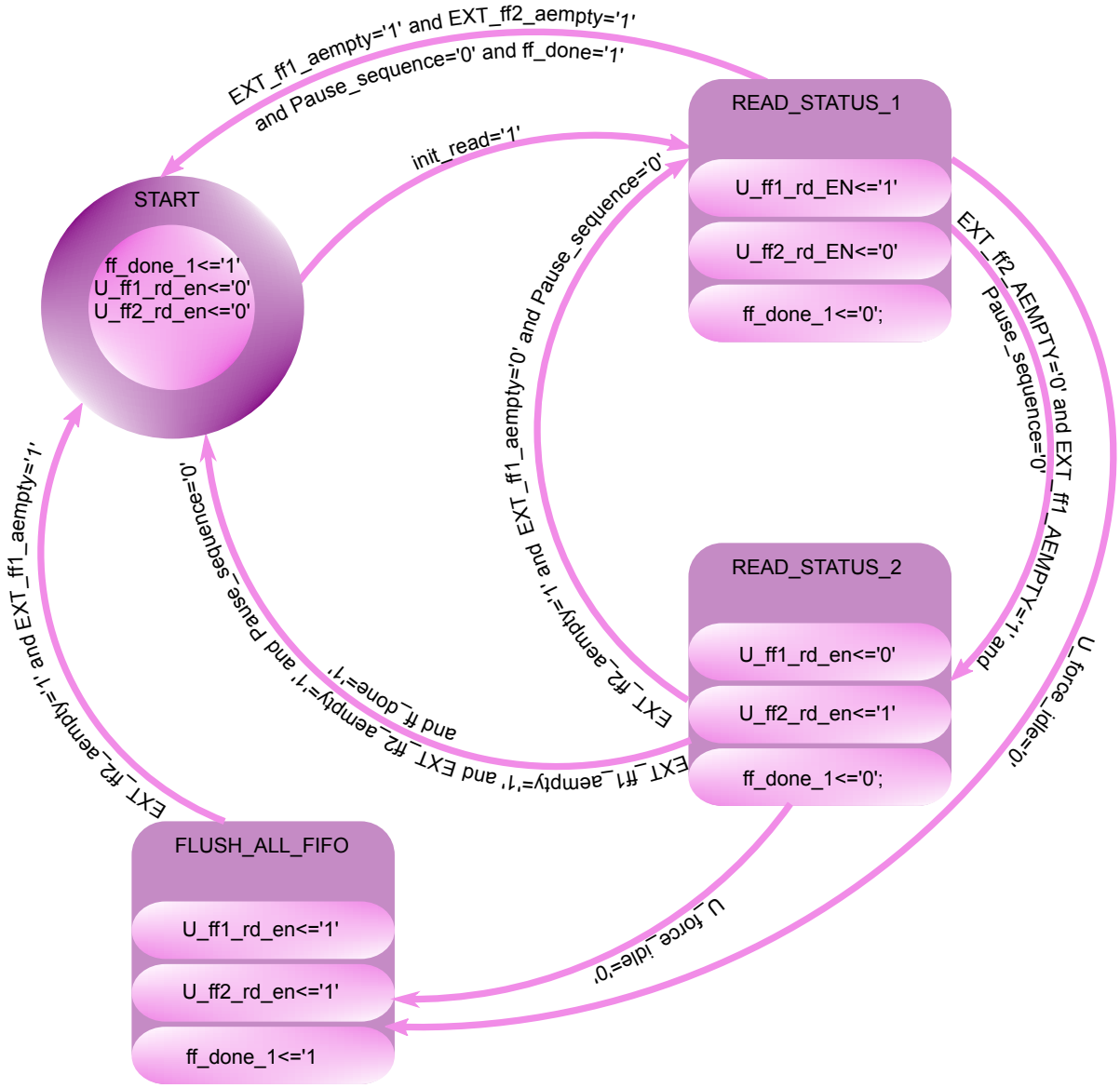


Fig. C.13 SM_C:SM for tracking and switching of both FIFO for reading purpose. This state-machine resolve the difference between completely empty or full FIFO and switch the FIFO to avail continuous streaming of data.

than 250 MHz. So if these FIFOs are being used in the mode where read and write clock are running independently at two different frequency then maximum which is support by design is 250 MHz. This is the maximum permitted as per technical specifically[5] of Xilinx.

[5] PG017.

Nevertheless, the idea used in this design can successfully switch the FIFOs are at any clock frequency. There is no restriction from the design side. As said it the specification limit of the logic of the BRAM FIFOs. Also, this restriction is independent of the mode in which FIFOs have been configured. The product guide of the FIFO generator from Xilinx describes all the feature and its specification in detail[6]. To achieve the success of this algorithm well tested predicted relation between reading enable and write enable signal and has to be known in advance and also well tested.

To get this idea working, an SM (see Fig. C.13) with four states has been designed. All the FIFO has to be configured in Interface type:Native, read mode:first word fall through (FWFT). SM_B initialize a Start_read signal under the condition (discussed in the last section), this signal is received by one of the processes which are a dependent process to SM_C. This process converts the Start_read signal into a pulse (duration equivalent to the configured clock: 20ns) which is captured by SM_C in its IDLE state to start reading the data. Read process starts by setting the read to enable signal (U_ff1_rd_EN='1') of first FIFO, while making sure that the read enables signal (U_ff2_rd_EN='0') for the other FIFO is still set to low.

Similarly, like other SMs discussed above this SM also acknowledge to the other section of the process that it is busy (ff_done_1='0') and another sequence shall not be requested as stated in the last section and also pushes the SM_c idle state to a newer state of READ_STATUS_1. In this state, it checks tracks down the empty signal, and as it finds this high, it tries to figure out the status of other FIFOs which should be non-empty or if this empty it reflects that sequence has finished. So based on the almost empty signal of the FIFO, it switches to the newer filled FIFOs. As per documentation[7] almost empty flag rises just before the last word in the memory, so this flag is used to extract the time information of its previous word content in the FIFO. As in sequential logic if a signal has been assigned a value this update is only visible in next clock cycle, hence in next clock cycle it combines with the pause status signal (discussed in the next section SM_D) in combinatorial logic and enables the actual read to enable signal (Ext_ff1_rd_en). Similarly, it moves to the next state (READ_STATUS_2) or IDLE after successfully reading the first FIFOs, depending on the conditional status of the data flow. This process is repeatedly repeated till the end of the complete sequence.

[6] PG017.
[7] PG017.

While implementation of this design, another technique which was based on the counting of data while writing and reading to the FIFO. A counter was also initialized each time the writing process into FIFO was initiated, this counter incremented at writing clock frequency while when reading started, it decremented with reading clock frequency. This way we have initialized two counter to track the down number of 64 bit wide data writing into FIFO. Although this method was successfully implemented, we, later on, realized that the same could be accomplished using the almost empty flag in the native interface mode. We preferred the first method as it reduces the size of the necessary logic for this design. It already seemed to grow exponentially during development stages. So all the effort has been tried to make it compact and simple. Nevertheless, the counter based approach was much more robust as it never required and preset configuration of the FIFOs. It could work irrespective of the memory resources type that has been used in designing the FIFOs.

It is highly recommended being very careful here as any small change might make the entire project unstable, so the developers are requested to look into the technical specification of the FIFOs, and it related documents[8]. As the stated aim of this thesis is to provide the idea behind the development of this project with minimal technical information. Discussing all the relevant section might be beyond the scope of this thesis.

Table C.8 SM_C states (READ_START) and respective error code

SM_C : State	Error
START	0xF000
READ_STATUS_1	0xE00
READ_STATUS_2	0xD00
FLUSH_ALL_FIFO	0xC00

- SM_D: Actual data that has to be streamed directly to the output port is already available at the 64-bits wide signal buffer (Zynq_output_buffer_2) in a process which is synchronized with the read clock (50 MHz). But it cannot be used to stream as the data which is available as record shall be read and differentiated before streaming as it might contain multiple time information. So to recognize and implement the time-related request as performed in the sequence, there is a need for an SM which can be read and implemented as requested. SM_D has been implemented for serving this purpose of reading and performing the time request of the sequence.

[8] UG416; PG017; UG912.

This is the last SM among the architectural pillar of the SMs that has used to realize this design on actual board. This SM is synchronous to the output streaming clock. The primary task of this SM is to receive the data from (Zynq_output_buffer2) and reprocess it in the sense that if there are any timing related information in the data, then this SM shall be able to resolve. It is responsible for implementing any timing interval requested in the sequence that includes the option to trigger it at external synchronization also. Beside this, it is also responsible for managing the FIFO out the signal to the external ports without any error. It realizes its task using following logic in the design.

1. Transporting data of the changed FIFO to the output port.
   A mealy type of SM performs this task deterministically. It is essential to implement a mealy SM here as the final output at the port is dependent on the data itself. For example, if the data contains a request of specific time duration, then the output shall change only at the interval of requested time in the sequence and meanwhile it shall be able to keep the output port stick to the last reported data. If we implement a more machine here and the output is synchronous to the continuous changing clock which means that the clock will continuously update the same data. And for any reason idea to stop the clock or stitch the last output to the port shall serve as a very deterministic way of doing it. This is the reason why Mealy SM has been used in this design for final data transportation. It keeps the state static during the requested time interval or the if this is an infinity long wait duration for the external trigger and prevents any change in the output ports. As any update even far off will have adverse effect on running experiment.
2. Manage the timer for precise counting.
   This SM reads all the data as it passes through toward the output ports. If it encounters delay information embedded between the continuous line of words in data. It restores the last read words from recorded sequence to the output ports and subsequently starts a timer. This counter starts from 2 and can go up to 2^{31}. The starting point is set to 2 as it takes two clock cycle (40 ns) to initialize and start the counting process. Hence, if the time gap requested in the sequence is less than 60 ns, it always gives 60 ns while any required delay beyond the 40 ns is accurately delivered. Since the timer is synchronously updating with reading clock, this is the reason the read clock always decides resolution.
3. Synchronize the output data with external trigger.
   As stated this SM reads the sequence records before forwarding it to the output port. It distinguishes well between the request of time delay, or it should wait until

external trigger redirects the leftover sequence records. In case, if the requested time is either infinite wait-time or external trigger, the sequence will update the previous value on the output ports for infinitely long time till external trigger is received and the SM allows for further processing of the experimental sequence. This triggering is also accepted with a time resolution of 20 ns. As the configured read clock has the 20 ns resolution so any attempt to trigger with less than 20 ns will show non-synchronous data streaming behavior.

More details on embedded sequence have been presented in the software section. Mealy SM SM_D machine needs five states to implement the task discussed above at logic level (see Fig. C.14). In an IDLE state, it captures init_read_buffer pulse generated by one of the processes. The signal, init_read, generates this pulse which is a synchronized signal generated by the design wrapper of M00 and M01. As described earlier, SM_C of both the masters (M00 and M01) initiates a Signal, Start_read, whenever their respective FIFO is ready to read, this signal from both masters reaches to their joint wrapper of CIP which is sitting above both masters (M00 and M01) in the same hierarchy level. The top-level wrapper of CIP receives the, Start_read signal from both master and initialize another signal (init_read), that informs SM_Ds of both masters that their counterpart is ready and hence if both deliver the data, it will be synchronized. So, to sync it entirely, this init_read generates a 20 ns pulse that is captured by the both SM_Ds. This way we make a method for synchronizing the lot of 80 analog channels and 27 digital channels. And also keep the option of syncing the more module (N_BERTHA) open and hence paving the possibility of designing the segment controller for more than 80 segments as discussed in the upcoming section.

The IDLE state of SM_D forwards the current state to SIMPLE_OUTPUT upon successful capture of (init_read_buffers). It manages (SIMPLE_OUTPUT) unabated streaming of the general data. Data of the (Zynq_output_buffer_2) is routed to the (Zynq_output) which is the final output from the Zynq boards. If any timing request is encountered in the sequence, then that specific word is recorded in a new signal (Zynq_output_buffer_3) and the current state is forwarded to the next state (INCLUDE_TIME_INFORMATION) where it extracts the time delay that is requested between subsequent data words. According to the currently implemented scheme bit position(63) is reserved to indicate the time-related request. IF 63^{th} bit of the sequence is set to '1' this inform the presence of the time-related request in the next subsequent line while the presence of this data ($0\times$FFFFFFFF) in the next succeeding line is considered as wait forever which means

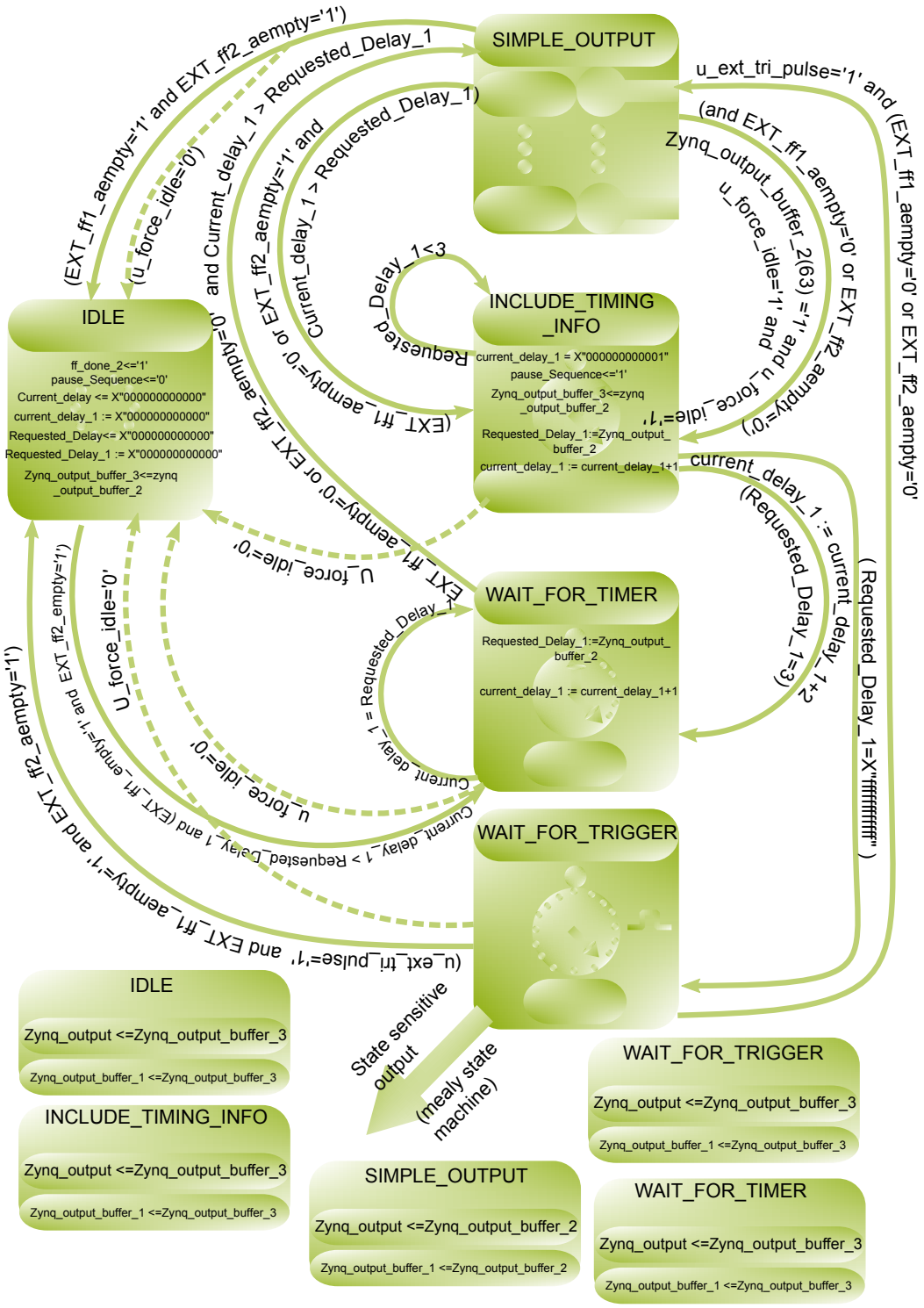


Fig. C.14 SM_D:Mealy type SM for enabling the data to the output ports. This state machine act as an output state to control the latching of erroneous data into bus and subsequently into the output pin.

some external trigger will determine the delay between two subsequent words. While beside this, any other words are treated as requested delay (words$x$20 ns) duration. In case of wait for specific duration delay current state move to the (WAIT_FOR_TIMER), while infinite time delay is forwarded to WAIT_FOR_TRIGGER state. During the stay of the current state in either of this state, final Zynq_OUTPUT is tied to the (Zynq_output_buffer_3), which contains the information of the last words of the bus before the delay information is read. As long as the current state stays in either of this state, bus Zynq_output_buffer_3 updates which rule out the possibility of updating any garbage information on the output port. Hence, acting as the deterministic streaming of sequence data record.

The possible error code will be written at the respective registers. It is strongly rec-

Table C.9 SM_D: SM (out_state) states and respective error codes

SM_D : State	Error
IDLE	0xF000
SIMPLE_OUTPUT	0xE000
INCLUDE_TIMING_INFO	0xD000
WAIT_FOR_TIMER	0xC000
WAIT_FOR_Trigger	0xB000

ommended to look into debug register to notice the origin of the error incurring in the sequence. Although beside this as there were infinitely many possible errors may commit while improving this project in future and whose origin might not be traced well, in all those case I would recommend to make logic time bounded and try avoiding all possible latches and digital glitches.

This SM can contain the logic of reading the records of sequence data so more options can be inserted here in this SM to make the sequence more comprehensive as discussed in the outlook sections. Data width 62 and 61 is still open to be used for similar implementation.

Although I do believe that the logic can be more optimized, apparently neither there will not any substantial saving of the device resources, nor it will show any improvement in the low-frequency output streaming, which we are using. Nevertheless, optimization of logic might be useful and necessary when there is a requirement of streaming the final output at the higher frequency more specifically at the edge of the upper limit of the frequency mentioned in the table:C.4. All these SM does consume substantially low % age of the total available device resources. The overall user device resources by all the SM and also total utilized have been

written in the appendix.

During the development of this project, there might encounter with infinitely many problems such as timing failure, unable to allocate the requested I/O buffers, unavailability of device resources and others. The discussion of all these issues will be out of scope for this thesis and also might appear as non-ending discussion. However, starting with project provided along with the digital copies of this thesis might substantially reduce the number of such problems as the environment variable has been already optimally preset there.

The port description of CIP and the sequential/ non-sequential processes (list up to 29 such processes) used to process the output and input signal of the CIP has been described in the appendix.

Data transfer methods

An elegant way for data transfer from the host computer to the FPGA (Zynq-702) boards have to adapt for optimized performance for the digital architecture discussed above. There were two modes which have been considered during the development phase either using USB mode or Ethernet mode. USB mode of transferring the data has been tried, but it was dropped mainly because USB drivers on the control computer often fail to respond due to multiple USB connections on the control computer. And also USB2.0, which is available on the board has minimal data transfer rate which might not be sufficient for transferring the large chunks of data from the control computer. But as USB appearing an easy way of the transferring point-to-point data in short distance and less overhead might be way ahead of the transferring the data. But considering all the fact, we decided to implement Ethernet mode of transferring the data as the data transfer rate was much better in this case. Nevertheless, we could achieve the speed of 50 MB/s through USB mode.

Transfer using multiple Ethernet mode

There could be a multiple way Ethernet mode of data transfer might be implemented for fast and deterministic data transfer. I will discuss the three ways that we have tried to achieve this.

1. NDIS protocol driver
   This method was a natural choice for implementation as it was/is already working on our old firmware. But there were several issues that we have to address before this mode of transfer can be adapted in the new generation design. Data transfer rate and future Operating System (OS) compatibility were some serious concern. Beside this old

firmware has a maximum sequence capacity of ∼60 MB, while the discussed firmware is supposed to support ∼15 time more data, which might not be easy to go using this protocol. Transferring large chunk of data using protocol was difficult as it reportedly could not allocate more continuously buffer in the chain to support the extensive data available at the Ethernet FIFOs. Nevertheless, this was also supposedly using scatter gather (SG) mode of the DMA transfer from Ethernet FIFOs to the allocated ring buffers in onChip memory (OCM).

2. using Linux server
   Embedded Linux can be extracted on the SD cards using standard methods as recommended by Xilinx for Zc-702 boards. Embedded Linux has inbuilt Linux servers which can be used to receive the sequence data from the host computer. Standard Linux files can be configured to share the interrupt of the Ethernet data receipt call. This interrupt line number can be used to recognize the requested sequence and execute it. This will not be very straightforward for implementation, but it has already been achieved in the early stage of its development. But it will benefit in managing and storing multiple sequences simultaneously due to the presence of the virtual memory mapping in the Linux. The very first experimental measurement commenced in the lab has used this method of data transfer.

3. embedded LWIP for Zc-702
   lightweight (LW) IP [Dun01] is an open source networking stack designed for the embedded system, which was initially developed at the Swedish Institute of computer sciences by Adam Dunkels in 2001. LWip is customized for full implementation of TCP-Stack with reduced onboard resources. More customized release of this program has been made available by Xilinx [ASU14] for our device. It initializes all the necessary register of gigabit Ethernet controller (GEC) to implement 1Gb/s full duplex ethernet networking in Dynamic host configuration protocol (DHCP) mode. Before importing this design for the embedded system general idea of LWIP, GEC of the Zc-702, an Ethernet frame is essential and hence recommended to overview the given references here.

Sequence data sent from control computer is handled by media access controller (MAC). MAC receiver handles the receiving of valid data available at the Ethernet port while MAC transmitter is responsible for packing the data into Ethernet frame and sending to the host. Block diagrammed of Ethernet controller ([UG517] Fig:16-1) shows the movement of Ethernet data through advanced high-performance bus (AHB) and access to slave register through advanced peripheral bus (APB). Ethernet communication initialized

by LWip first initialize the certain generic which are generic to the desired Ethernet type protocols. It follows up and initializes the DMA controller either in SG modes (used in design). In SG mode DMA controller prepare a set of ring descriptor, which is nothing but the several groups of continuous commands, where each group states explicitly the amount of data to transfer, address from where data has to be received, the address where data has to be written back and finally address of the next descriptor. This is a standard and more efficient way of data transfer through DMA controller because in this case, an interrupt is issued after the last chunk of the data has been transferred rather than releasing after every successful transfer of the data. This is called ring buffer because the last descriptor contains the address of the first descriptor. This method of transfer of data through DMA transfer is similar to the data transfer technique discussed in the earlier sections. Ring descriptors for either transmit or for receive are allocated on fast, accessible memory region so that access to this descriptor is quick and easy as these will decide the movement of data from FIFOs to the allocated memory buffers of the MAC controller. Memory region from $0\times$00000000_h to $0\times$0002FFFF_h is an active accessible OCM region where LwIP does dynamic initialization of it's receive or transmit ring buffers descriptors to perform SG mode DMA. And for this reason, the memory space 100 MB, from $0\times$00000000_h to $0\times$0002FFFF_h have been left unused on the FPGA side.

Connecting to the LWip network stack

There is a specific constraint that the sequence record has to be followed before it can be allowed to execute on the discussed firmware.

- sequence sending protocols

  The layer (see Fig. C.15) suggests the step for wrapping the sequence data into the Ethernet frame. Although, included description is windows 7 OS specific nevertheless similar socket control can be programmed on the Linux machines also. The C++ program compiled in visual studio 13.0 Onward release is part of the digital submission due to substantial content. It is currently used to establish the client-server connection between the firmware before sending the sequence records. This communication protocol can also be accessed in the local network, but it is not recommended doing so as this will degrade the overall optimized performance of this device. It is not secured against oncoming connection request from the arbitrary host so any computer can be connected to this machine and send invalid sequences which might push the machine into sleep mode. Also, optimized data transfer rate might be affected if it is used on the network. Hence, standard one-to-one communication must be established for optimal and secured

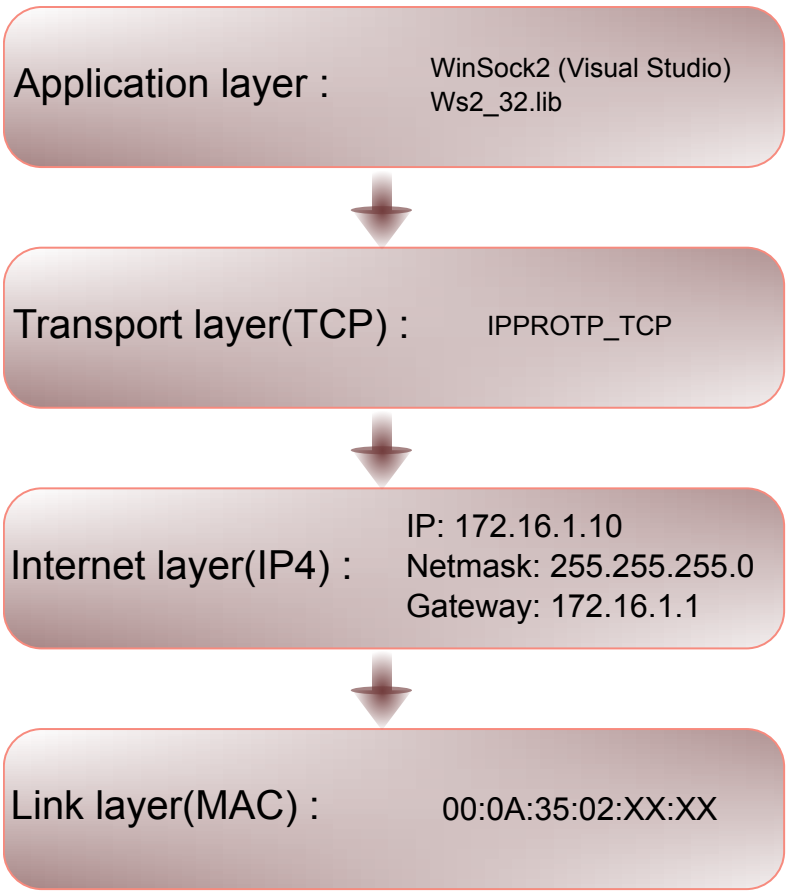


Fig. C.15 Different layers of Ethernet protocol in design

performance from the machine. Needless, but it is essential to mention that the host computer should share the same gateway as of the device to establish TCP/IP based connection successfully.

- Arrangement of the sequence record
  RAW application programming interface (API) echo server [ASU14] has been upgraded for implementing in this design. The callback function rxperf_recv_callback receives the Ethernet packet for preprocessing of the sequence records. Currently, in the customized form of LWip, data on the next Ethernet packet is untraceable, so information about the size of the total sequence records has to be extracted from the first packet as it receives. Hence, a pre-definition of the experimental sequence has been set (see Fig. C.16) for differentiating between valid and invalid data in the sequence. The sequences are assumed as illegal which does not have their data record arrangement as per predefined protocol (see Fig. C.16,C.17). The invalid sequence are flushed completely, and the machine moves to the sleep mode indicating that sequence generation is faulty and software

compiler needs to be revised before sending any more data. This feature acts an extra security layer in stopping the execution of the wrong sequence on the Quantum Computer. In case of valid sequences, the data are written at the respectively assigned memory of M00 and M01. During the ongoing write, promised size of the data is continuously checked against the received data, and any mismatch is considered as an illegal attempt to run an incompatible sequence structure forcing the machine to move to sleep mode and flush the received data, so far. There is the possibility of adding mathematical functions to check the validity of the quantum algorithm. Currently, the experimental data received is accepted as valid quantum algorithm if it follows the protocol (see Fig. C.16,C.17) strictly.

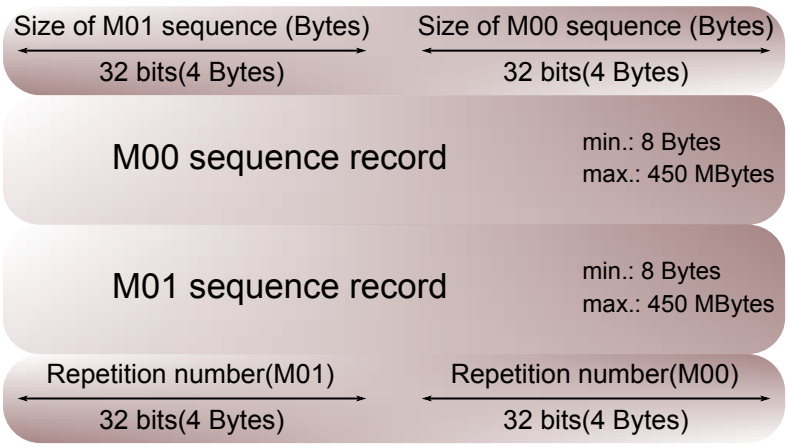


Fig. C.16 Structured sequence record format in 64-bits as prepared in the host computer

- maximum transmission unit (MTU) configuration of the control computer MTU is another additional constraint required for matching the data processing protocol at ARM processor. In windows, MTU defines the maximum packet size of the Ethernet frame, the preset default value of MTU is 1500, which is maximum possible size of Ethernet frame that Windows or any linux machine can build and send it over Ethernet. Unlike jumbo frames which is special where upper limits is around 9000 (Bytes). By default, the maximum payload (MTU=1500) can be transfer (0x5A6_h=1446 Bytes) of data in one frame. As 0x5A6_h cannot use 32 aligned memory optimally, so a new value of MTU=1480 has been adopted for transferring the data. With MTU=1480 the newer value of maximum payload is 0x5A0_h (1440 bytes), which can be written into 32-bits memory as 32 bit aligned unsigned int data structure. In 0x5A6_h format, writing the last 6-byte into memory will need data structure as char, which acts as bottle-neck in faster data transfer.

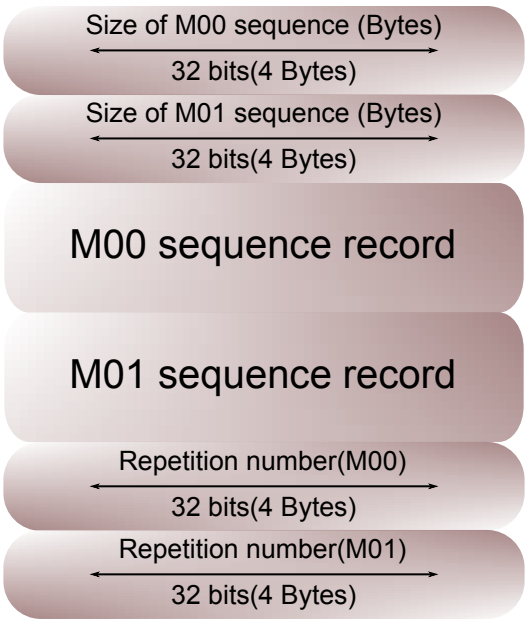


Fig. C.17 Structured sequence record format in 32-bits aligned memory format as received by the SoC

```
0 Size of payload(p->payload) 5A0_h Bytes
M00_size 1E50_h Bytes
M01_size 1E50_h Bytes
Avarage Payload 1E50_h Bytes
M00_address=6400000_h
M01_address=22600000_h
1 Size of payload(p->payload) 5A0_h Bytes
2 Size of payload(p->payload) 5A0_h Bytes
3 Size of payload(p->payload) 5A0_h Bytes
4 Size of payload(p->payload) 5A0_h Bytes
5 Size of payload(p->payload) 5A0_h Bytes
6 Size of payload(p->payload) 5A0_h Bytes
7 Size of payload(p->payload) 5A0_h Bytes
8 Size of payload(p->payload) 5A0_h Bytes
9 Size of payload(p->payload) 5A0_h Bytes
10 Size of payload(p->payload) 46C_h Bytes
Repetition number 100000
```

Fig. C.18 COM port output serialized on the putty while receiving the Ethernet data

Performance of the established Ethernet connection

The analysis recorded (see Fig. C.18 and Fig. C.19) for real-time data transfer has been deliberately measured using Cygwin on Windows 7 OS, during the optimization of the RAW

API based connection for the real testing of the experimental sequences. The maximum possible through output is 1 Gbits/s hence in this firmware we could achieve the transfer rate of ∼980 Mbits/s which is close to the maximum possible value and also in the whole argument with recommended value. Fig. C.19 is very similar measurement has been demonstrated in [ASU14]. Although, the measurement (see Fig. C.19) was recorded after disabling the initialization register and leaving rest of the pre-processing active. This way frame packets are deliberately sent to SoCs Ethernet port for 1 sec, and a receipt was received for each successful transfer. The repeated measurement for 10 sec provides statistical performance report for continuous data transfer in the firmware. It shows that even with pre-processing a decent data transfer rate of 730 Mbits/s can be achieved.

```
kaushal@vkaushal-PC ~
$iperf -c 172.16.1.10 -i 1 -t 10 -w 64K
------------------------------------------------
Client connecting to 172.16.1.10, TCP port 5001
TCP window size: 64.0 KByte
------------------------------------------------
[  3] local 172.16.1.200 port 29312 connected with 172.16.1.10 port 5001
[ ID] Interval                Transfer          Bandwidth
[  3] 0.0-1.0 sec        86.9 MBytes          729 Mbits/sec
[  3] 1.0-2.0 sec        87.4 MBytes          733 Mbits/sec
[  3] 2.0-3.0 sec        87.1 MBytes          731 Mbits/sec
[  3] 3.0-4.0 sec        87.6 MBytes          735 Mbits/sec
[  3] 4.0-5.0 sec        88.1 MBytes          739 Mbits/sec
[  3] 5.0-6.0 sec        86.6 MBytes          727 Mbits/sec
[  3] 6.0-7.0 sec        87.0 MBytes          730 Mbits/sec
[  3] 7.0-8.0 sec        87.2 MBytes          732 Mbits/sec
[  3] 8.0-9.0 sec        84.6 MBytes          710 Mbits/sec
[  3] 9.0-10.0 sec        87.2 MBytes          732 Mbits/sec
[  3] 0.0-10.0 sec         870 MBytes          730 Mbits/sec
```

Fig. C.19 Data transfer rate analysis of the RAW API based communication established between control computer and the firmware with necessary data preprocessing.

The tabulated info (see Tab. C.10 shows the transfer rate with the similar protocol as used in the lab. Transfer time is actual sequence transfer duration. While execution time is included contains passing of the execution command over Ethernet, waiting for the sequence to complete and receive the completion message. It has been measured by Thomas Ruster using the standard visual studio based software MCP. In this measurement the max. the data transfer rate of 550 Mbits/s has been achieved, which is 20-25% lesser than the directly measured value on the firmware development computer. Slightly reduced performance might be due to

```
kaushal@vkaushal-PC ~
$iperf -c 172.16.1.10 -i 1 -t 10 -w 64K
------------------------------------------------
Client connecting to 172.16.1.10, TCP port 5001
TCP window size: 64.0 KByte
------------------------------------------------
[  3] local 172.16.1.200 port 29312 connected with 172.16.1.10 port 5001
[ ID] Interval               Transfer          Bandwidth
[  3] 0.0-1.0 sec        109 MBytes          918 Mbits/sec
[  3] 1.0-2.0 sec        113 MBytes          946 Mbits/sec
[  3] 2.0-3.0 sec        111 MBytes          934 Mbits/sec
[  3] 3.0-4.0 sec        112 MBytes          944 Mbits/sec
[  3] 4.0-5.0 sec        112 MBytes          938 Mbits/sec
[  3] 5.0-6.0 sec        110 MBytes          927 Mbits/sec
[  3] 6.0-7.0 sec        112 MBytes          940 Mbits/sec
[  3] 7.0-8.0 sec        113 MBytes          945 Mbits/sec
[  3] 8.0-9.0 sec        112 MBytes          938 Mbits/sec
[  3] 9.0-10.0 sec        111 MBytes         932 Mbits/sec
[  3] 0.0-10.0 sec        1.09 GBytes        936 Mbits/sec
```

Fig. C.20 Data transfer rate analysis of the RAW API based communication established between control computer and the firmware without any data preprocessing.

the Ethernet adapter card or due to multiple hierarchy levels of the software which could delay the overall response time. Nevertheless, this value is still about ten times higher than previously used firmware which was using NDIS based transfer protocol. The substantial improvement in the data transfer speed is due to the handling of the optimized LWip based RAW API network stack while improved execution overhead is due to newly implemented hardware (discussed above) design.

Table C.10 Sequence transfer rate measured in MCP

Sequence size (Bytes)	Data transfer rate Mbits/sec		Execution overhead (% of total time)	
	Zc-702	Virtex-5	Zc-702	Virtex-5
6108	71.47	57.66	2300	687
60828	315.70	57.98	364	310
304028	458.41	67.90	100	277
608028	483.22	69.40	47	272
3040028	544.19	70.88	10	269
6080028	544.19	70.45	5.4	308

Table C.11 Sequence control protocols via Ethernet

Sequence size (Bytes)	Operations
1	Full software reset
2	Restart
4	Restart with new repetition
>5A6	Close socket

Feature in currently used network transaction

Besides sending the standard formatted sequence, there are some additional features that has configured on this device. The information provided (see Tab. C.11) shows other possible controls of the N_Bertha by sending some specific data type over the Ethernet port. If ARM PS receives a single byte of data, it takes this as reset request and resets the currently running sequence on M00 and M01. This feature is useful if a long wrong sequence has been requested which takes several minutes or hours for the execution, in these circumstances this feature proves handy to terminate the running sequence using the software. Data of any 2-bytes are assigned to restart old sequence. It proves advantageous when control computer does not want to wait for the sequence transfer, which means MCP (control software) can send the sequence and start doing some other task meanwhile and at its ease, it can trigger using by sending 2-bytes to start the sequence. Also, this feature can be used to restart the previous sequence. New repetition value request can be processed by wrapping its value in 4 bytes frame and sending it. While a frame size of greater than $0\times5A6$ can be sent to close the TCP socket, Ethernet frames of this size is generally packed and send by windows when a request to close a connected TCP socket is requested.

Interrupts handling and its transmission over Ethernet

There are three interrupt lines installed in this design. Out of these, only two are used. The third interrupt is dedicated to the timer (line number: 63) which is currently not configured for use. Nevertheless, it is present and ready for use. Two configured interrupt lines are hooked to CIP, and general purpose input and output (GPIO). CIP interrupt line (line number: 62) is used to inform the ARM PS about the successful completion of requested sequence. Another GPIO-interrupt line (line number:61) can be invoked by push button (SW15),which is used to check correct installation and initialization of the device. It can be also used to execute a sinus signal with an amplitude of ±40 V on all 80 analog channels forever by pressing once, and subsequent pressing reinstate to the normal usable state and hence allowing external software (in our case MCP) to take control via Ethernet protocol as discussed in earlier. The hardwired interrupt line in the design needs to be addressed in the software to get control of it. This

is done by initializing an instance at the specific address of the interrupt controller, and the interrupt line is addressed to find the right line for it. If the lines have been figured out, then its line-number is used to configure call-back functions. Activation of the event register a call on the connected line (interrupt-line) and hence immediately calling their call-back functions attached to it. The line number 61 is writing the sequence into the memory when it is pressed for the first time while second press it resets the registers. Similarly, line number 62 creates a TCP-packet and sends data on port (port number 5001), which is listened by the control computer and recognized as successful completion of sequence.

C.4 Development of analog electronics

Analog electronics has been developed after successful completion of the digital electronics. So, analog unit stands next in level of the hierarchy from development viewpoint. In this section, description of Backplane, multi-channel Analog cards, power supplies has been discussed in their respective sections. The backplane provides physical and electrical support to these analog cards and power-supplies. Digital signal generated by SoC-FPGA based design has to be transferred to DACs systematically to persuade a full-fledged running system that can support quantum register reconfiguration by provoking right shuttling operation. Therefore, a properly designed DACs and its amplifiers are grouped and connected to time-dependent digital signal produced at digital section with right impedance. The development of overall design layout of this section has been done by me and Dip. Ing. Heinz Lenk.

In the first stage, the design of back-plane has been prepared which set the stage for distribution 100-digital signal generated via SoC-FPGA with necessary power resources and other signal are directly transferred from FMC-adapter. Then a proper rearrangement of DACs has been structured to support the presence of maximum DACs on a single printed circuit boards (PCB). These analog cards have been designed to be constrained within 6 HE height and 19"-compatible rack. Beside this, the power supplies have also been designed that can support simultaneous swing of voltage range [-40, 40] V in all analog channels independently. And lastly, the conceptions and design of cables that can sustain such complex and sizable analog voltage sources have been developed (discussed in Sec. D.16).

At each stage, several strict preset standards have been met to develop an electrically sustainable system with optimized performance. For say, the entire unit altogether with back-plane, several analog cards, SoC-FPGA , power-supply, shielded cabinet (housing for all the electronics), TTL digital output for pulse control, along with the designed cable has to function

reliably in the lab environment. And also, it should fulfill the stringent requirements needed by the ultracold ions, which are very sensitive to technical noise (see Sec. 4) (for more info on result see Chapter. 4 and 5).

The basic functionality and performance of analog units has already been discussed (see Sec. 4). In the upcoming sections, PCB design attributes and circuit analysis of different units has been discussed.

Back-plane

The general description of backplane has already been presented (see Sec. 4.2.2). It provides mechanical and electrical support for power supply unit, multi-channel analog cards, and SoC-FPGA . The SoC-FPGA digital lines and the power lines of the power supply are distributed among the analog card via this. It is screwed at the back-side of metallic box[9] of N_Bertha, so that can hold 5-analog cards, 6-power supply and 1-SoC-FPGA board. All these units have to plugged into their respective slots as shown in Fig. C.4.

Description of the backplane PCB

It is 429.2 mm$\times$262.0 mm large, four layered PCB. Each layer is distinctively used for either power or digital lines. In top-layer, low voltage digital-lines signals are distributed and second layer acts as dedicated GND plane for top-layered signals. Through this method, we have tried to maintain similar impedance for all the digital signal. This idea of signal distribution is also very fundamental to the design as later on in the analog section we will see that it is mandatory to maintain the signal integrity within delay-limit of $<$3 ns for deterministic programming all analog channels. The distance between first DAC and the last DAC is 700 mm, which might easily have delay of $\sim$2 ns. So, any mismatch in net impedance for any of the digital channels may lead to severe timing issue which might be difficult to compensate with discussed digital design (see Sec. C.3). Therefore, while designing PCBs of the backplane and analog cards we have tried to maintain the integrity of all the digital signal identical to each other. The third layer contains a power plane for VCC, +45 V and -45 V, also there is GND-plane for the digital and analog section separately. The bottom-most layer (fourth layer) contains power planes for +2.5 V and +5 V and also ground plane. The figure shown in Fig. C.21 shows the symmetrical distribution of the digital signals among several DACs on analog cards symbolically.

[9] Enclosure Inpac 6 HE 84 TE, 10828-068, Pentair Schroff

There are total 12 a-c type female connectors (64-pins)[10] and 6 z-d type female connectors (15-pins) [11] installed at the back of back-plane. Two a-c connectors are used to provide the link to the SoC-FPGA adapter while remaining are used to provide the electrical connection to the analog cards. All the z-d type connectors have been used to mount power supplies units. The analog power supplies (43V,2.5Vand Auxiliary PS) are mounted in left side, while the digital power supply unit (see Sec. 39) is installed in right side.The digital isolators that provide electromagnetic immunity to all the digital signal originating from SoC-FPGA and directed to DAC are mounted at the top plane of backplane-PCB, therefore while installation into housing back of PCB faces front so that analog cards, power supplies, and SoC-FPGA can be mounted. The front side contains the circuit that regulated the mains power supply ($\sim$230 V).

The diagram shown (see Fig. C.21) and the tabulated info (see Tab. C.12) are symbolic representation of digital signal distribution at backplane. Both represent the same idea, but the immediate comparison might appear misleading as in graphic representation DIN refers to data input line for analog channels while Chip-Select line (CS) is control line for the respective group of analog channels. In the tabular representation array of the digital line stands for data lines and individual data lines are the counterpart of CS. All the digital line are similar in nature before reaching to I/O buffers inside the SoC-FPGA so specific data lines are assigned for controlling the data and called as CS lines from the FPGA perspective but from the standpoint of analog card design CS is the control line, and data line are lines that carry data from SoC-FPGA . The symbolic representation is digital line distribution from the analog cards perspective while tabular has attributes from the SoC-FPGA side. As said earlier (see Sec. 4.2.3), group of four analog channels is controlled by single CS line nevertheless in graphic DIN represent the data line, and CS is required CS line. While tabular number indicates actual digital channels numbers which are used as the data line and CS respectively. First 50 digital lines from each of 64-bits output bus of M00 and M01 digital machines (discussed in earlier sections) inclusively summed to reach the requisite number of 100 lines to control all DACs. It contains 10 a-c female connector[10] to support five analog cards. Beside analog cards, Five power supplies boards are always active while one is occasionally used. These boards are hooked into respective slots through 15-pole z-d connector[11] (see Fig. C.4).

The digital-signals of FPGA are digitally isolated from itself using digital isolator of type HCPL-90xx [12]. The quad HCPL-09xx CMOS are the digital isolators which have high speed and very low pulse width distortion (2 ns (max)). Since, our system is optimized for $\sim$70 MHz

[10] DIN41612f64acl3 Bürkin:52F7046
[11] DIN41612-H15 Bürkin:54F1470
[12] HCPL-900J-000E

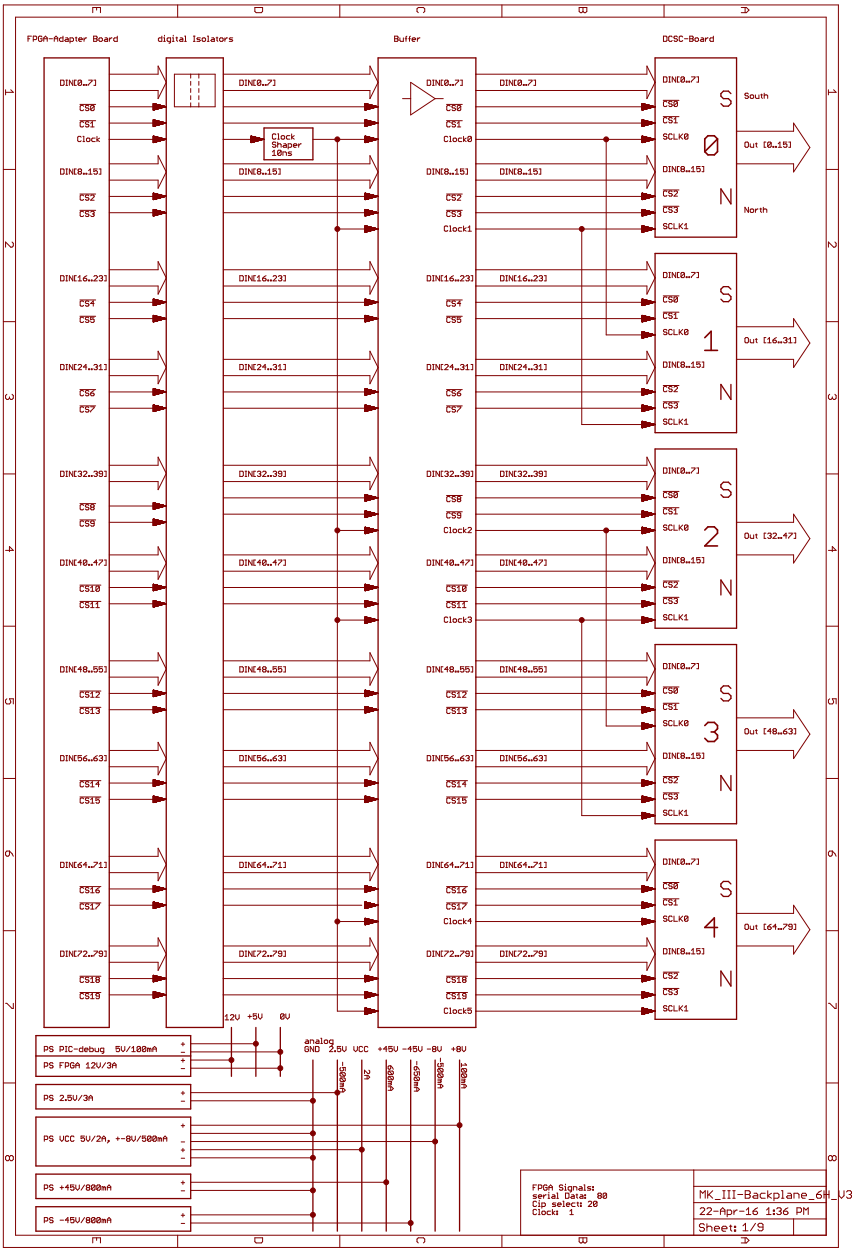


Fig. C.21 The planned digital signal and power supply distribution overlay across the backplane. This shows how the initial blue print of the backplane and its re-distribution of the digital signal through multiple analog cards.

clock (operating at 50 MHz,20 ns), this means pulse distortion is less than 10%. These digital isolators provide galvanic isolation between the digital section of the FPGA and analog section of N_Bertha. This isolation is of immense use as in the lab environment it helps to maintain the

FPGA data input lines (DIN)	Channel group	Slot number	Position from right
DIN[0:7], DIN[8], DIN[9]	South	0	1st
DIN[10:17], DIN[18], DIN[19]	North	0	1st
DIN[20:27], DIN[28], DIN[29]	South	1	2nd
DIN[30:37], DIN[38], DIN[39]	North	1	2nd
DIN[40:47], DIN[48], DIN[49]	South	2	3rd
DIN[50:57], DIN[58], DIN[59]	North	2	3rd
DIN[60:67], DIN[68], DIN[69]	South	3	4rd
DIN[70:77], DIN[78], DIN[79]	North	3	4rd
- DIN[80:87], DIN[88], DIN[89]	South	4	5th
DIN[90:97], DIN[98], DIN[99]	North	4	5th

Table C.12 Digital lines distribution across the back-plane. Position of analog card slot is indicted in fourth column (from right, i.e starting from SoC-FPGA position). The backplane contains total of 101 digital lines, out of which 100 are for data lines (DIN array) and Chip select (individual DIN) and 1 line for Clock. North and South are the group of distribution channels as discussed in section (see Sec. C.2).

integrity of trap DC-electrode by checking the inflow of any unwanted white noise caused due to several TTL pulses which are being used to control laser pulse. The input/output capacitance of these isolators is ~1.1 pF. These isolated signals are buffered through octal buffer/line drive to maintain signal integrity on longer transmission line up 500 mm. The propagation delay of these octal buffers varies from 2 ns to 4 ns (max). These octal drivers can deliver current up to 50 mA. The termination of these digital signals has been made at the end of analog cards to avoid the back reflection of incoming stronger digital signals.

Clock distribution

Simultaneous, rise and fall of clock and data at the input of DAC might lead to ambiguous output, and this happens as embedded circuits in DAC fails to resolve the data status (high or low). Hence, latches fail to register the incoming data at the rising edge of the clock, hence output is compromised. To avoid this, we may need to adjust or shift the clock cycle in order of few ns scale. So for adjusting the delay, there is special circuitry which adds delay to clock-lines. The digital clock from FPGA also passes through digital-isolator. Then, a derived delayed clock is generated using IC-40A[13]. Either reference or delayed clock can be selected using jumper (JP1), which is forwarded to clock drivers (IC-42 and IC-43). Each of these clock driver (IC42[14] and IC43[15]) generate five copies of clock which is then routed to the respective

[13] 74ACT74D
[14] CDC328A
[15] 14

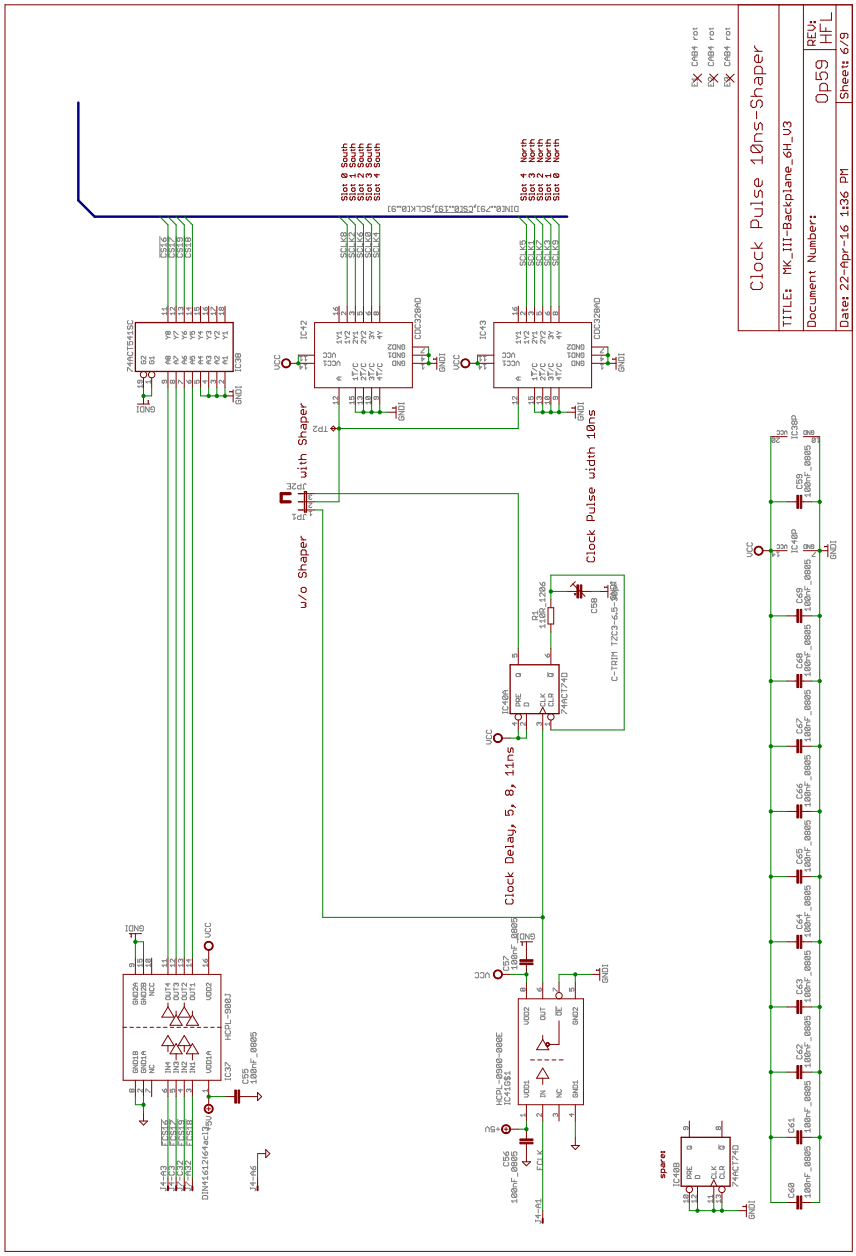


Fig. C.22 Circuit diagram for adding delay to the clock pulses for programming DACs in the analog module.

analog card slots. IC42 generates and distributes clocks to north channels and IC43 does same for south. The schematic is shown in Fig. C.22

The use of hardware delay selection is optional and can be selected (if needed) for programming DAC channels. It can be selected via jumper JP1 on the back-plane. Selection JP1-2 shorts the delay circuit, so there is no delay however subsequent selection adds a delay of 10 ns and 20 ns delay. The main control over signals and clock are achieved via the FPGA timing calibration in Xilinx design constraint file. For the forwarding Clock from FPGA to the backplane, a Output DDR primitive (ODDR) module has been used in the design. It is a useful and very elegant approach to forward the clock signal as it adds clock driver inside FPGA . This ODDR based approach is generally useful for streaming data and clock(s) as well from FPGA with necessary delay.

Power supply units

There are four linearly regulated power supplies and one switch mode power unit in this design. The SMPS units are used for the powering SoC-FPGA while for driving the analog cards linear power units are in place. We have avoided the idea of powering the analog section by SMPS type units as the SoC-FPGA itself is a significant source of noise in the high-frequency spectrum due to continuous switching of numerous digital logic. So installation of SMPS unit of 12 V/40 W on the extreme right section of the N_Bertha shielded box shall not impact the overall performance of all the DACs as all the analog boards are situated on the left part of the device. The presence of SoC is unavoidable as this is the heart of the system and hence essentially needed to derive the analog and digital section. So the use of SMPS unit to drive SoC-FPGA has been thought as the available space required was very small. Also, spectrum analysis of analog channels in broadband of 100 kHz to 100 MHz with and without SoC-FPGA SMPS does not reflect any noticeable difference. Therefore, the use of SMPS did have no impact on the signal quality of our analog channel.

The low noise is one of the essential requirement for the analog section, hence use of any SMPS units for the analog section has been completely avoided. All the linear power units are custom designed by mounting toroids transformer on the PCB. Low mechanical hum, availability of flexible dimension for mounting on PCB, the low energy requirement for maintaining the output voltage, and less stray magnetic fields are some natural advantages of using toroids transform. There are two units of 43 V/1 A, one 2.5 V/3 A, one auxiliary unit for 5 V/2 A TTL, +30 V/500 mA and -8 V/500 mA toroids transformer based power supply used for N_Bertha.

Linearly regulated : 43V/1A power supply

This linear power supply is a rather simple design. The toroid transformer's TR1 [16] secondary voltage is rectified by the bridge rectifier D3 (B125R) and filtered by C9 and C10 (1000 uF). A toroid transformer exhibits a much lower magnetic stray field than a standard transformer with M-, E- or U-core. The capacitors C3, C4, C7 and C8 (100 nF) (see Fig. C.23) prevent RF-noise caused by the reverse recovery of the rectifier diodes.
The voltage regulator IC2 (LM723) consists of a 7 V reference voltage source and an operational amplifier stage. It is powered by a voltage which is held constant by a 15 V-Zener-Diode D2 (BZX79-15), thus reducing the influence of the raw DC voltage hum. The output stage is a cascade with transistor Q2 (BC140) and R2. Q2 makes the connection between the low voltage regulator (15 V) and the "high" raw voltage (+67 V) and prevents the regulator IC from heating up.
Q2 does have a collector-emitter breakdown voltage of 80 V so that it can withstand the 67 V DC raw voltage. Q1 (TIP102) is a Darlington-transistor with high current amplification. This power supply uses sense lines to minimize voltage drops caused by contact resistance. When it is used without sense lines, resistors R4 (22 Ω) and R14 (22 Ω) will limit the increase of output voltage to 100 mV. Transistor T1 (BC107) together with shunt resistor R15 (0.56 Ω) work as a current limiter. Transistor T1's collector pulls the output voltage down when the current through R15 exceeds 1 A.

Linearly regulated : 2.5 V/500 mA power supply

This power supply can act as a source and sink as well, for the current up to 3 A maintaining constant voltage at 2.5 V (see Fig. C.23). The secondary windings of transformer TR1[17] and half of the rectifier bridge D1[18] make a two-way rectification. The "high" transformer impedance will limit the peak charge current and its stray magnetic field. There is only one diode forward current voltage drop. The three capacitors C1, C2 and C3 (4700 µF) filter the raw voltage. IC2 [19] works as a precision 2.5 V Zener-diode. IC3 [20], a rail-to-rail operational amplifier with up to 50 mA output current, together with the complementary transistor pair T1 [21] and T2 [22] buffer the 2.5 V within a ±2.5 A current range. The use of sense lines reduces the

[16] Hammond 1182J22
[17] Talema 20610-P1S02
[18] B40C5000
[19] TL431
[20] AD8041
[21] BD243
[22] BD244

sensibility for contact resistance changes (or wire resistance).

Linearly regulated : Auxiliary power supply

This 280 mm long PCB board contains three power sources.

1. **5 V/2 A TTL:** This power source is used to power the Optical Isolators and TTL-buffers of the backplane's analog area, TTL ICs and the DACs digital part.
2. **8 V/500 mA:** This power source is down-regulated to -5V on analog cards and powers the intermediate OpAmp and two +2.5 V_{ref} buffers.
3. **30 V/500 mA:** This raw power source is used to generate stabilized +24 V and V_{DD} voltages on each of the analog cards. TTL of 5 V and -8 V are low drops out (LDO) designs, which means that the input voltage can almost be as low as the output voltage. Utilizing separate power sources for output amplifiers enables the user to get a summed up output power of 40 W or 1 A from analog cards.

Switch mode power supply: 12 V/40 W

This power unit is commercially available in the market[23]. Pin assignment, alignment, and connector of this unit have been considered in prior at the time of design all the units. Hence, it was ready to use the module for us. It is a 51 W (12 V, I_{max}=4.2 A) switch mode power supply (SMPS), that is used to power the SoC-FPGA . SoC-FPGA needs 12 V and at $\sim$2 A current for driving all its digital pins. Remaining power is used for driving the amplifier circuit of the digital outputs.

Digital output for pulse control

It is a simple common emitter circuit. The hex inverter buffers/driver's input can be powered with on-board 3.3/5 V, making it fully compatible to used with SoC-FPGA , where the TTL output voltage is 3.3 V. Therefore, it is being used as translator hence enabling the SoC-FPGA output to drive loads without actually loading it.

The schematic (see Fig. C.24a) shows one the channel among available 24-digital channels. Rest of the channels are an identical copy of this circuit, while Fig. C.24b is schematic of the input port. In standard design of N_Bertha , there is only one input port, and it is used

[23] SEK112 type, 13100-044

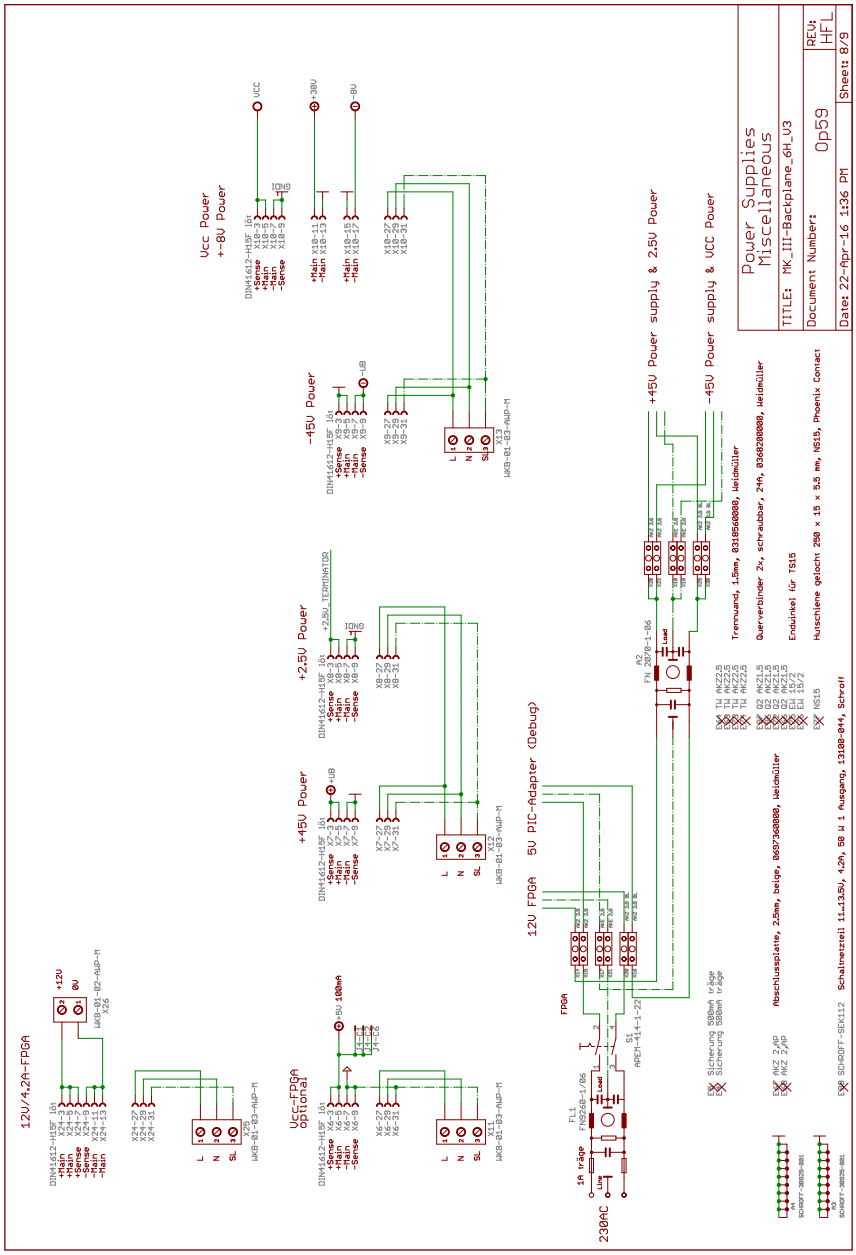
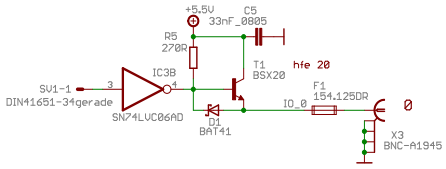


Fig. C.23 Different power supply units and their pin configuration N_Bertha

to trigger this device externally. However, for scalable master-slave units (see Sec. D.21) where more than one input port is needed at the front plate, this design should be copied while designing the PCB, although output port can be rewired as input port later as well. The open collector buffer is powered by an onboard mounted 3.3 V switch mode DC/DC power supply,

The input of hex buffer (SN1-1) [24] (Fig. C.24a) is the TTL output signal from SoC-FPGA which are lines in the digital section of N_Bertha . It is providing time-dependent TTL signals which can be used to trigger high impedance load (50 Ω compatible also). The duration for time-dependent trigger can be set in the software that is passed to N_Bertha in term of the binary data structure.

(a) Circuit diagram of common emitter for driving 50 Ω loads



(b) Circuit diagram for high impedance load for buffering the input signal to the SoC-FPGA logic

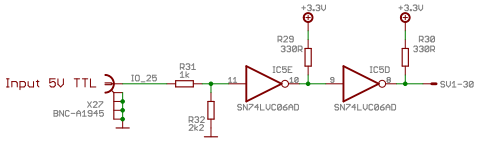


Fig. C.24 Circuit diagram for digital channels

which itself is powered from the power supply (see Sec. 39) which is used to power SoC-FPGA .

R27 (270 Ω) is the load resistor at the collector of the buffer's output transistor. The NPN transistor T23[25] acts as a current amplifier and can feed the load with 100 mA at 5 V. As 5.5 V onboard switch mode power supply unit can deliver up to 3 A therefore, in principle 30-digital line can be simultaneously used to drive 50 Ω load. There are on-board installed special fuses[26] that prevent the transistor from short-circuiting in case if the output shorted for unknown reasons. New fuses can replace these fuses. When the TTL-buffer output transistor turns on, the output is pulled low via the Schottky Diode D23[27]. The inclusion of the resistor R31 (1 kΩ) protects the input of IC5E from ESD discharges.

Analog-cards

The development of multichannel analog cards followed by the SoC-FPGA digital architecture was the next challenging task in the hierarchy level. The diagram shows (see Fig. C.25) the planned on-board distribution of the digital lines for data and control signal CS. In this diagram, each of the rectangular blocks represents a DAC[3], that has an analog voltage range of [0, 2.5] V. Then, it is followed by two-stage amplification, and first stage enhances the voltage by eight times raising the new-level to [0, 20] V and second stage has gain factor of four times, final

[25] BSX20
[26] OMNI-BLOK, fast, 125mA
[27] BAT41

gain 32 times, i.e the voltage range of [0, 80] V. But due to the presence of a negative voltage offset -13.33 V, the final output voltage is adjusted to [-40, 40] V. The design is replicated multiple times sharing some common digital lines. It builds-up 80-channel analog device. Second stage amplification has been not shown in some case of the diagram (Fig. C.25), for avoiding congestion.

Four DACs are grouped to form a single Bank, that is controlled by one control CS line. In this diagram, two such symmetrical groups represents the presence of eight analog channels grouped in top side (known as north bundled channels or north channels) of the analog card. The last two blocks followed by the broken shaded lines represent similar two groups of DACs, and they are located on the bottom side (known as south grouped channels or south channels) of the cards. These are same north and south group that has been indicted in section.C.2. The shaded line represents the continuation of the identical circuit has been used above. The exact representation is missing to avoid congestion due to limited space. Altogether these DACs on the analog cards are simultaneously updated using their respective control signal and hence function as 16 channel voltage sources.

As described earlier (see Sec. C.4), that digital clock line from SoC-FPGA is received to the buffered clock driver. Two of these clock buffering units together buffers ten clock signals. Each of the analog cards needs two of these clock line to feed their north and south grouped channels. For programming these DAC, we use only three digital lines that includes data lines for data, clock line for clock, CS line for chip select or control. However, there is a load line $\overline{LDAC}$ (see Fig. C.31) which can be used to update the DACs with the registered inputs. When this signal is set to active-low it updates the DAC output, so all the load lines are connected to GND (set to low) so that as soon as all DAC are registered with all 16-bit inputs data, DACs update immediately. In this way, we can relatively speed up the DAC update saving one digital line per channel.

This way we can continuously update DAC at 360 ns (16 clock cycles for the data (20x16=320 ns) and 20 ns for setting the $\overline{CS}$ to low before data incoming and 20 ns for setting it high for enabling the output of DAC) when the clock is running at 50 MHz. The digital lines are precious resources in our design. Therefore, we have decided to not use this load signal ($\overline{LDAC}$). Also, the importance of the single digital line can be used from the fact that an analog voltage channel can be used to program it. All the digital line have been optimized meticulously in term of number of analog channels that can be programmed using these lines.

The layout of the DAC distribution on the analog card, amplification stages in the circuit for DACs, fine timing details DAC programming (see Sec. 56) have been discussed in the

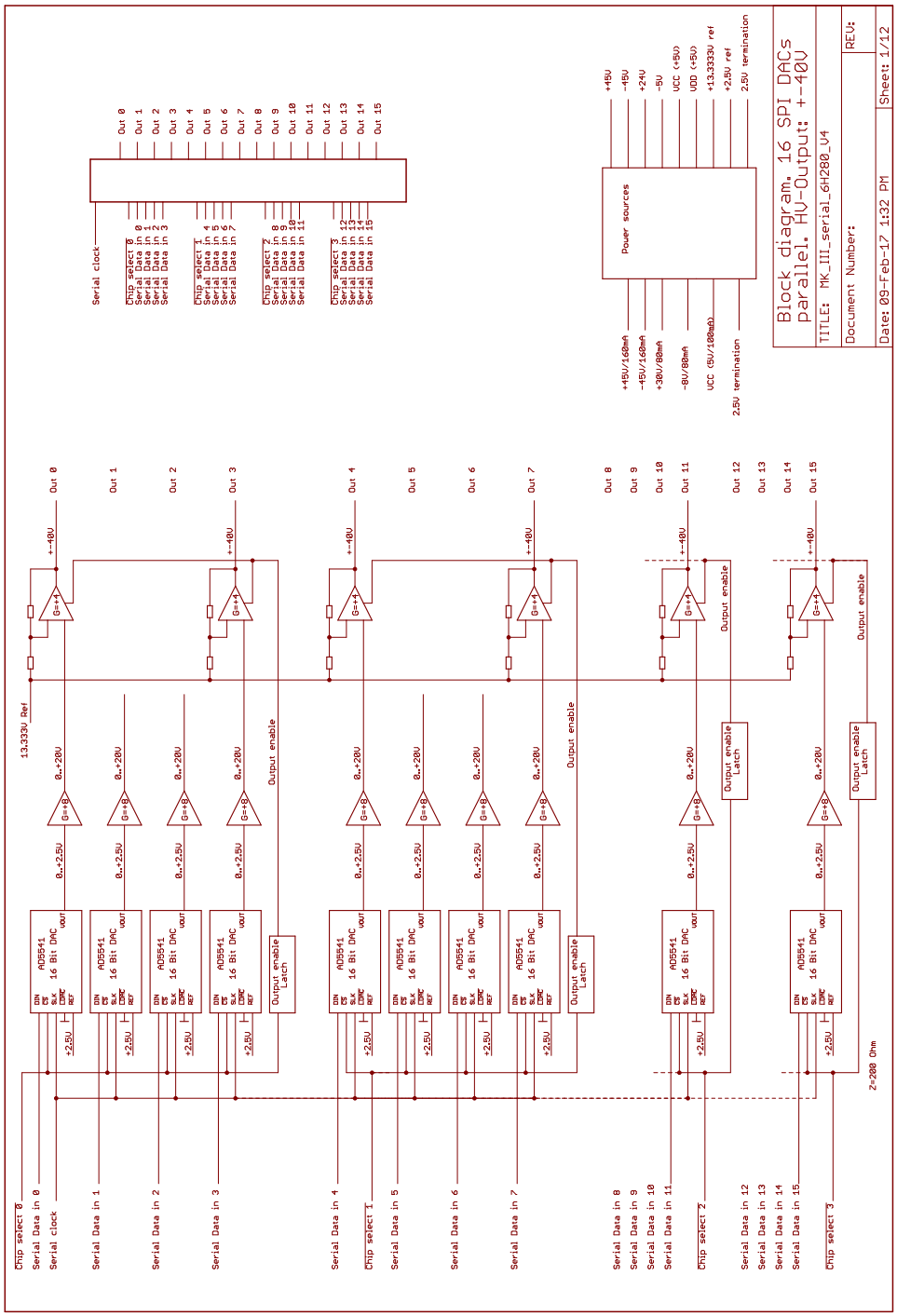


Fig. C.25 Design overview of the multichannel analog cards at block-level (symbol)

upcoming parts.

Besides the programming line, the power supply line necessary for powering the DAC is also shown symbolically (see Fig. C.25). It shows control line (CS) and data line (DIN), clock(CLK) and the output data, needed for the standard SPI based parallel programming of all DAC analog cards.

Layout of digital line distribution in analog card

The circuit diagram for the digital lines and its termination has been shown in Fig. C.26. The transmission-line type signal propagation design has been adopted to reduce the overall power loss in transmission. The backplane is congested with numerous the digital line. So, it is crucial for us to minimize any unwanted power consumption. Also, we should keep in mind that behavior of the electrical components deteriorates with rising temperature. So, these electrical power losses should be minimum by optimizing the characteristic impedance of each of the digital lines.

Programming of the DAC[3] is done via SPI. Each of the DACs on the analog cards does have its dedicated serial data line (For example for Card0: Channel_0: DIN0, Channel_1: DIN1 and so on up to Channel_15: DIN15). As the transmission line impedance is ~96 Ω which are terminated by 180 Ω (R1 and R16)resistor at the end. The long-running copper wire trace of approx. 400 mm in length and diameter (0.035 mm) constitute 0.8 Ω which partially compensate the mismatch in the exact impedance matching by reduces the back reflection of digital signals along the wire. The worst case calculation of the back reflection on the data lines at 2.5 V is 13.9 mA that means a total of 80x13.9 mA=1.1 A, the sink of octal buffers driving these lines can sink this current.

As each line of the octal buffer driver[28] can act as a sink or source up to 50 mA, hence the digital error caused due to back-reflection these high-frequency digital signals can be handled. Four $\overline{CS}$ lines are used to control four banks (each of DACS) in a multichannel analog card as explained in the start of this sections. Although 100 Ω terminates all the four $\overline{CS}$ and two clocks (CLK) lines resistors, based on the similar calculation limit of the required current sink is 25 mA. Therefore, their back-reflection is also compensated well using these hex buffers.

[28] 74ACT541SC

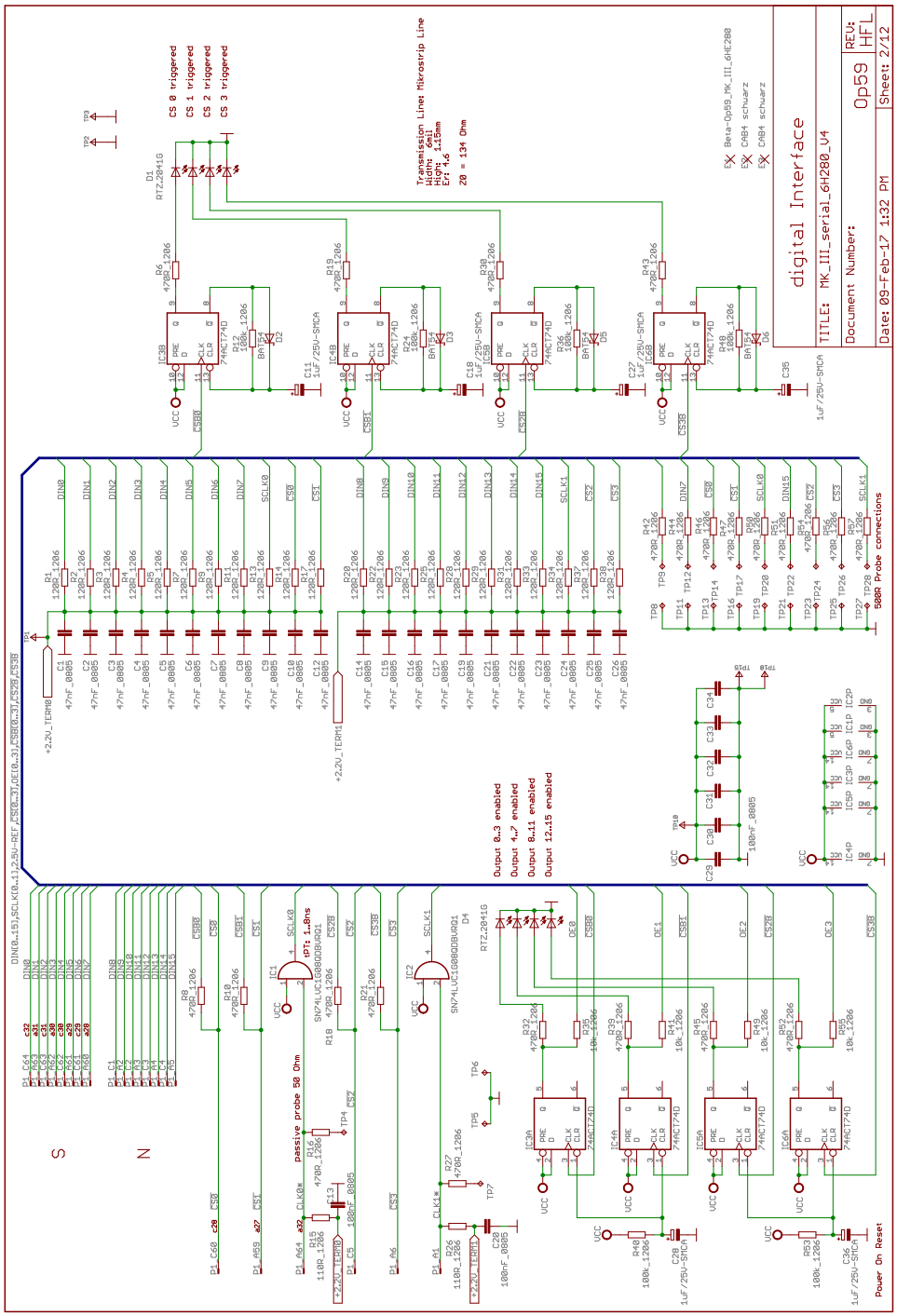


Fig. C.26 Schematic for the several digital line arriving from SoC-FPGA and their on-board termination in analog cards.

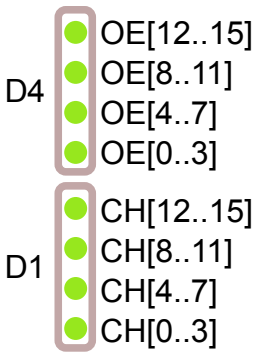


Fig. C.27 Channel representation of LED D1 and D4. This representation can be associated with Fig.D.18 as they are directly related. In channel notation small 'h' in this Fig. D.18 and capital 'H' shall not be seen differently as they represent same. Difference in alphabets are due to their convention in hardware ('H') and software ('h') side.

There are four modules of D-flip flop (DFF) [29] that have been placed intentionally at the front edge of the analog card PCB, near the LEDs which lights ups once these CS are set to high. The presence of the LEDs is to provide the visual status-display of the internal control lines of the DAC ($\overline{CS}$) and -status of the multiple power lines on the cards. There is a total of 10 LEDs in each analog card. 8 (D1 and D4, an array of 4 LEDs) out 10 LEDs are installed at the front panel while two LEDs (LED1 and LED2) are installed onboard. LED1 and LED2[30] are forward biased to display the onboard status of +45 V and -45 V availability respectively. D4[31] is intended to display the status of output that means the specific channel is enabled to set or reset the DACs. LED-array (D1) informs the triggering of the control line (CS) of the DAC which provides visual realization of DAC setting to newer value. The first LED array (top-down in sequence of D4) is an output enable for the channels controlled by first LED of D1 in the same sequence. It is now repeated for the rest of the LEDs in the series (see Fig. C.27). The default state of the control line ($\overline{CS}$)is active-high (output disabled). The DFF of the respective unit provides 20 mA for driving these LEDs. However, to avoid the spurious misinterpretation from these LEDs (D1) after power on, these are disabled by DFF . The other on-boards DFF are IC3A, IC4A, IC5A, and IC6A.

Therefore, hot-plugging the analog card or restarting N_Bertha , the LED1, LED2 and D4 LEDs light up, which displays that the boards have initialized with correct internal state. D1 remains off as the output of all the DACs are disabled at power on. This is however passed to user control or SoC-FPGA controlled as soon as the user wants to program it. The chip select

[29] IC3A and others: 74ACT74D type
[30] LED1 or LED2: I-LED934 type
[31] D1 or D4: RTZ.2041R MENTOR type

trigger keeps the LEDs (D1) lighted for ~1 ms, this enables the user to notice if writing into DAC is successful.

First stage amplification

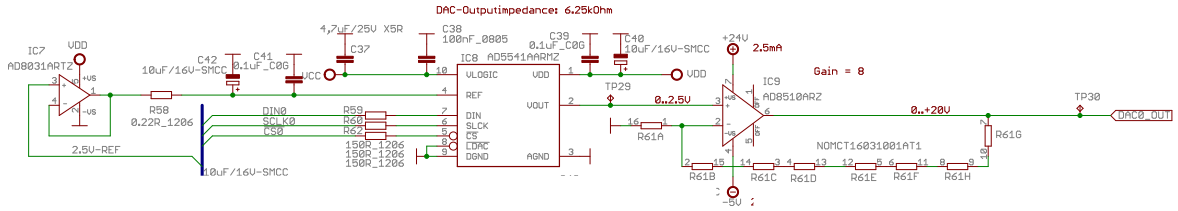


Fig. C.28 Eagle schematic of stage: 1 amplification using OpAmp IC9 , and resister array R61 (for channel: 1). This non-inverting amplification provides gain of 8, that outputs voltage range of [0..20] V

The circuit diagram (see Fig. C.28) shows the 16 bit serial DAC [32] and OpAmp IC9[33] amplifier with gain resistance (R61[34]). This OP-Amp amplifier with gain resistance (R61) amplify the voltage range from [0, 2.5] V to [0, 20] V, providing a gain of 8.

According to data-sheet [Dev18], it has very low noise spectral density of $11.8\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, fast settling time of 1 µs, low GIA of $1.1\,\mathrm{nV}-\mathrm{s}$ and other significant figures. Apart from these important low characteristic, it is available in 10-lead MSOP packaging, that provides still access to debug or modify in case of design error or malfunctioning. The measurement values from data-sheet are for reference as we need to measure these value in our design which has several other design elements that can affect these values. However, a more realistic approach that includes the presence of all the electronics, design implementation, overall performance has been discussed in Sec. 56.

The DAC output function is

$$V_{out} = \frac{V_{ref} \times DIP}{2^N}, \quad Where\ N = 16 \tag{C.1}$$

For V_{ref}=2.5V, the mid-scale load (digital input code (DIC)=0x8FFF_h) and full scale load (DIC = 0xFFFF_h) will provide V_{out}=1.25 and V_{out}=2.5, respectively. The amplification gain at the first stage is gained by using R61 series resistors and OpAmp, IC9. An OpAmp based

[32] Dev18.
[33] AD8510ARZ
[34] NOMCT16031001AT1

non-inverting amplifier has been implemented that governs the final amplification at the first stage by

$$V_{out}^{stage^1} = (\frac{R61A + R61B + R61C + R61D + R61E + R61F + R61g + R61H}{R61A} + 1) \times V_{in} \quad \text{(C.2)}$$

Where R61x (x=A,B,..H) are same resistances of IC (R61) packages. R61 is resistance array package with 8 precision resistances (1 kΩ) that has excellent long term stability ratio (ΔR±0.015). Due to its 16-SOIC type packaging, design errors are easy to debug and if needed replacement can also be done without affecting the other on-board component. The voltage ranges is [0..20] V at the end of this stage. IC9 used at this stage of amplification is a low noise and wide bandwidth JFET OpAmp[35]. It has also low total harmonic distortion (THD) (~0.0005% of total distortion when configured in positive unity gain (the worst case) and driving a 100 kΩ load), excellent gain linearity, settling time of 0.5 to 1 µs (0.9 µs with in 0.01% in step of 0 to 10 V), low noise spectrum density of $8\,\mathrm{nV}/\sqrt{\mathrm{HZ}}$. It is available in SOIC package and prior experience of using this OpAmp in old design were some reason for choosing this amplifier.

The amplification gain can be reduced to enhance the slew rate as we will see in next section that this board can be easily tuned to provide the final voltage range of ±20 instead of ±40.The series resisters (R45 for DIN, R46 for CLK) along with the input capacitance on the digital line, act as low pass that decrease the rise and fall time of the digital signals by 1 ns. VLOGIC is the logic power supply that is buffered by ceramic capacitors C23 (4.7 µF) and C24 (100 nF) are low grade capacitance of type ceramic X5R and X7R respectively that reduce the digital ringing on the digital power line.

The reference input (at pin:4 V_{ref} see Fig. C.26) is buffered by the combination of C28 (10 µF) and C27 (100 nF). C28 is standard tantalum electrolytic while C27[36] is high quality ceramic multi-layer capacitor, that shots the high frequency component to GND. A careful investigation has revealed addition current spike on VDD and V_{ref} is generated whenever control signal (-CS) is set to high. This issue has been solved by installation of 16 additional 2000 µF electrolytic buffer to buffer VDD and V_{ref} (+2.5 V). This issue was resolved in the older version by usage of 16 additional buffer OpAmp for 13.33 V voltage reference. Please note that it's default state is active-high that disable the output from updating a voltage sample, and input digital value is registered into internal registers.

[35] Dev17.
[36] EIA: COG

second stage amplification

Properties	Amplification stage	
	stage:1	stage:2
OpAmp:	AD8510	LTC6090
Large Signal voltage Gain Vol:	107000	10000000
Gain Bandwidth Product (3 dB):	8 MHz	12 MHz
Slew rate:	20 V/μ s	21 V/μ s
Noise 1 kHz:	8 nV/$\sqrt{\text{Hz}}$	14 nV/$\sqrt{\text{Hz}}$
Total Harmonic Distortion:	0.0005%	0.001%
Gain:	8	4
BW:	1 MHz	3 MHz
Input:	0..+2.5 V	[0,10] V
Output:	0..+10 V	[-40,40] V

Table C.13 Specification of analog channels at first and second amplification stage.

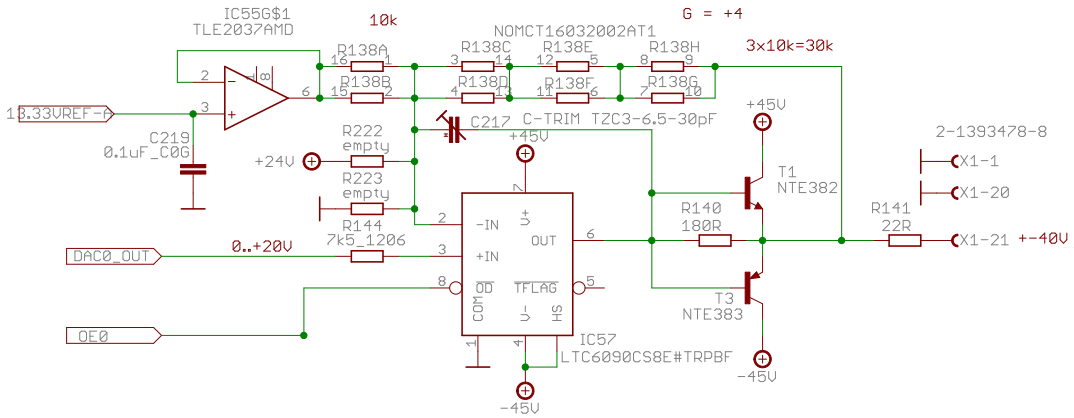


Fig. C.29 Eagle schematic of stage2 amplification using OpAmp IC57, and resister array R138.This non-inverting amplification provides gain of 4, that output voltage range of $\pm$40 V

The initial preset requirement for the voltage was set to $\pm$40V for the experimental requirements (discussed in Sec. 5.2.2), which means the essential gain factor for the amplification stage is (80 V)/(2.5 V) = 32 as full scale load of DAC outputs only voltage range of to [0, 2.5] V. This is achieved by dividing the amplification stage with gain of 8 first stage (discussed above) and 4 at second stage. In second stage choice for OpAmp was mainly based on the rail-to rail gain amplification, and available packaging that can be easily mounted and debugged.It may be run from a single 140 V or split $\pm$70 V power supplies and are capable of driving up to 200 pF of load capacitance and these are available in 8-lead SO package with exposed pad. This OpAmp (IC57) and resistor array (R138) provides requisite amplification gain of 4 for

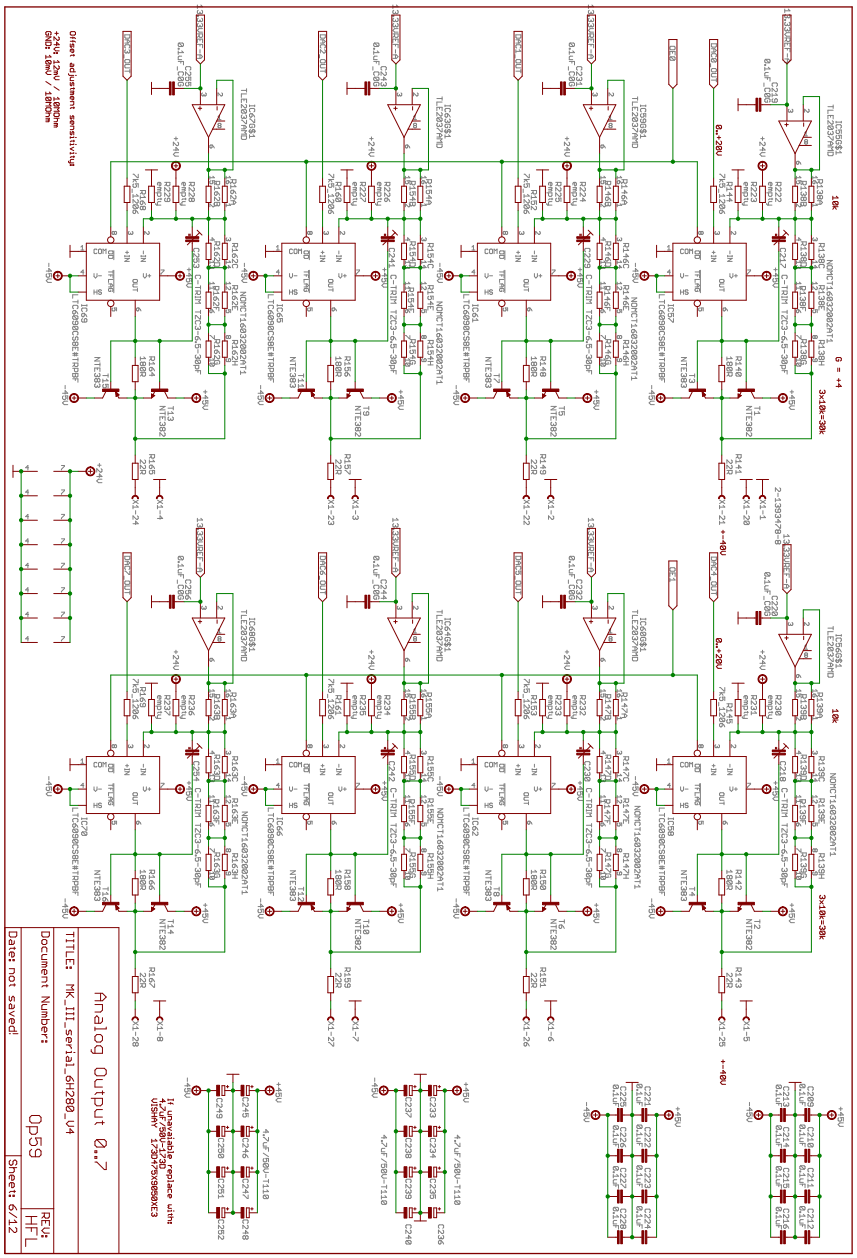


Fig. C.30 Schematic of 8 analog channels at stage:2 amplification, two output enable signal (OE0 and OE1) are dedicated to control these 8 analog channels. Each of these output enable signals are interconnected to group of 4 analog channels at $\overline{OD}$ (output disable: Pin 8) to control the second stage amplification output.

channel:1. Similar group of series resistance and OpAmp has been used for other channels.

Resister array are same precision resistor that is being used at the first stage.

Although single OpAmp amplifier LTC6090, that is used currently at second stage shall be sufficient to achieve the requisite gain factor (32). Nevertheless, in this design two stage amplification stages have been used.As the small signal bandwidth gain for single stage amplification configuration would be 12 MHz/32=37 kHz, where 12 MHz is the bandwidth gain of the LTC6090 amplifier and the resultant noise spectral at 1 kHz will be $33\times 14\,\mathrm{nV}/\sqrt{\mathrm{Hz}} = 462\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, while two stage amplification with the two different amplifier (AD8510A and LTC6090) are designed to provide the gain of 8 and 4 respectively has improved bandwidth and low noise. The bandwidth and voltage noise density (at 1 kHz) in the later case, where duo are designed together are 0.95 MHz (measured in simulation) and $\sqrt{(8\,\mathrm{nV}/\sqrt{\mathrm{Hz}}\times 9\times 4)^2+(14\,\mathrm{nV}/\sqrt{\mathrm{Hz}}\times 5)^2} = 262\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ respectively. In amplification circuit, if the noise spectrum is assumed as evenly distributed about 0 V then gain factor is (voltage gain+1). The AD8510 precision amplifier draws only 2.2 mA current, which results in the power dissipation of ~55 mW, while LTC6090 dissipates power of ~340 mW at 0 V output, which is another factor why selection of the single stage amplification with faster OpAmp has not been taken as the first choice. The reduced power dissipation contributes in maintaining the long term stable behavior of the electronic components, which finally improves the thermal noise of the electronic components.

This configuration improves the bandwidth gain twice while reducing the noise by half. Therefore, it reduces the temperature drift during the DAC output. However, an inclusion of third stage would have been even better in term of overall performance, but then we have to establish a trade off between the available on board resources while design the PCBs. And in the current design there was not enough space to design anymore stage for the amplifications.

The resistor R99 (7.5 kΩ) is added for a low pass, to keep the AC-linearity of the system above 1 kHz, it shall not be confused as an requirement for the design to provide input bias current (pA for LTC6090) as needed for bipolar OpAmp.

A complementary addition push-pull circuit at output stage using T1[37] and T2[38], to help IC41 (LTC6090) for delivering additional current requirements in the worst case. However, upto ±2.5 mA the current is delivered by IC41 through the 180 kΩ resistance. The load shall not be be drawing more than this limit nevertheless if it happens this additional complimentary

[37] transistor NPN type NTE382
[38] transistor PNP type NTE383

circuit can ease the supply upto 100 mA, however it is not recommended. Trim capacitor (C191)[39] shall be adjusted for fast response with no overshoot with a ±5 V square wave. The OpAmp IC39 (TLE2037) works as a buffer for the offset reference voltage V_{ref}=13.333 V. There are two such adjustable buffers available on the boards where each is dedicated for north and south group of channels.

The latest handling report from several user physicists is rather disappointing, it seems a very low impedance is connected at the load which causes reckless demand of current up-to amperes. In such case either of the two fuses installed on the boards will be blown to save the output transistors or the OpAmp (IC41) itself will short circuit. If electrical short is still not resolved it burns the fuse, output transistors, then IC41. Many users complain about design issue which is incorrect as in Microlab of Uni-Mainz, these cards are running for more than two years without even single such instance. Such reported case from other labs so far can be considered as mishandling issue against the preferred way of operation.

Programming the DACs

The digital lines generated from SoC-FPGA has to be precisely controlled at the input of the DACs for precise and successful update of voltage at the output channel. The timing requirements (see Fig. C.31) between the control ($\overline{CS}$) and data line (DIN) feeds into the DACs has to be delayed or adjusted strictly to the timing relation recommended in the data-sheet. Any mismatch among the input digital lines will lead to wrong voltage output at the DAC output. Therefore, individual input lines ($\overline{CS}$) and data-line (DIN) has to individually checked and adjusted well within the mentioned limit with respect to the clock for a reliable and successful programming of DACs. There is single clock line and four DACs has to be controlled by one control line ($\overline{CS}$), these two condition act against each other and provide us very small window for adjusting these lines (for eg. DIN[0..3], CS0, CLK). The only reliable way is to adjust the delay on these line is to monitor the incoming digital signal manually and define the measured delay in design constraint files (in embedded development software Vivado) and hope that it should work for another similar unit of N_Bertha , which may or may not be true. In case if this delay constraint fails to work for other design, one has to use the ground rule by individually monitoring the delay and setting it to constraint file to regenerate newer SoC-FPGA program for that specific unit. This is tiresome work to do, nevertheless due to very sound and precise digital electronic development, shift in the working delay values once set has not been observed so far.

[39] TZC-6.5-30 pF

AD5541A

TIMING CHARACTERISTICS

V_{DD} = 5 V, 2.5 V ≤ V_{REF} ≤ V_{DD}, V_{INH} = 90% of V_{LOGIC}, V_{INL} = 10% of V_{LOGIC}, AGND = DGND = 0 V, –40°C < T_A < +105°C, unless otherwise noted.

Table 4.

Parameter[1,2]	Limit at 1.8 ≤ V_{LOGIC} ≤ 2.7 V	Limit at 2.7 V ≤ V_{LOGIC} ≤ 5.5 V	Unit	Description
f_{SCLK}	14	50	MHz max	SCLK cycle frequency
t_1	70	20	ns min	SCLK cycle time
t_2	35	10	ns min	SCLK high time
t_3	35	10	ns min	SCLK low time
t_4	5	5	ns min	$\overline{CS}$ low to SCLK high setup
t_5	5	5	ns min	$\overline{CS}$ high to SCLK high setup
t_6	5	5	ns min	SCLK high to $\overline{CS}$ low hold time
t_7	10	5	ns min	SCLK high to $\overline{CS}$ high hold time
t_8	35	10	ns min	Data setup time
t_9	5	4	ns min	Data hold time (V_{INH} = 90% of V_{DD}, V_{INL} = 10% of V_{DD})
t_9	5	5	ns min	Data hold time (V_{INH} = 3 V, V_{INL} = 0 V)
t_{10}	20	20	ns min	$\overline{LDAC}$ pulse width
t_{11}	10	10	ns min	$\overline{CS}$ high to $\overline{LDAC}$ low setup
t_{12}	15	15	ns min	$\overline{CS}$ high time between active periods

[1] Guaranteed by design and characterization. Not production tested.
[2] All input signals are specified with $t_R = t_F$ = 1 ns/V and timed from a voltage level of (V_{INL} + V_{INH})/2.

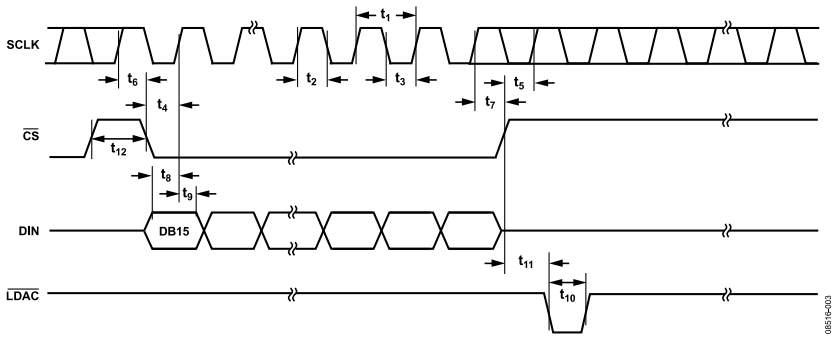


Figure 3. Timing Diagram

Fig. C.31 Time constraint of the digital input of DAC. It is important to maintain this specification for deterministic programming of any channel in any analog card.

The DAC located near backplane (south bank: 06,07 and north bank: 08,09) are not time critical. However, for farther DACs do show random requirement of delay-duration. Therefore, individual monitoring of each channel in every card are needed for setting their right delay.The different delay is due to uncorrelated behavior between two identical electronic components. For example in same test set delay needed for a DAC might differ from another identical DAC in order of *ns* scale and similar characteristic has been observed with other electronic component in this design. Therefore, we have decided to individually set the delay for each of the channels. The individual channels have been tested for the minimum and maximum delay, where each of the individual DAC registers fail to register correct incoming digital control inputs. And final delay has been selected at the intermediate position so that irrespective of the individual

N_Bertha units, all the channels shall be working. This approach has been very successful and so far we have not seen any exception to this, which irrespective of the NBertha unit any preprogrammed SoC board can be used with any arbitrary chosen analog card, and it shall be working (Fig. C.31). Multiple tests that has been running for months has been performed to test it.

Glitch on lower significant bits

Observed glitches

Ideally, a DAC output shall be smooth linear varying with digital input code (DIC). But reality this is not the case. Overshooting, undershooting, ringing behavior of the output signal are very well seen in all the DACs. Glitch is also kind overshooting or undershooting behavior of the DAC output, which happen at every update of the analog signal. Glitches are caused to uneven switching of analog output switches which are faster on timescale than others or in some case the capacities coupling between digital input and analog output has also causes significant glitch. The IEEE STD 181 defines glitch as a “transient that leaves an initial state, enters the boundaries of another state for duration less than duration for state occurrence and returning to the initial state." Glitch impulse is measured in term of energy which is commonly specified as nano-Volts-sec (nV-s) , called as GIA. For the analog update with larger amplitude it is insignificant but for smaller amplitude it becomes significant against the programmed voltage.

It is very significant at major-carry transition, which happens when the maximum number of the bits changes it state i.e. from ’0’ to ’1’ or vice versa. Major-carry transition is transition of single bit transition (LSB) which leads to change of MSB bit. Although glitch are available for DACs at all the transition but as said it is maximum at transition of 0x8000_h (1000000000000000_b) to 0x7FFF_h (0111111111111111_b) or vice-versa. Nevertheless, glitches are available at all possible transition but their amplitude is small in general making it insignificant against the available noise in the signal. While, in some case there is significant amplitude of glitch at lower LSBs as well. Currently all of used DAC are showing glitches with significant impulse are at specific lower bits as well.

For measuring the GIA (see Fig. 4.12a and Fig. 4.12b), MSOX3104A and a differential probe from Agilent has been used. The mains power line power the isolation transformer, which then power the oscilloscope and N_Bertha. The length of differential probe is approx. 0.5 m which load the DAC with $300\,\mathrm{k}\Omega$ at time scale of glitch signal (0.5-1 MHz). Differential

probe has been used in order to avoid any common noise source.

Generally, glitch at lower significant bits are not insignificant against the noise floor of the signal. But in this DAC we have observed significant GIA at special combination of lower bits. This shall not be there in DACs, so we can assume that there is problem with this DAC. We have also tried to contact Analog Devices but received no feed back so far. But low pass filter used at feed-through of the trap flange (discussed in next section) smooth-en it and hence eliminating the chance of kicking the trapped ion during execution of the experimental sequence. Fig. 4.12a shows the dips during execution of sinus signal on all the channels simultaneously. We have figured out the exact combination of the DIC to establish this fact. As we started driving the

Table C.14 Observed glitches at lesser significant bits

serial number	DIC	Hex code	decimal value	DIC difference
0	1000 0100 0111 1100	847C	33916	
1	1000 0100 0101 1010	845A	33882	-34
2	1000 0100 0011 0111	8437	33847	-35
3	**1000 0100 0001 0101**	**8415**	**33813**	**-34**
4	**1000 0011 1111 0011**	**83F3**	**33779**	**-34**
5	1000 0011 1101 0001	83D1	33745	-34
6	1000 0011 1010 1110	83AE	33710	-35
7	1000 0011 1000 1100	838C	33676	-34
8	1000 0011 0110 1010	836A	33642	-34
9	1000 0011 0100 0111	8347	33607	-35
10	1000 0011 0010 0101	8325	33573	-34
11	**1000 0011 0000 0011**	**8303**	**33539**	**-34**
12	**1000 0010 1110 0001**	**82E1**	**33505**	**-34**
13	1000 0010 1011 1110	82BE	33470	-35
14	1000 0010 1001 1100	829C	33436	-34
15	1000 0010 0111 1010	827A	33402	-34
16	1000 0010 0101 0111	8257	33367	-35
17	1000 0010 0011 0101	8235	33333	-34
18	**1000 0010 0001 0011**	**8213**	**33299**	**-34**
19	**1000 0001 1111 0001**	**81F1**	**33265**	**-34**

DAC with sinus or multiple different kind of waveform with sufficient large samples, this problem of dips and bumps, or special glitches were better observed. Table:C.14 shows the analysis of binary code that has been programmed into DAC, and bold digital values are the value where these special glitches have been noticed. Since these data are taken on falling slope of a sinus signal so it shows bigger and smaller bumps, while on the rising signals bigger and smaller dips are seen in Fig. 4.12a. In Tab. C.14 at serial number 3 and 4, big bump has been

observed while SN: (11 and 12) sees small bumps similarly at SN: (18 and 19) another big bump has been observed. A very similar pattern as shown in figure Fig. 4.12b, but orientation changes. A very general bit pattern concluded so far is transition of bit position[7..4], change of DIC at this position from 0x..1110.... to 0x..0001.... or 0x..0000.... results in such special glitches. The bigger bump or dips has amplitude of $\sim$35 mV-40 mV PK-PK while the smaller has 13 mV PK-PK resulting GIA of $\sim$35 nV-s and $\sim$12.5 mV respectively.The further investigation of the DAC does reflect any other significant issue.

In conclusion, we have demonstrated that with the help of the latest digital programmable technology, a complete experimental control can be developed for any experiments. In analog section, we have tried to show how precise voltage source can be developed that can be updated in less than 400 ns. The current technological development presented in this chapter shows the success of our effort in designing a complete hardware solution to the scalable ion trap-system, which shall help in realizing a scalable quantum computing node for which we are aiming for.

D

External electrical wiring

In appendix: C, the underlying fundamental details of newly developed SoC-FPGA based low noise and precision arbitrary waveform generator (N_Bertha), that is intended to provide a complete experimental solution developed for scalable ion-traps have been discussed. Although, it has been designed to support all kind of ion traps that have a low current requirement ($<$10 mA), but using it for the ion-traps which do not need several voltage sources might be underutilization of the resources. Miniaturized segmented ion traps [Sch+08] or HOA-2 surface ion traps [Mau16] are two good candidates that have been successfully tested so far.

The first step before installation was the search of ghost sources radiating high energy in the trap vicinity. Spectrum analyzer and a well terminated passive/active probe with a coil connected on the other end acting as receiving antenna has been used for finding available noise frequencies in the lab. And result of this investigation was rather horrible, as due to multiple laser sources and other instruments there were several carrier frequencies which were/are available in the lab. And it was difficult to point out right origin of these ghost sources. Also, even though we may acknowledge the real cause of these noise sources, it might not be possible to get rid of them, as it might be an electrical equipment whose presence might be needed for experiments. These ghost noise sources are strong enough to deteriorate the performance of so-called low noise mAWG. And, it would not be surprising if a so-called low noise voltage source which has tested thoroughly outside of the lab, turn out otherwise in the lab.

There is no reasonable quick solution to get rid of these ghost noise sources unless until there is complete separation of the trap-system and high-frequency carrier sources like Acousto-optic modulators (AOM) drivers, EOM, Power supplies and many others for maintaining the performance of our low noise N_Bertha. The workaround in this situation is to minimize noise

which have harmonics in vicinity of working trap frequency. Besides this all the instruments can be kept as far as possible from the trap vicinity as it will attenuate the carrier amplitude. Also, all the simple BNC[1] cable in the near trap vicinity has been replaced by Pasternack's double shielded BNC[2] of RG142 co-axial type, where XX-is length of this cable. These cables are available in different length and can be ordered as per requirement. These cables have much better attenuation factor for high-frequency signal against the commercially available RG58 type cables. Apart from these noise harmonics, there is a mythical/real factor that has tremendous influence in reducing the electrical noise is ground loop. There is no clear methodology to pinpoint and establish presence ground loop in RF-trap system. For a system, which has the large current source it is relatively easy to figure out a ground loop but for our set up where maximum current feed into the RF-trap system is 2.9 A at 0.8 V from oven producing calcium vapor. Beside this, there is no other source feeding very small current. So, to establish that there is the possibility of ground loop is not easy nevertheless, its presence can also be not overlooked, as ions being super-sensitive sensor [Rus+17], can easily detect the presence of noise due to ground-loop (even with mA). The use of longer cables whose one end is directly or indirectly connected to the RF-trap system shall also be avoided.

In this appendix, the discussion starts with introducing the potential noise sources in the vicinity of ion-trap system (Sec. D.1), then trap-RF generation and control principle has been discussed in detail. This is followed by introducing the need for filtering the analog channels, the design of filters, and motivation behind their development (Sec. D.1.1). Special cable designed for connecting N_Bertha and ion-trap has been discussed (Sec. D.16) and the pin-mapping of our micro-lab segmented ion-trap and channel of N_Bertha is also presented. Then, there is a brief discussion on, how shall this design be scaled for larger ($>$ 80 electrode) ion-trap system (Sec. D.3). And finally, this chapter ends with a brief overview of the ion-trap which has been successfully tested so far.

D.1 Electrical noise in the trap vicinity

Origin of the noise and its nature as well, which leads to decoherence of qubits are not well understood in the experimental lab (in most of the cases). Although ions being sensitive sensor can precisely quantify the magnitude of this effect [Bro+15], origin of these sources can be either due to surface of trap or from the electrical sources connected to it. In our case, as access to ion-trap is limited, so we will keep our discussion limited to the electrical noise induced in

[1] Radiall RG58
[2] PE3495LF-XX

the vicinity of trap vacuum chamber. This noise can be assumed to originated from fluctuation of voltage on the trapping or neighboring electrodes and source of this effect can be either voltage-source dependent or independent of it [Sch+15]. Categorically specifying interference, flickering, inter-modulation, crosstalk noise are our assumptions and all possible effort like optimization of the ground loop, twisting the cable, improving the capacitive coupling, proper shielding of the cable and finally separation of the electronic equipment has been tried meticulously to improve the overall performance of the ion-trap-system characteristic. The ion-trap and its vacuum chamber have often been referred as trap-system. Before designing the cables that could support the translation of voltage from (female sub-D 37 connectors) analog cards to the trap flange (male 25 pins Sub-D), it is important to analyze other electrical instruments in trap-vicinity. As directly or indirectly connected wire may cause the static or dynamic voltage fluctuation, while the mere presence of strong noisy electrical equipment can cause dephasing noise.

The electrical sources which are directly coupled to the trap-system as voltage/current sources

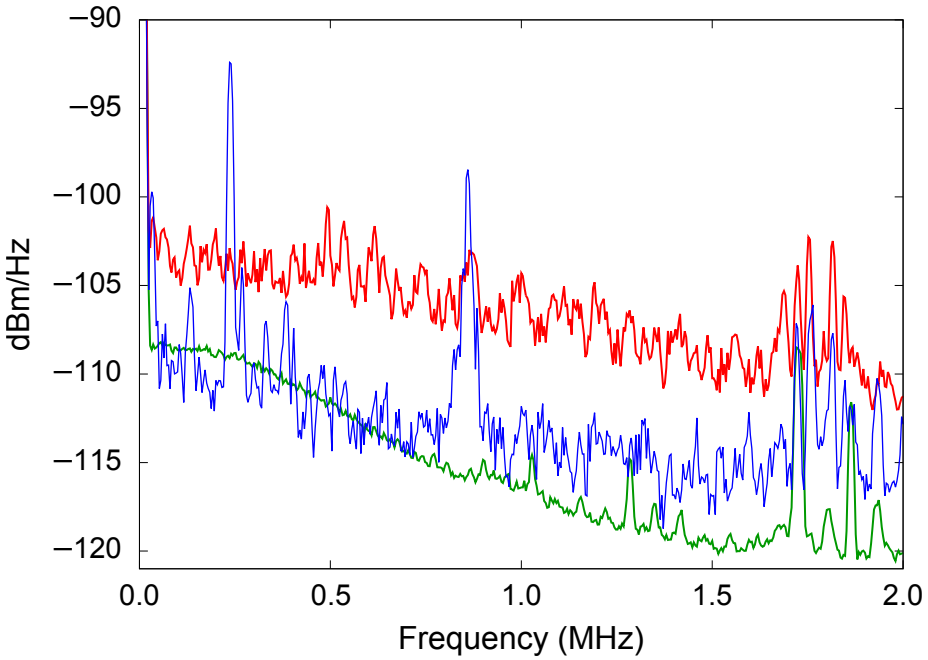


Fig. D.1 Noise level with shielded and unshielded cable. The noise spectra shown in red shows the worst case scenario, when there is no shielding in flat-cables. The indigo-spectra is for the shielded flat cable (see Fig. D.9), while green-spectra shows noise-floor for shielded-coaxial cable-RG142 type used for each channel, (see Fig. D.16 for more information on the cable design).

are analog channels, power supply for the oven that produces ca atoms, a constant power source for the vacuum chamber to maintain the vacuum pressure, and a helical resonator that generates

static RF-signal for trapping field. The sources which are indirectly coupled to the trap-system are all TTL signals which are generated from N_Bertha. These TTLs are essentially used for the precise control of the laser pulse duration and are connected to the RF-amplifier sources placed at far away places in the lab. Among all directly and indirectly coupled electrical sources, trap-RF and N_Bertha has the most complex contents and hence a properly planned arrangement is required for a better result in the experiments. The detailed discussion of the N_Bertha working mechanism has been already discussed in the appendix: C, hence in the succeeding section, we will discuss the working mechanism of the RF helical resonator. The complete detail of trap design process, its assembly inside the vacuum chamber and description of the RF system are extensively discussed in [Kau+17].

RF-system outside the vacuum chamber has RF signal generator [3], power amplifier[4], the helical resonator, stabilization circuit [Dil14] and capacitive coupled monitor circuit for monitoring the RF amplitude on the RF electrodes of the ion-trap. The electrical arrangement RF system has been re-mapped around the trap vicinity in order to improve the performance of the helical resonator. This overhauled makeover was important as it helped us to improve the trap characterization (see Sec. 3). Earlier [Kau+17], in the RF system, RF source of 33.15 MHz at -13 dBm was fed into the water cooler amplifier to generate the RF amplitude 27 dBm to fed into the helical resonator to achieve 300 V PK-PK (at the resonance frequency) at the RF electrode of the trap. While in current set-up the RF signal generated (~33.14 MHz) from the RF main source fed as an input to same water-cooled 50 Ω power amplifier that amplifies the RF signal from ~-17 dBm to ~23 dBm. This amplified RF signal is then fed as input to helical resonator which enhances the signal with the quality factor of ~100 i.e ~320 V (PK-PK).

Therefore, in the same trap-system, now higher quality factor has been achieved by optimizing the impedance at same resonating frequency. The resonanting frequency for installed helical resonator is affected by all directly/indirectly connected electrical instruments. So, any mismatch in impedance in-turn affects the quality factor of the helical resonator. And, if the helical resonator does find the right match for which it is optimized, the Q factor decrease and hence more power is needed to achieve required RF amplitude (even by unintentional hanging wire can do it). It can be inferenced from the current evident condition that the trap-system need to optimized in such a way that there is minimal loss of power into int. Hence, if the impedance is not matched well, in experiments ion get heated faster and measurement reports large rise in heating rates. The sensitivity of it can be accessed from the fact that it varies the

[3] R&S SMA100A Signal generator 9 kHz to 6 GHz,
[4] Mini circuit ZHL-5W-1+

measured heating rate from 10-1000 times.

Therefore, every individual signal that is connected to the trap-system must be given a dedicated GND line, which stays in the close vicinity to the main ground plane. This idea has been passed to design the cables, whose assembly instruction has been given in see Sec. D.16. The current transverse secular frequency at 320 V PK-PK are $\omega_{x,y,z}/2\pi = \{1.5, 3.8, 4.6\}$ MHz (LIZ, seg: 20 or 19). The cable assembly instruction norm shall be followed strictly otherwise optimal configuration will be difficult to achieve. The engineered cable and ground system are shown in Fig. D.19 reduces the mainline 50 Hz noises as well.

RF monitor and rectifier circuit

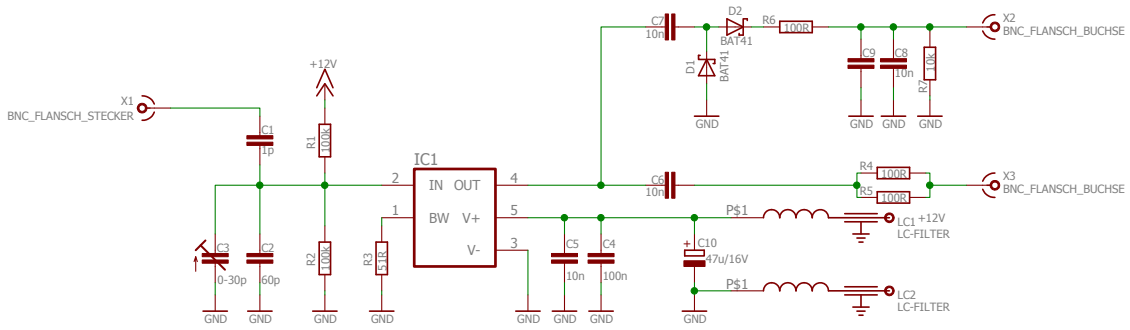


Fig. D.2 Circuit diagram of instrument hooked to trap-RF source for monitoring amplitude of resonantly amplified RF-signal used in the ion-trap. Its rectifier circuit feeds DC-conversion of capacitive coupled RF-signal used in monitoring.

There is a rectifier circuit (see Fig. D.2) which is hooked to resonantly amplified RF signal connected to RF electrodes of trap. It capacitively couples (see Tab. D.1) to the resonantly amplified RF signal, which in turn is monitored to track the working RF amplitude and frequency on the RF-electrodes. It couples ~1/120 part of the trap-RF signal at 33.14 MHz and inbuilt rectifier circuit converts this ac signal into dc and feeds to the input of the PI (proportional integral) controlled feedback system [Dil14; Kau18]. This PI control system affects the trap system in two-way, first it changes the impedance mismatch (if any) for the helical resonator, second, it provides external amplitude modulation to compensate the trap-RF, i.e any change in the amplitude is compensated by the PI controller. This provides active support to prevent any

delta change against preset RF amplitude, however, our effort was to provide optimal external stability to the transverse frequency by improving the capacitive coupling at the junction i.e where RF-monitor signal is capacitively coupled to trap-system RF signal. In absence of this active stabilization, instability in the RF amplitude is ~$2\pi\times6$ kHz, which improves to less than $2\pi\times40$ Hz [Kau18] with this active stabilization. But, this endeavor does not pay off in term of radial modes stability (in term of heating of the ions) and transverse stability measured with and without active stabilization remains same. However, it increases the decoherence contrast of the motion and spin superposition state (discussed in section.3.4).

This capacitively coupled circuit induces flickering noise due to non-stable capacitive reactance contribution to the output impedance of the helical resonator. Therefore, new circuit Fig. D.2 has been designed to reduce this effect. It offers higher capacitive reactance to the resonating circuit.

There is a changing capacitive attenuator circuit (with C1,C2, and C2) that loads resonantly amplified RF signal (see Fig. D.2). The attenuated signal (theoretically 1:90) is biased with a 12 V dc signal at the input of IC1[5] which is a high-speed unity gain OpAmp acting as the buffer. The DC part of the buffered is blocked by C7 (10 nF), and a signal is rectified by diode D2[6] and D1[6], to produce a rectified output at X2. Similarly, at another node, the biased DC voltage at buffered output is blocked by C6 and then ac-signal is available for monitoring main RF amplitude and frequency. For example, if trap has voltage of 300 V PK-PK, then ~3 V PK-PK will be biased with 6V and same will be available before C6 and C7, which will block DC offsets and allow the ac signals to pass through so at X2 we shall get 3 V PK-PK, and X3 we can monitor less than 3 V as diode biasing voltage.

The table:D.1 is calibration data of RF signal generator[3], the helical resonator, power amplifier[4], and rectifier circuit using the setup shown in Fig. D.3. Input is the delivered power by the RF signal generator to the amplifier. Then, it is resonantly amplified by the helical resonator, this amplified signal (RF output) is measured at the junction output from the helical resonator. Thereafter, at the output ports of the monitor and rectifier circuit, attenuated and rectified signal is measured at X3 and X2.

The calibration was done at 51 kHz while the actual trap is currently working at 33.14 kHz, therefore to exact attenuation ratio can be measured with the transfer function (see Fig. D.4b)

[5] BUF634
[6] BAT41

Input (dBm)	ZHL-5W-1 (dBm)	RF output V(pk-pk)	Monitor output V(pk-pk)	Rectifier output V	coupling strength
-27	10	86	0.71	0.36	1:121
-20	17	190	1.56	1.13	1:122
-17	20	266	2.24	1.74	1:119
-16	21	300	2.50	2.00	1:120
-14.6	22.4	350	2.90	2.35	1:121
-13	24	412	3.44	2.89	1:120
-11	26	520	4.41	3.66	1:127
-9	28	650	5	4.67	1:130

Table D.1 Test result of the monitor and rectifier circuit (51 kHz) outside of the lab. Currently in lab, the resonance frequency is 33.14 kHz, while the monitor circuit display 380V pk-pk. It means actual amplitude at trap-RF is 320V (pk-pk) as the coupling strength is ~1:120 at 33 kHz.

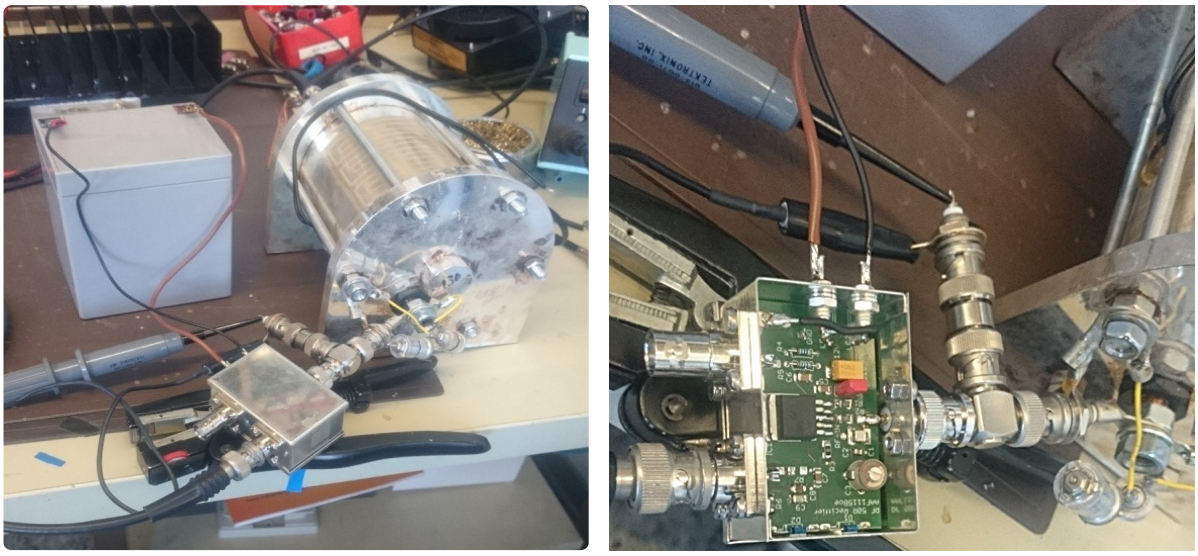
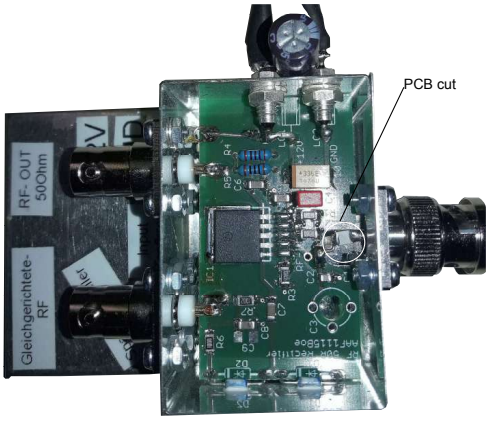


Fig. D.3 Helical resonator and RF monitor/rectifier circuit test set up outside of the lab. The exact lab environment is difficult to reproduce however for fixed tap point we vary the frequency and characteristic impedance to find the coupling strength and linearity relation between RF and respective DC output.

of this circuit. Moreover, the attenuation capacitive reactance has to be as small as possible therefore 1 pF surface mounted capacitor were loading the RF signal and therefore PCB has been cut off, to minimize this effect (see Fig. D.4a).

(a) RF Monitor/rectifier circuit



(b) current operating region of trap-RF

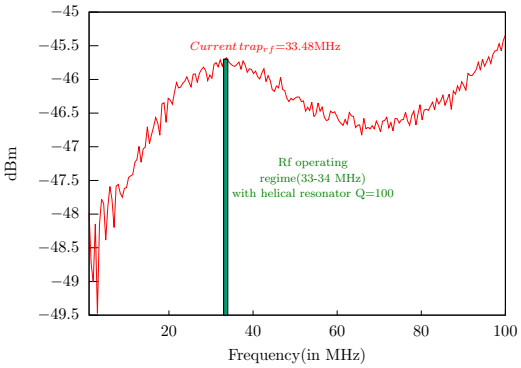


Fig. D.4 **(a.)** PCB of the monitor/rectifier circuit, PCB near the coupling area has been cut out to improve the capacitive coupling. **(b.)** the transfer function of this circuit, the green region is working regime for trap-RF.

D.1.1 Filters

For ion traps electrodes, it is needed to resolve the asymmetric patch potential that gives rise to the static electric field to deviate the ion from it's trapping node [DJ+] is generally done by the installing a low-pass filter, close to the trap-system, in our case it rights above the top-flange of the vacuum chamber. For this purpose, there was a 50 kHz filter were used to filter all the analog channel, however later on the measurement revealed that such heavy filtering is not needed, and we can improve the cutoff limit, therefore 100 kHz filter is now in use. Besides this, due to the complex design of our segment controller, there are signals in GHz range these and the low-pass filter is unable to attenuate it, therefore addition inline-filters has been designed for attenuating the noise rising due to metallic housing. Both of these filters have discussed below.

Low-pass filter

The second order low-pass filter designed for filtering the static analog voltages of N_Bertha has CLRC topology, that has been designed by Claudia Warsburger. The cutoff frequency of this low-pass has been decided according to the experimental requirement. Motional modes of the ions are very sensitive to electric field density that shares spectrum near their motional frequency (Tab.3.2). Therefore, the noise spectrum in the vicinity or at the trap-frequency needs to be filtered heavily. In other words, near the motional mode frequency, if possible noise shall be in its lower limit, i.e theoretically the thermal noise that is produced by the resistance of the

connected circuit shall be present only.
Therefore, a cutoff frequency which is way lower than working motional mode frequency shall be chosen for this purpose. A filter of f_c=50 kHz has been chosen and subsequent successful demonstration of fast shuttling operation has been performed [Rus+14; Kau+16]. Later on,

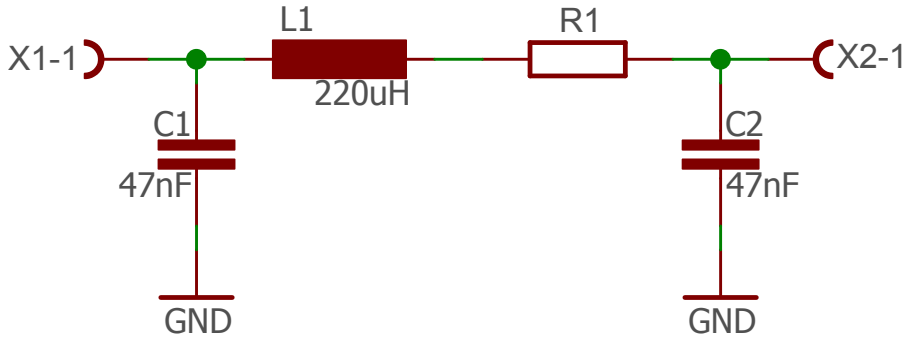
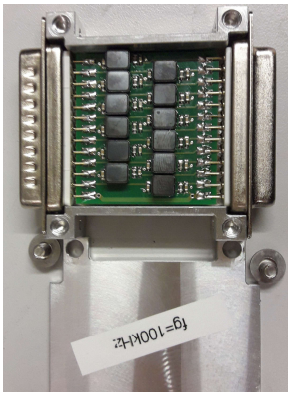


Fig. D.5 Schematic of the LRC type low-pass filter. This filter is installed right at feedthrough for filtering the analog voltages used for trapping and shuttling operations. The cut-off of this filter is $f_c = 100$ kHz.

(a) 100 kHz filter



(b) Filter response curve

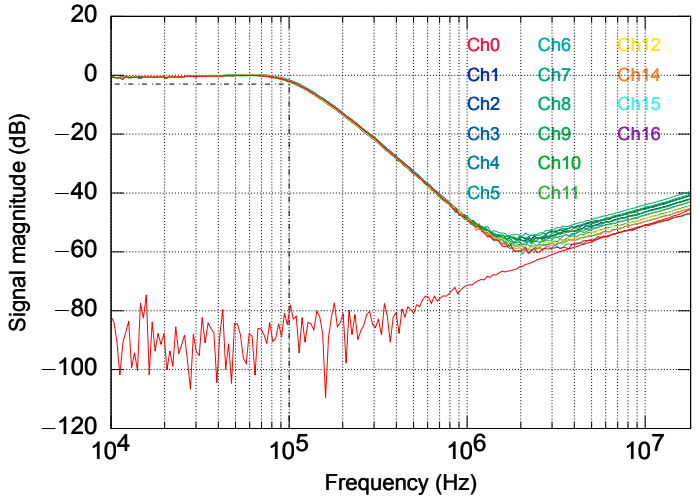


Fig. D.6 Response characteristic of all (16) 100 kHz low-pass filters. The minimum relative crosstalk attenuation (bottom red curve) on the nearest neighboring channels is 100 dB. It is measurement of the filter connected at flange:02.

due to significant experimental updates, similar low-pass filter with higher cutoff f_c=100 kHz has been successfully demonstrated to be used.

The schematic of low-pass filter has been shown in Fig. D.5. The specific arrangement of the different parts on the PCB has been manually tested and optimized for minimal cross-talk and linearity behavior. It contains 24 individual low-pass filters for analog channels, assembled together on a 35×36.99 mm of PCB. It has sub-D 32 pin male and female pin mapping. One end is mounted directly on the SUB-D pin slot at the top flange while another end is connected to the N_Bertha cable (see section.D.16). However, currently only 16 out of 24 entity is in use over each slot, rest are unconnected. The test of each of the inline is important as it has been found that even though identical parts have been used but still some inline filter-channels have been seen exhibiting different transfer function than others, which has been resolved by merely using new parts. Each of the filters has been tested well for the similar response in mainly in term of cutoff, crosstalk, overshoot and undershoot, before installing at the respective slot of the flange. The response curve of low-pass filters recorded for Sub-D slot.2 of the top flange is shown in Fig. D.6b. All the other units in rest of the Sub-D of the top flange has been tested for an identical response as shown in Fig. D.6b. It is recommended that before implementing any future update on use low-pass filter, crosstalk and channel characterization shall be matched with this.

The components used in this filter are f_c=50 kHz (C1=47nF[7], L1=220uH[8], R1=69.8R[9], C2=47nF[7]), while for f_c=100 kHz, (C1=69.8nF[10], L1=150μH[11], R1=69.8R[9], C2=69.8nF[10]).

Inline-prefilter

The presence of high-frequency signals has been noticed due to the structural envelope of the segment controller (the metallic housing that is used to house all the electronics developed)[12]. It is difficult to trace the exact reason and origin of this noise. These signals have been observed only if the output of the analog channels is measured after installation within the box.There are no sources in the design which generates GHz range signals, also the amplitude of these signals have been measured to vary in the range of {30,80} mV. Therefore, it appears as if the low signal is being resonantly amplified here. This can be understood as: the housing can be modeled as resonator circuit (LCR), therefore fast switching of the digital signals on the analog card might induce signals in this resonator which is being noticed at the output. These unwanted high-frequency signals are present at the GND line of the analog channels. Therefore,

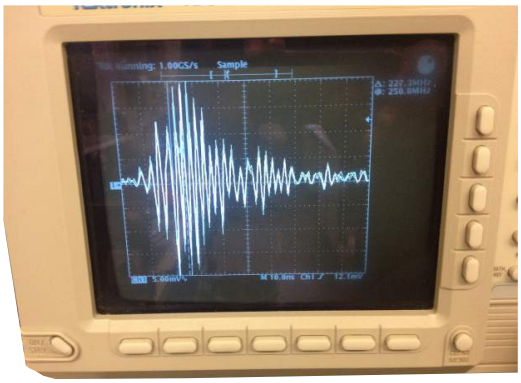
[7] AVX 06035C473KAT2A
[8] COILCRAFT 1812PS-224JLB
[9] TE CONNECTIVITY 5-1879222-5
[10] AVX 06035C223KAT2A
[11] COILCRAFT 1812PS-154JLB
[12] EuropacPRO kit from Schroff Catalog Number: 24563-474

low-pass filter is unable to attenuate it. Hence, to prevent it from emitting N_Bertha cabinet the inline-prefilter has been designed.

The T-type filter[13] was chosen to get the highest attenuation at 400 kHz. It's beaded at the in- and output which dissipates high-frequency signals as heat, while the capacitor with its small serial inductance will short RF to ground. The frequency response in the data-sheet was obtained with 50 Ω at both the signal source and sink, whereas the source impedance of the OpAmp in an analog channel is ~400 kHz, which is complex and high impedance. Also, the trap itself is not 50 Ω. Therefore, a 47 Ω resistor has been added at the output of this T-filter, that also provide termination for the RG178 coaxial cable, which has been used for connecting segment controller to the trap flange.

This does not only prevent the high-frequency signals emitting from the housing but also attenuates the digital crosstalk (~150 mV to ~15 mV, the attenuation factor of 15) which is seen at the analog channels even with the low-pass filters. Fig. D.7a and Fig. D.7b are the view of observed structural and digital crosstalk noise and their attenuation using the inline-prefilter.

(a) Noise due to metallic housing



(b) Attenuation of metallic housing noise

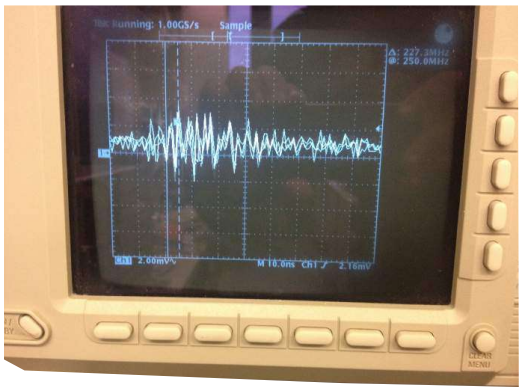
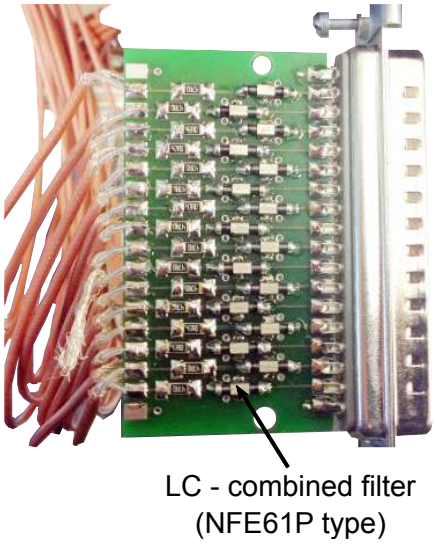


Fig. D.7 **(a.)** Presence of the unwanted noise due to structural design, which includes big 19änd 6H metallic cabinet and cable, otherwise this noise are not visible if the analog cards are tested outside the metallic box. **(b.)** Attenuation of noise caused due to structural design by installing a filter right at the output, this is called prefilter.

[13] NFE61PT472C1H6

(a) Prefilter assembly



(b) Attenuation of the digital crosstalk

Fig. D.8 Image of several T-filters on PCB (53.91×29.7 mm) with terminating resistance and its attenuation of digital noise by this filter. **(a)** NFE61P type T-filter are installed with 47 kΩ terminating resistors.**(b)** Green signal is final signal, which attenuates digital crosstalk from neighboring channels. It was measured at channel0 with 50 kHz low-pass filter (without inline-T-filter), while adjacent channel (channel1) is monitored with inline-filter (Red signal). This crosstalk noise is available on all channels. For both channels, there are same voltage scale.

D.2 Cable assembly for ion trap feedthrough

We have been using standard shielded sub-D 25 flat cable (Fig. D.9) with old segment controller. Its female end was connected to the flange and male end was hooked to the old segment controller. It is 25 conductors flexible flat cable with copper shielding wrapped around it. This wrapped shielding has to connect to Pin:13. Fig. D.9 shows the lab optimized version by Henning Kaufman, where multiple additional wires have been added to end the GND loop. (Relevant to the internal members of our group: pin:13 is the standard dedicated GND pin used in all the Sub-D25 flat cable connections). The attenuation of crosstalk in flat cable for kHz signals (<100 kHz) range is ~-90 dBm (~0.177 mV). Therefore, a cable design which has crosstalk-attenuation below floor-noise of N_Bertha and maintain highest SNR are the fundamental requirement for the cable design. The noise-floor level of flat-cable is same as of N_Bertha but due to thin shielding layer, it is difficult to maintain the best SNR ratio for our set-up hence more susceptible for the induced fields. Therefore, smaller pitch width (0.5 mm between two channels) and thin shielding were the limiting factors of flat-cable. Moreover,

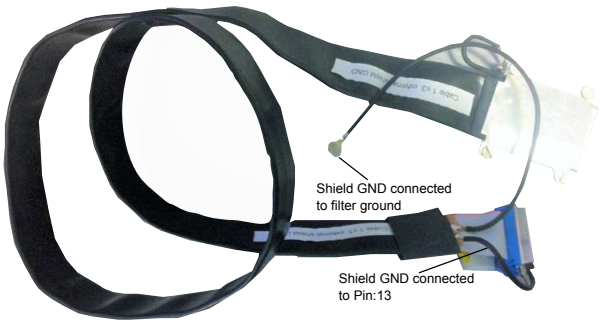


Fig. D.9 Old flat cables used for old segment controller.

our trap flange contains sub-D 25 pin and analog card has sub-D37 poles which would be a mismatch if use flexible flat cable for this design. Considering all these factors we decided to use a thin coaxial cable (RG178) as it provides us highest SNR ratio in a noisy environment (lab). Beside this there are multiple benefits of using these cable like we could maintain signal integrity of every channel and also a one-to-one mapping of individual channels will reduce the crosstalk. The attenuation measured with 16 cables RG178 cable bundled together is lesser than <-110 dBm for the kHz signals (<100 kHz).

But all these benefits come at the cost of designing an absolutely new cable design that shall be able to bias numerous trap-electrodes as per our requirement. Therefore, based on these benefits two different kinds of bundled cable (Type_1 and Type_2) have been made for trial and error based test purpose to match the lab requirement. The further optimization in the lab has been used with assuming the trap-system as a system that should be operated with minimum RF-power. The result reported are purely based on trial and error methodology.

Fig. D.10 to Fig. D.14 demonstrates the step for installation of the final cable (Type_1), that is in use in the lab. It is recommended to keep cable length as short as possible. And also, it should be taken care that GND of the respective signals find its main ground in proximity of its high impedance load. It is also recommended for using specified parts for best results.

The type_2 cable is mounted with specially designed inline filters that attenuates high-frequency noise caused by the complex structural entity bought to house all electronics that includes all components of N_Bertha. The idea of exact nature and source of this radiated field from this structure with the electronics inside might be needed for its proper control, but to model it and do a precise calculation of it could be very beyond the scope of this thesis.

Fig. D.10 Bundle of 16 RG178 cables inside the insulation tube and shielding

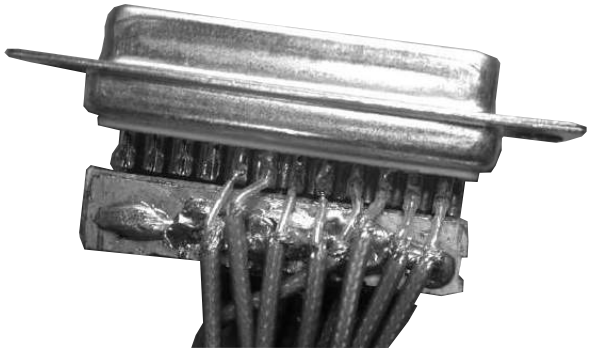


Fig. D.11 Copper plate installed close to pin for improving single pin (pin13) ground

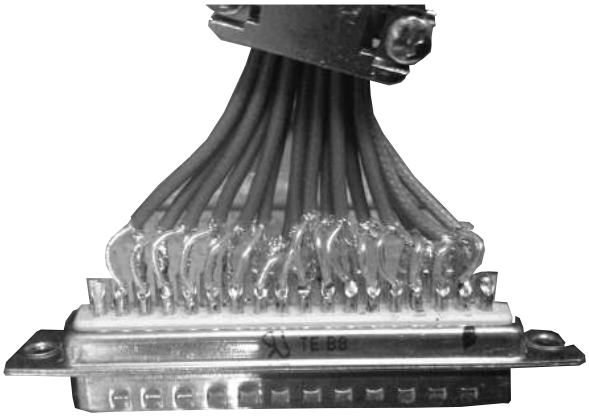


Fig. D.12 Image of dedicated GND pins for each channels

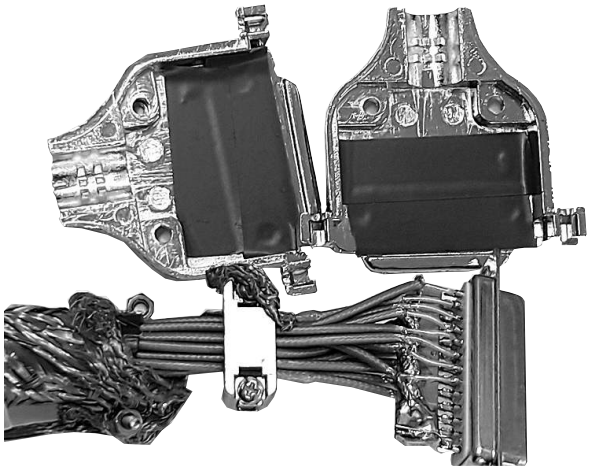


Fig. D.13 Image of metallic connector case insulated from inside

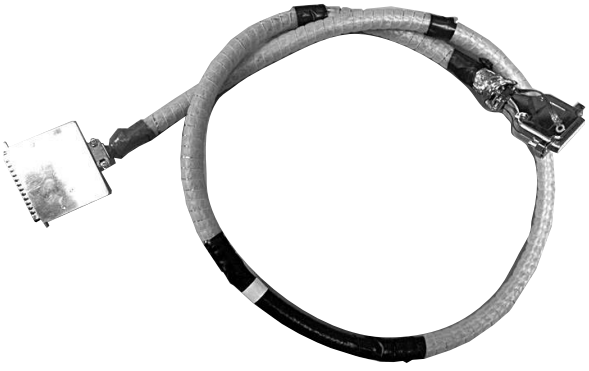


Fig. D.14 Image of external shielding insulated using cable spiral

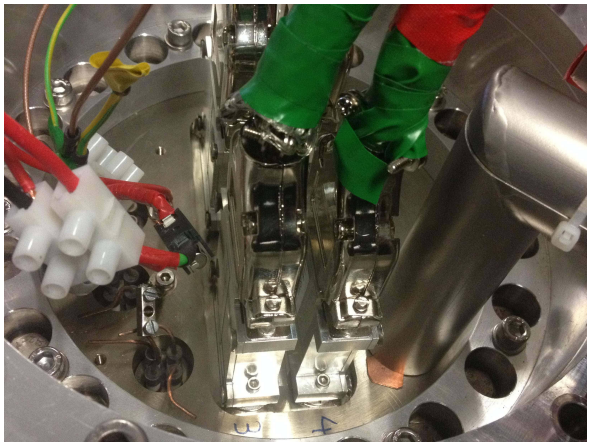


Fig. D.15 Image of installed cable in lab picture with low-pass filters at feedthrough

Fig. D.16 Cable installation steps

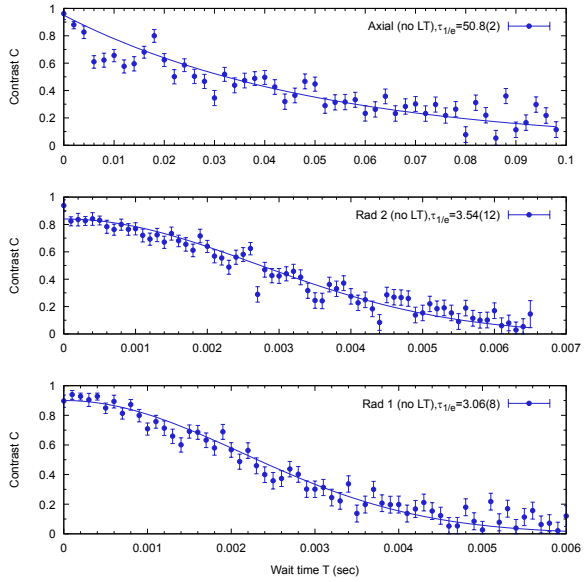


Fig. D.17 Motional coherence showing improved decoherence duration after installation of N_Bertha, which featured reduced noise figure and enhanced attenuation of 50 Hz noise from AC-main lines. The old data has been taken from the doctoral thesis of Henning Kaufman [Kau18].

modes	freq (MHz)	old (ms)	new (ms)
		no LT	no LT
axial(ω_x)	$2\pi\times$ 1.5	58.7(9)	56(2)
rad1(ω_y)	$2\pi\times$ 3.6	**0.248(9)**	**3.06(8)**
rad2(ω_z)	$2\pi\times$ 4.8	**0.323(7)**	**3.54(12)**

Table D.2 The improved motional coherence after installation of N_Bertha, Substantial attenuation of the 50 Hz noise has been achieved with the recommended wiring style (see Fig. D.16).

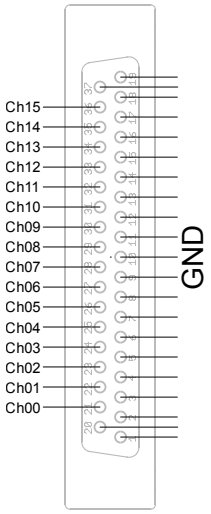


Fig. D.18 Pin-mapping of analog-channels and Sub-D 37 pin connector in any analog cards.

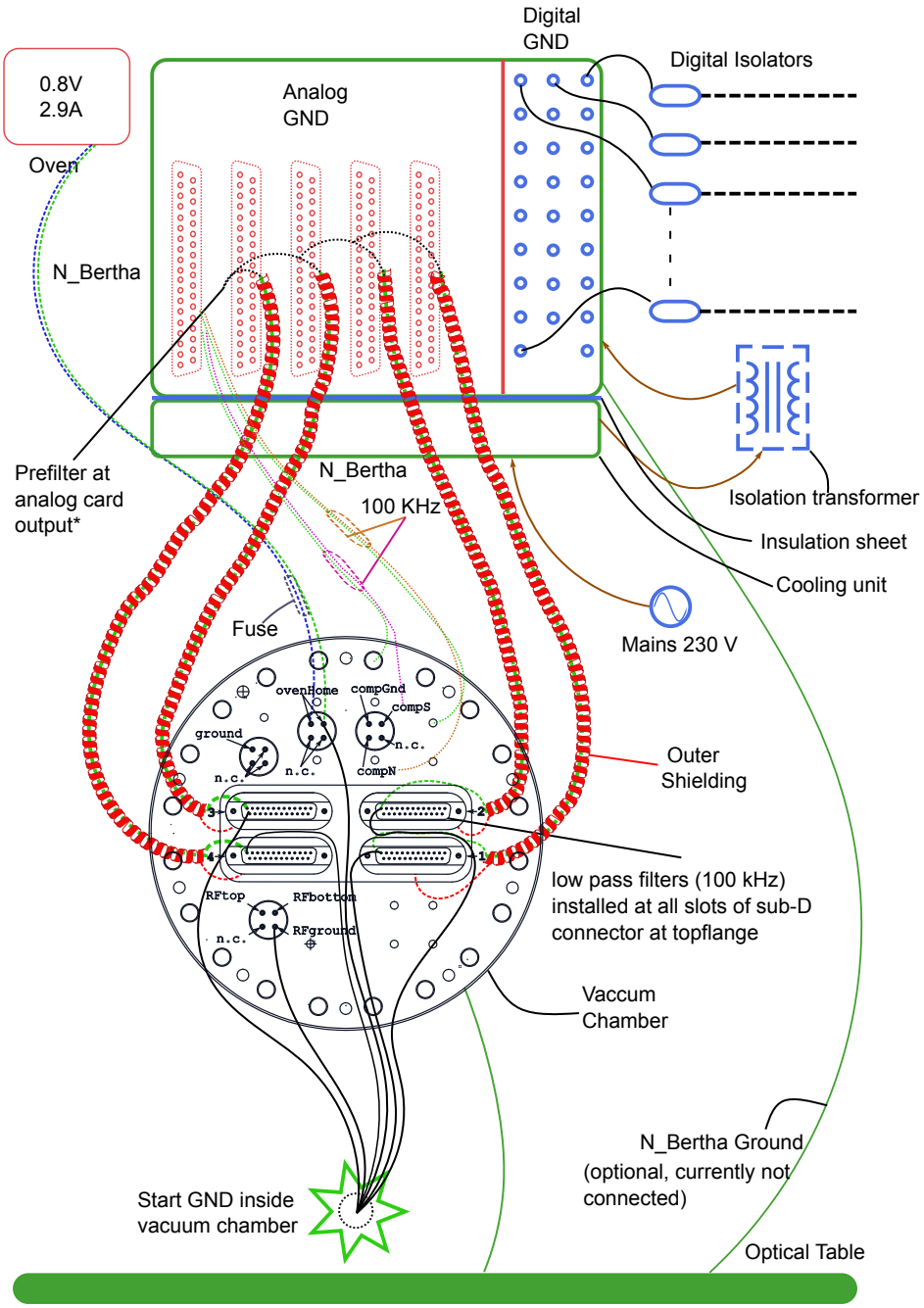


Fig. D.19 Recommended wiring of trap-system with the cable (see Sec. D.16). The individual 100 kHz filters are the simple first order RC (R=100 Ω, C=10 µF) filter. While, the special low-pass filter (see section.D.1.1) is installed right on the flange. This wiring style has enabled to drive the helical resonator with the highest quality-factor (Q) and also provides suppression of 50 Hz noise (see Tab. D.2) which have been dominant in this trap-system earlier.

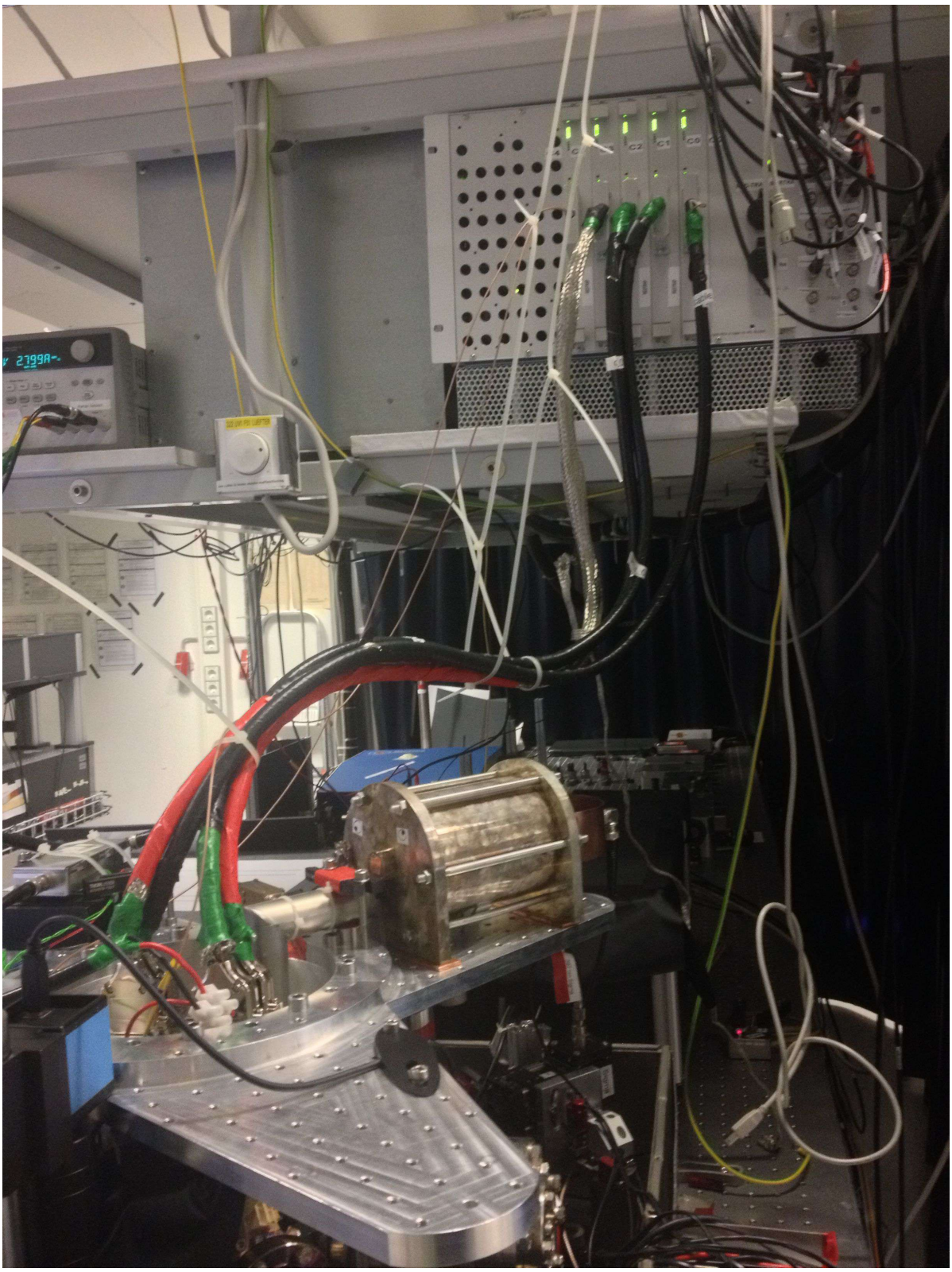


Fig. D.20 The image N_Bertha in use with segmented ion trap in the lab.

Channel detail[14]	connection details[15]	channel detail[14]	connection details[15]
{0,**0**}	{**1**,1,1}	{2,**0**}	{**17**,3,1}
{0,**1**}	{**2**,1,2}	{2,**1**}	{**18**,3,2}
{0,**2**}	{**3**,1,3}	{2,**2**}	{**19**,3,3}
{0,**3**}	{**4**,1,4}	{2,**3**}	{**20**,3,4}
{0,**4**}	{**5**,1,5}	{2,**4**}	{**21**,3,5}
{0,**5**}	{**6**,1,6}	{2,**5**}	{**22**,3,6}
{0,**6**}	{**7**,1,7}	{2,**6**}	{**23**,3,7}
{0,**7**}	{**8**,1,8}	{2,**7**}	{**24**,3,8}
{0,**8**}	{**101**,1,14}	{2,**0**}	{**117**,3,14}
{0,**9**}	{**102**,1,15}	{2,**1**}	{**118**,3,15}
{0,**10**}	{**103**,1,16}	{2,**2**}	{**119**,3,16}
{0,**11**}	{**104**,1,17}	{2,**3**}	{**120**,3,17}
{0,**12**}	{**105**,1,18}	{2,**4**}	{**121**,3,18}
{0,**13**}	{**106**,1,19}	{2,**5**}	{**122**,3,19}
{0,**14**}	{**107**,1,20}	{2,**6**}	{**123**,3,20}
{0,**15**}	{**108**,1,21}	{2,**7**}	{**124**,3,21}
{1,**0**}	{**9**,2,1}	{3,**0**}	{**25**,4, 1}
{1,**1**}	{**10**,2,2}	{3,**1**}	{**26**,4,2}
{1,**2**}	{**11**,2,3}	{3,**2**}	{**27**,4,3}
{1,**3**}	{**12**,2,4}	{3,**3**}	{**28**,4,4}
{1,**4**}	{**13**,2,5}	{3,**4**}	{**29**,4,5}
{1,**5**}	{**14**,2,6}	{3,**5**}	{**30**,4,6}
{1,**6**}	{**15**,2,7}	{3,**6**}	{**31**,4,7}
{1,**7**}	{**16**,2,8}	{3,**7**}	{**32**,4,8}
{1,**8**}	{**109**,2,14}	{3,**0**}	{**125**,4,14}
{1,**9**}	{**110**,2,15}	{3,**1**}	{**126**,4,15}
{1,**10**}	{**111**,2,16}	{3,**2**}	{**127**,4,16}
{1,**11**}	{**112**,2,17}	{3,**3**}	{**128**,4,17}
{1,**12**}	{**113**,2,18}	{3,**4**}	{**129**,4,18}
{1,**13**}	{**114**,2,19}	{3,**5**}	{**130**,4,19}
{1,**14**}	{**115**,2,20}	{3,**6**}	{**131**,4,20}
{1,**15**}	{**116**,2,21}	{3,**7**}	{**132**,4,21}

Table D.3 The pin mapping among N_Bertha analog cards and its channels, Sub-D slot on top flange, trapping segment and pin-number in respective Sub-D slot

[14] {card number,**channel number**}

[15] {**trap segment number**,Sub-D slot on top flange,pin-number in respective Sub-D slot}

Nevertheless, we developed a workaround method by designing an in-line filter that could attenuate this signal. Its magnitude goes up to $\sim$70 mV and it is mainly available at the GND line of the analog channels at the SUB-D 37 output. The timescale of these signal varies in few GHz ranges ($\sim<$5 GHz). It is very unlikely that these signal can be harmonics of lower frequency signals as the amplitude of this signal is substantially large ($\sim$70 mV).

D.3 N_Bertha as scalable voltage generation technology for scalable ion-traps

N_Bertha has been designed for providing scalable voltage support for even larger (beyond 80 electrodes) segmented ion-traps. The scalability features of N_Bertha provide simultaneous support for numerous trapping electrodes for such experiments. The design constraint confines the upper limits of the trapping electrodes as 1600 (20×80), which mean 20 N_Bertha units can be simultaneously activated with precise control on each of the analog channels in less than 400 ns, with well quantified electrical error budgets (Sec. 56). But before using this, one has precluded that ion-traps shall match the specification requirements laid down by N_Bertha . More specifically if the net impedance of trap electrode >4 KΩ then it safe (for the N_Bertha) to bias the ion-trap electrodes, as it has not been designed to derive the loads (ion trap electrodes) of lower impedance. However, there are push and pull circuit (see Sec. 44) that can fulfill the emergency requirement (if any) up to (<10) mA when all the channels are simultaneously swinging Voltage within $\pm$40. It is also important to check if the trap electrode is designed for $\pm$40 V.

As in case if the trap electrodes are not designed for $\pm$40V then it is not recommended using these analog cards merely by assuming that voltages shall be controlled by using the software. As during the initialization process of SoC-FPGA , the voltage can swing between $\pm$40V and as a designer we have no control over this. It occurs as due initialization process of SoC-FPGA spits outs random digital signals before actual onboard program could reset the digital logic to the predefined states. This random logic can be differentiated from the analog side hence can lead to a situation where it can swing between its limits. Apart from this situation, the voltage may also move to -40V due to a short circuit caused due to low impedance loads. Both of these situations are dangerous for the ion-traps whose voltage is less than $\pm$40. Therefore, for these kinds of traps, there are two recommendations. Either reduce the amplification gain by changing the gain resistors of the analog card or design attenuators based on voltage divider and use N_Bertha with recommended cable design (Sec. D.16). By

changing the gain resistors to lower gain, the resolution and slew rate will improve while the use of voltage divider will have larger slew rate. However, replacement of the gain resistor shall be done only by profession to eliminate any misdeed with other onboard electronics.

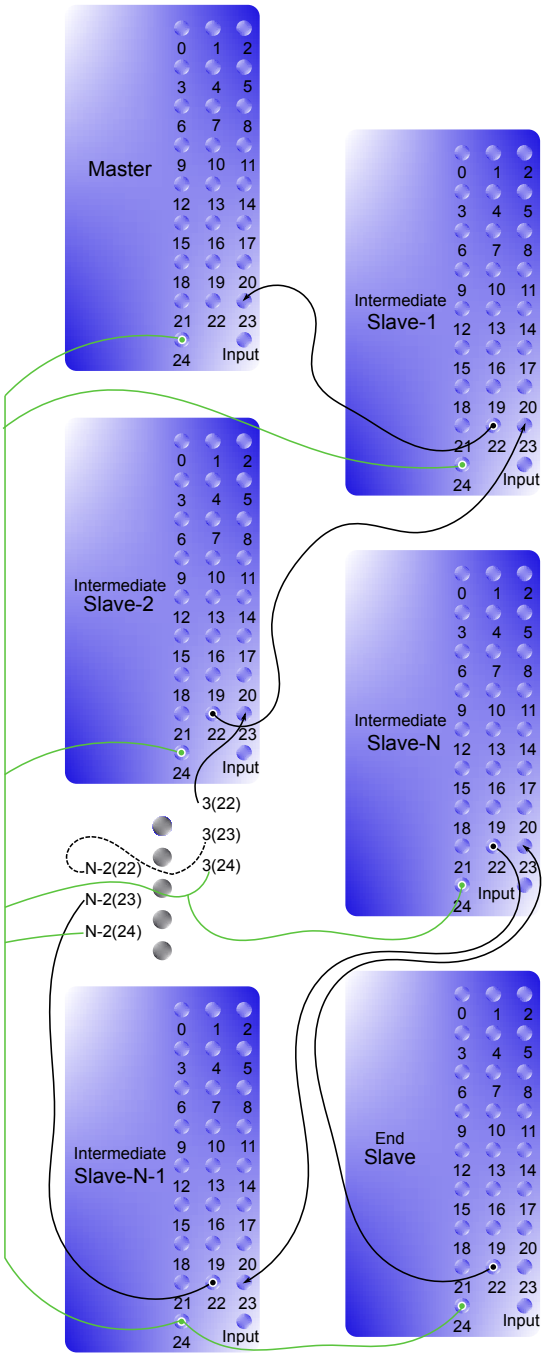


Fig. D.21 Master Slave configuration for biasing more than large number (>80) of trap-electrodes.

Master-Slave type of configuration can be adapted to bias numerous electrodes in micro-structure ion-traps (see Fig. D.21). This configuration is a daisy chaining of three variants of N_Bertha units. The variant are Master (project_1_M), Intermediate_slave (project_1_Ins) and End_Slave (project_1_EnS). The Master variant sits at the top in the hierarchy level. As the name suggests all the subsequent Intermediate Slave variants are situated in the middle level, while End_slave is the last one in the chain. It is recommended to rename the Intermediate_slaves serially (1,2,3....N) (as suggested in Fig. D.21) for the sake of simplicity. All the intermediate_Berthas are an identical copy of each other. The respective hardware configuration (.bin files) from their parent's directory can be used to program the respective entity of this configuration. These bin files are part of digital submission along with this thesis. For example, Master program shall be used to program Master and the same holds for a respective slave.

Synchronization principle for master-slave system

The master-slave version of N_Bertha is similar to its standalone version (see Sec. C) except for few special ports which are mainly used for synchronizing the master and rest of the slave unit within the resolution of 20 ns. Hardware-wise Master has one special output port at Pin:24 and Pin:23 for synchronization, while End_Slave has output port at Pin:22 and input port at Pin:24. However, all Intermediate_slave being an identical copy of each other contains Pin:22 as an output port, Pin:23 and Pin:24 as the input ports.

Pin:22 of End_Slave is output port that sends out its status information to its neighboring (N)the intermediate slave, While Pin:22 of the Nth slave is gated output with its input Pin:23 that receives the information from End_Slave. This way the information is passed to the top of the hierarchy. Nth slave contains the status report of End_Slave, while (N-1)the slave contains the information about a Nth slave, and End_slave and so on. This way the Master that is sitting at the top contains information of all the slaves.

The connection shall be established as suggested in Fig. D.21. Pin:24 of all the units (Master, intermediate, End) shall be connected to each other. This pin is the output of the master device is being used to pass initialize command to all the slave units.

Input Pin:22 of the End_Slave has to be connected to the Pin:23 of the last Intermediate_Slave (say N) in hierarchy level. Then Pin:22 of the Nth slave be connected to Pin:23 of (N-1)the intermediate slave. This scheme rises up in the level of hierarchy follows till Pin:22 of

the firstst intermediate slave is connected to the Pin:23 of the Master unit.

Except the End_slave there is an and gate inside all the intermediate slave, so when subsequent slave informs that data has been successfully storing in the First FIFO it issues a ready signal to its neighboring intermediate slave. Neighboring slave access their status information to the neighboring slave, in this fashion the information that all the slaves are ready for use.

It has been well tested with two units (Master and End_slave), successfully. Apart from this configuration, multiple individual N_Bertha units can be installed and triggered simultaneously to achieve a similar situation.

software guide for master-slave system

All the units need to be connected via a router. It is recommended to send data in the bottom to top way. This means the experimental sequences shall be encoded and well documented so that the right data group shall be sent to the right units. This experimental sequence data shall be sent to End_slave, then Nth slave, followed by (N-1)th slave and finally to the Master unit. Once the master unit passes initialize command via Pin:24 then all the analog channels shall be synchronously programming the requisite waveform.

In order to achieve this, a distinct IP address for each of the units shall be edited in the C files of SoC-FPGA and then programmed distinctly to the SoC-FPGA . This is needed to avoid the conflict of IP among different units working together. It is not needed for single units as there is no scope of conflict in these cases. For example, if Master has IP of 172.16.1.10, then others shall be distinctly programmed as 172.16.1.11 and so on.

This will be some work from the software side, nevertheless, we have successfully demonstrated master-slave configuration for two units, hence an implementation shall not be very difficult.

Different ion-traps in use with mAWG (N_Bertha)

There are still several ion-traps which is still using the old-segment controller [S+06; Dan+14; Fel+15]. However, with N_Bertha, besides the segmented ion trap discussed in this thesis, some other ion traps as follows.

1. CQED ion-trap [Pfi+16]

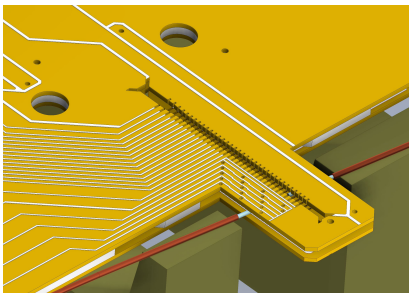


Fig. D.22 CQEDTrap in Mainz

2. Sandia-trap [Mau16]

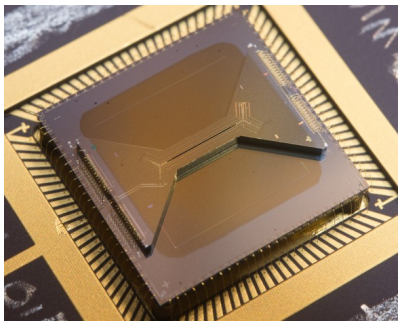


Fig. D.23 Sandia's HOA-2 trap

Fig. D.24 Tested ion-traps with N_Bertha.

Analog card and backplane

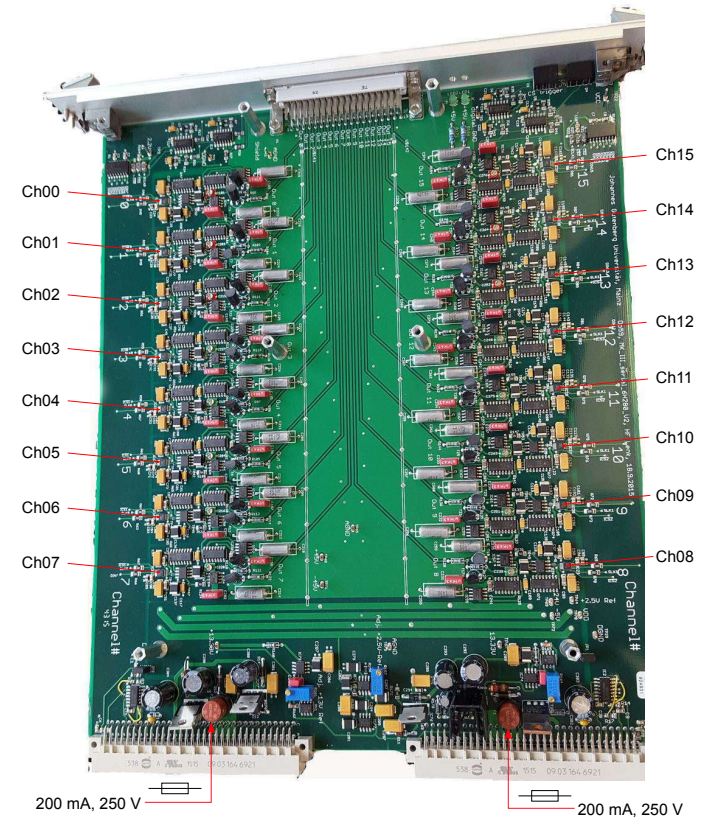


Fig. E.1 Possible troubleshooting for Analog card

Troubleshoot: If any of the output channel of the card is stuck to -40 V, then it might be the fuse(see Fig. E.1) which needs replacement. Replace both the fuses and also check for the reason, which might have caused this.

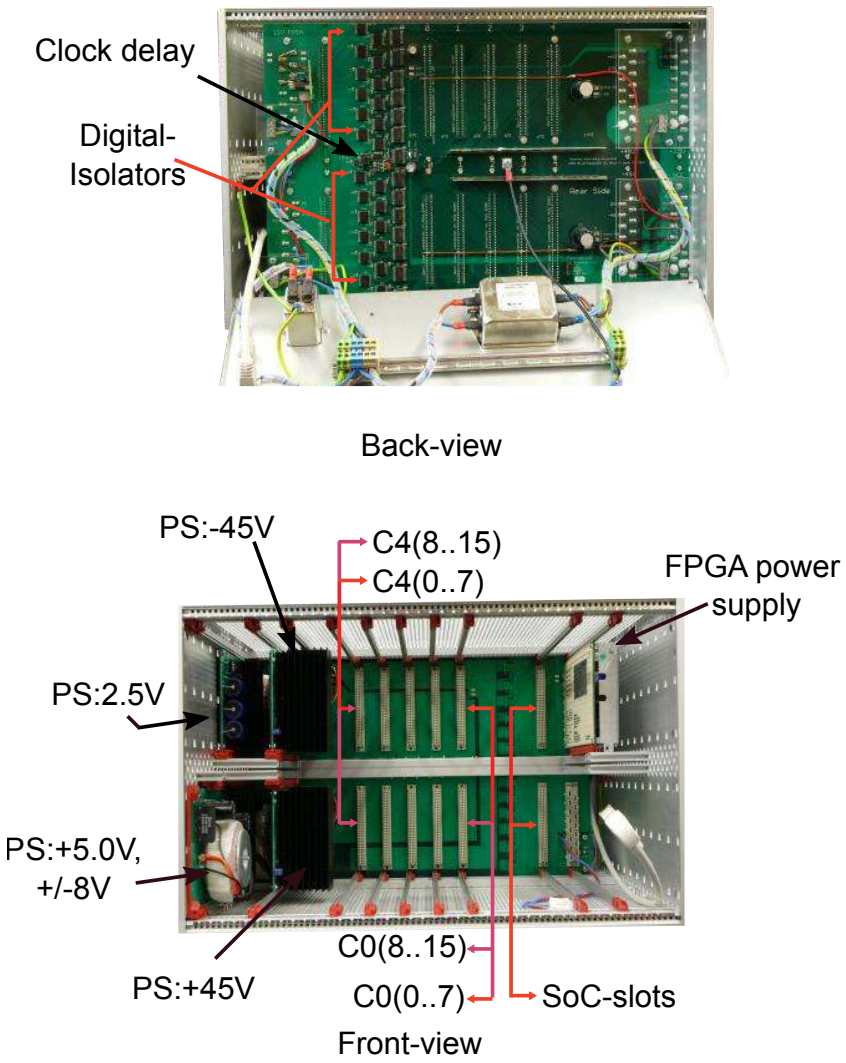


Fig. E.2 Introduction to essential digital and analog components of back-planes, installed on front and backside of backplane-PCB.

Troubleshoot: The most common error observed in backplane is burnout of installed digital isolators. Therefore, if any of the analog channels are not working, probe the dataline before and after digital isolator.

Display of device installation and available features in N_Bertha

```
Welcome to QuantenBit Multi_Channel Waveform Generator(MCWG-NEW_BERTHA)
Type: (BS 16) @JGU (Uni-Mainz)
Release: N_Bertha2017
Release Date:28_Aug_2017
@ www.quantenbit.de
@ Quantum AG Smidth Kaler
@ Designed and Developed by Vidyut Kaushal, Heinz lenk and Ulrich Poschinger

Release Features:
1.Improved Forced_idle_system(soft Reset),
2.Repeat_Sequence,
3.Repeat_Sequence_With_new_loop_number
4.close_socket_request
5.Sequence Ending Information
6.Push Button added to generate a sinus test sequence(press SW5)
7.Improved voltage consistency for other Channels.
8.Support for addition of Timing information.
9.Improved R_lines and Burst_number algorithm
10.Minimum wait interval(resolution) via timing protocol is 40 ns,
wait interval above 40 ns is accurate within resolution of 20ns.

IMPORTANT: Connect Ethernet for successful initialization of all modules!
---------------------------------
Initializing MCWG Clocks......
Master clk(M_CLK) initialized to 401 (400Mhz)
FIFO(FF) Wr clk(WR_CLK) initialized to 2 (M_CLK/2)
FF Rd(RD_CLK and MCWG clk frequency) initialized to 8 (M_CLK/8)
```

```
FF WR_duty_cycle(should be C350)= C350
FF Rd_duty_cycle(should be C350)= C350
FIRST= 7
Second= 2
MCWG Clock Initialized

-----Machine ready for programming -
Auto configuring all channels to 0 V...
-----------------------------------
Master00 Initialized at 0x22600000
Master01 Initialized at 0x6400000

Device Specification of Shuttling based Quantum Computing:
Supported memory 2x450 MB
Max. programmable samples  4718592 on each analog channels (4 million samples)
Number of supported output analog channels for segment control: 80 per unit.
Number of supported output digital channels for pulse shaping: 24 per unit.
Number of supported input digital channel for external trigger: 1 per unit.
Digital Resolution: 20ns, Analog resolution: 380ns.
Use SW5 on board push button to start and stop auto testing sequence.
Note:Scalable with more units using external trigger only. Check for
exclusive program designed for this purpose
---------------------------------
All Channel set to 0 V (Interrupt check: OK).
---------------------------------
Initializing MCWG ip configuration...
Board IP:       172.16.1.10
Netmask :       255.255.255.0
Gateway :       172.16.1.1
Start PHY autonegotiation
Waiting for PHY to complete autonegotiation.
autonegotiation complete
link speed for phy address 7: 1000
=================================
QuantenBit MCWG:Ready to Connect...
```

Visual error codes in experimental control system(N_Bertha)

- **Error CODE:1** Machine(Module_0:M00) is going through timing content of sequence, which means last loaded sequence has in-sequence for module M00 wait durations which is being executed. Please check encoded sequence for wait time related error.
- **Error CODE:2** Machine(Module_1:M01) is going through timing content of sequence for second module (M01) similar to Error CODE:1. Please check encoded sequence for wait time related error.
- **Error CODE:3**, Similar error like **Error CODE:1** and **Error CODE:2**, it states problems exist with both modules. Please check encoded sequence for wait time related error
- **Error CODE:4**, Desired trigger in experimental code is not possible, problem in module(M00). Please check encoded sequence for wait time related error
- **Error CODE:5**, Desired trigger in experimental code is not possible, problem in module(M01). Please check encoded sequence for wait time related error
- **Error CODE:6**, Desired trigger in experimental code is not possible, problem in module(M00 and M01). Please check encoded sequence for wait time related error
- **Error CODE:7** Not programmed

The device has been passed the test for randomly generated sequence over six months. So, there is minimal chances for non-executable sequences. Therefore, for the problem related

to non-executable experimental, it is recommended to check experimental sequence. A very common error has been request of experiment at negative time. Also, the software soft reset provides an option to perform smooth resetting of device the without loosing ions. For most of the times, software reset is good enough,but in case if SOFTWARE reset cannot reset, hardware reset via reset pin shall do the job, without loosing ions.

Restarting the device (turn off/on) will lose the trapped-ions as some voltages swings in between [-40:40] in uncontrolled fashion before actual control is handed over to FPGA. Initialization or Re-initialization takes 6 s.

For exact information on the error, the error registers can be investigated. Please see Sec. C.3 for detail information.

Acronyms

AHB advanced high-performance bus

AOM acousto-optic modulators

APB advanced peripheral bus

API application programming interface

BRAM block random access memory

BS burst Size

CIP custom intellectual property

COM center of mass

CS Chip-Select line

DAC digital to analog converter

DAQ data acquisition

DFF d-flip flop

DHCP Dynamic host configuration protocol

DIC digital input code

DIN data input lines

DIC digital input code

DMA direct memory transfer

DNL differential non-linearity

EMCCD electron-multiplying charge coupled device

FIFO first In first Out

FPGA field programmable gate array

FWFT first word fall through

GEC gigabit Ethernet controller

GIA glitch impulse area

GPIO general purpose input and output

GUI graphical user interface

HP high performance

HPC high pin counts

IDC insulation displacement connector

INL integral non-linearity

IP Intellectual property

LPC low pin counts

LSB least significant bit

LW lightweight

MAC media access controller

mAWG multi-channel arbitrary waveform generator

MCP master control program

MSPS mega samples per second

MTU maximum transmission unit

N_Bertha New Bertha

OCM onChip memory

ODDR Output DDR primitive

OpAmp Operational amplifier

OS Operating System

PCB printed circuit boards

PL programming logic

PMT photo multiplier tube

PS processing system

QCCD charge coupled device

ROCK out-of-phase

SFDR spurious free dynamic range

SG scatter gather

SM state machine

SoC System on Chip

SPI serial programming interface

THD total harmonic distortion

VFG versatile frequency generator